ECEN 248 –Introduction to Digital Systems Design (Spring 2008)

(Sections: 501, 502, 503, 507)

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Programmable logic device (PLD)

- A PLD is a general-purpose chip for implementing logic circuit.
- It contains a collection of logic circuit elements that can be customized in different ways.
- A PLD can be viewed as a "black box" that contains logic gates and programmable switches.
- The programmable switches allow the logic gates inside the PLD to be connected together to implement logic circuits.

Programmable logic device as a black box

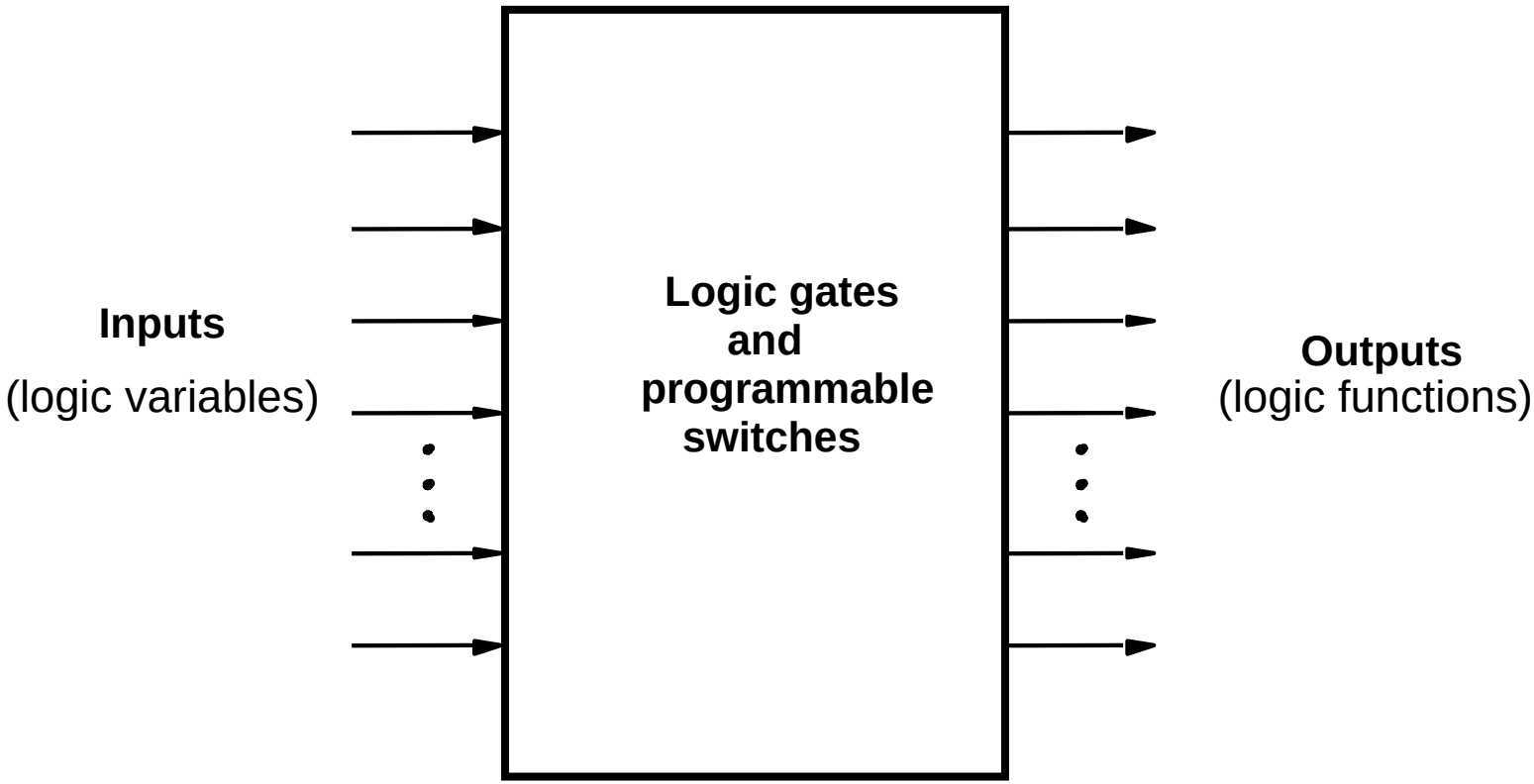


Figure 3.24. Programmable logic device as a black box.

Programmable logic devices

- Different types of PLD
  - Simple PLD (SPLD)
    - Programmable logic array (PLA)
    - Programmable array logic (PAL)
  - Complex PLD (CPLD)
  - Field-programmable gate arrays (FPGA)

Programmable logic array (PLA)

- PLA is developed based on the sum-of-product form.
- A PLA includes a circuit block called an AND plane (or AND array) and a circuit block called an OR plane (or OR array).
- Input → Buffer/inverters → And plane → OR plane → Output

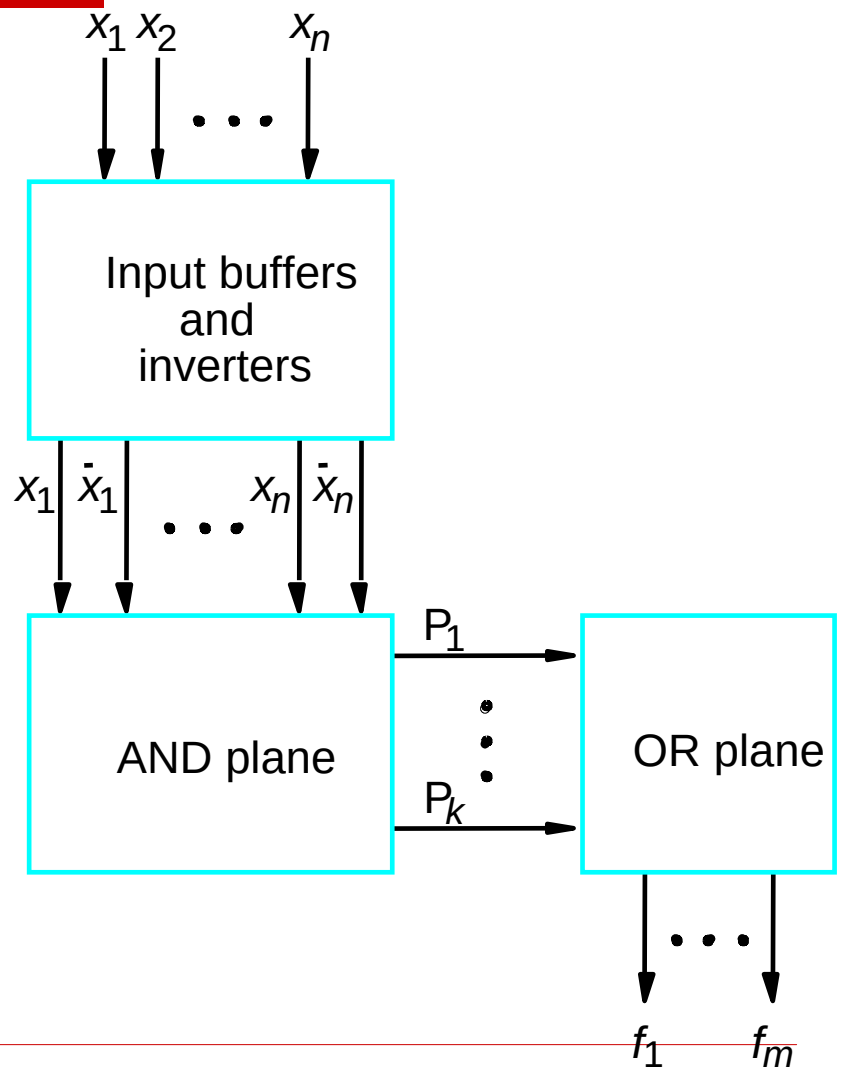
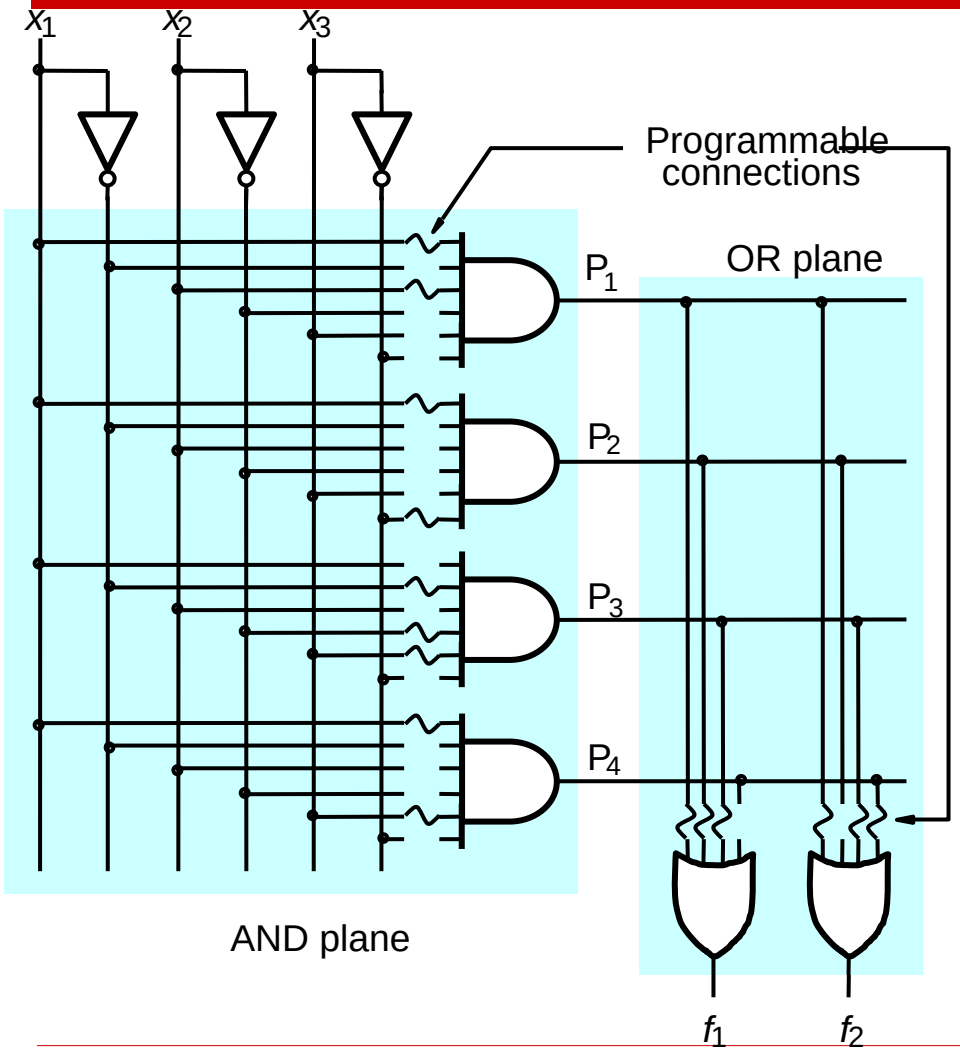


Figure 3.25. General structure of a PLA.

Gate-level diagram of a PLA



Output of And plane:

$$P_1 = x_1 x_2$$

$$P_2 = x_1 \bar{x}_3$$

$$P_3 = \bar{x}_1 \bar{x}_2 x_3$$

$$P_4 = x_1 x_3$$

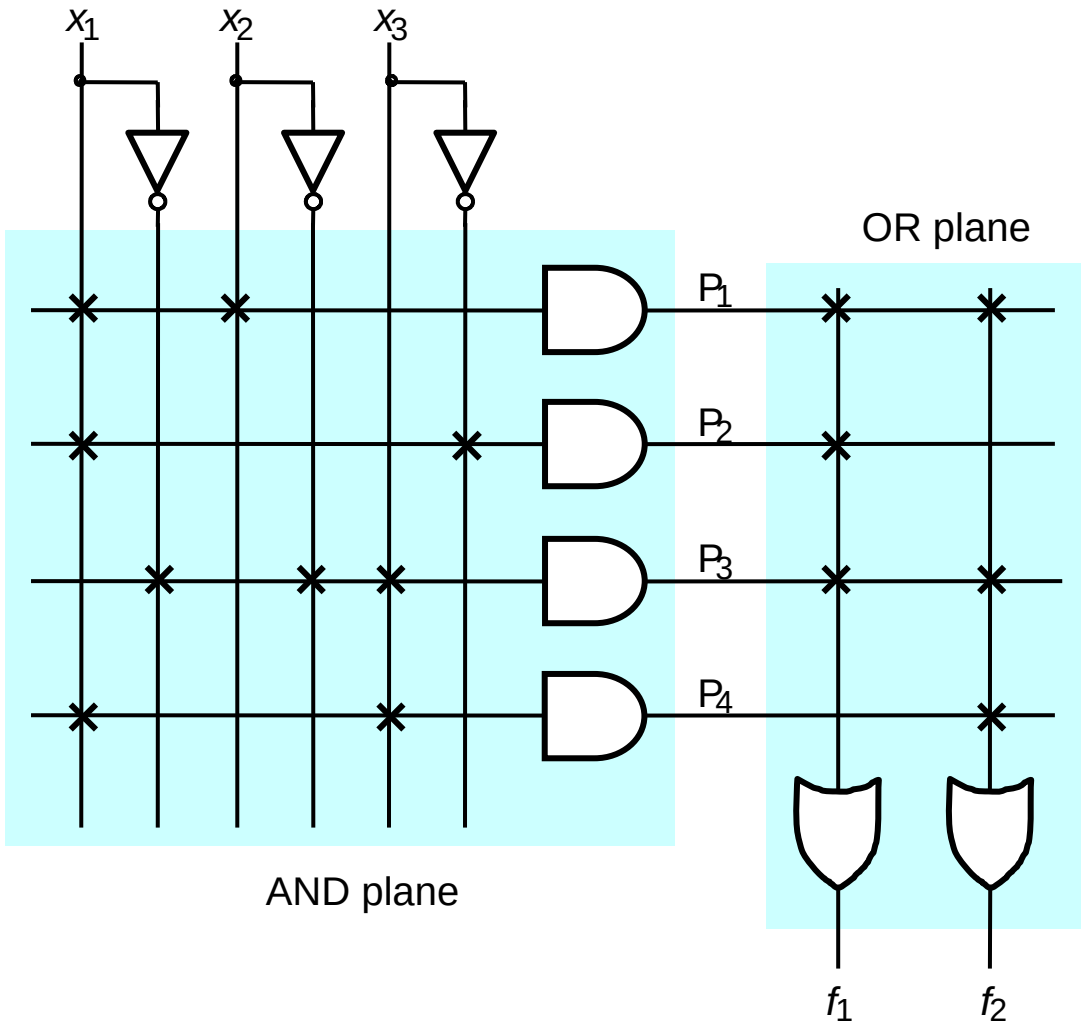
Output of OR plane:

$$f_1 = x_1 x_2 + x_1 \bar{x}_3 + \bar{x}_1 \bar{x}_2 x_3$$

$$f_2 = x_1 x_2 + x_1 \bar{x}_2 \bar{x}_3 + x_1 x_3$$

Figure 3.26. Gate-level diagram of a PLA.

Customary schematic for the PLA



Output of And plane:

$$P_1 = x_1 x_2$$

$$P_2 = x_1 \bar{x}_3$$

$$P_3 = \bar{x}_1 \bar{x}_2 x_3$$

$$P_4 = x_1 x_3$$

Output of OR plane:

$$f_1 = x_1 x_2 + x_1 \bar{x}_3 + \bar{x}_1 \bar{x}_2 x_3$$

$$f_2 = x_1 x_2 + \bar{x}_1 \bar{x}_2 x_3 + x_1 x_3$$

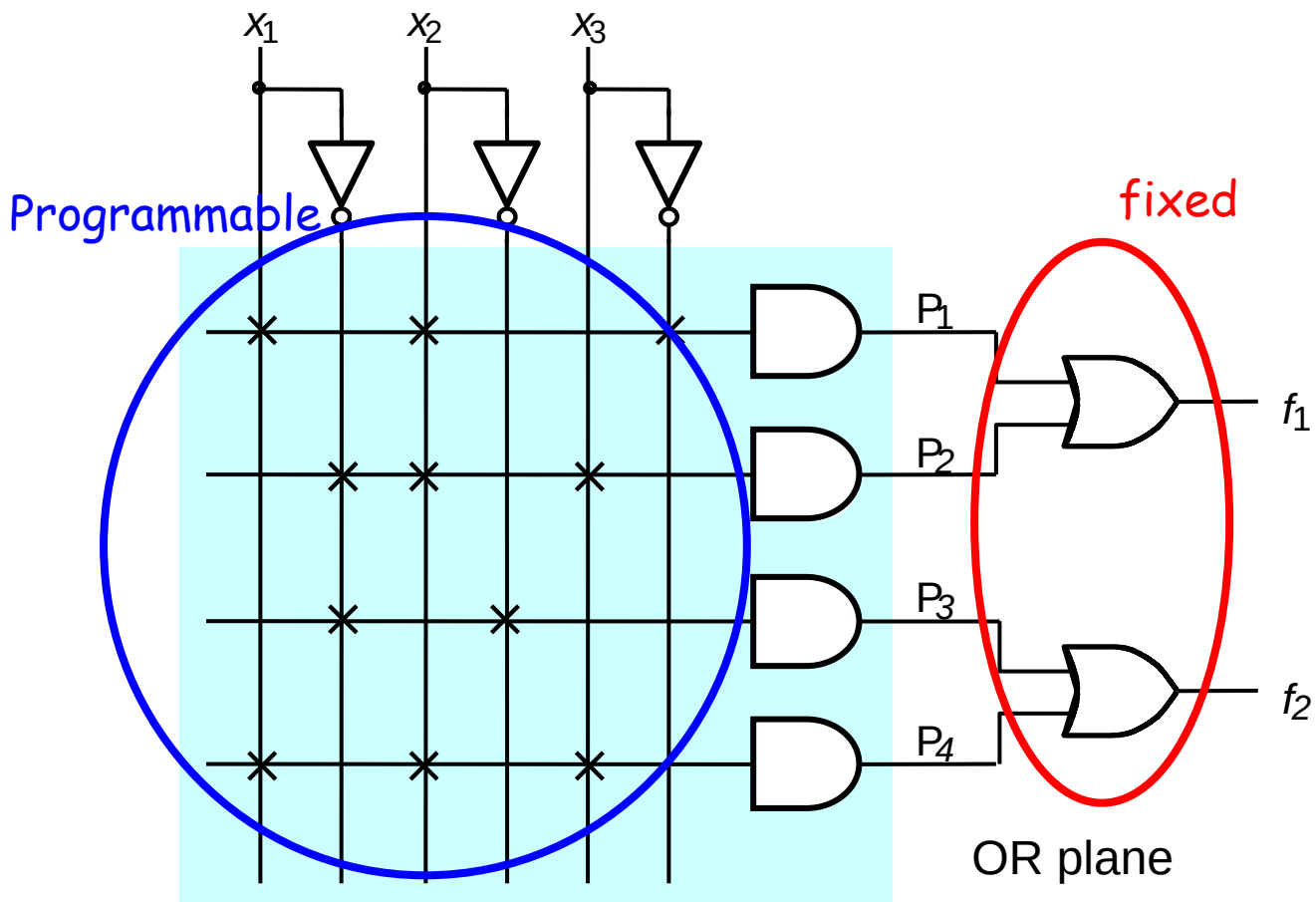
Figure 3.27. Customary schematic for the PLA in Figure 3.26.

Programmable array logic (PAL) device

- Programmable array logic (PAL) device

  PAL is a programmable logic device similar to PLA.
- Difference between PLA and PAL
  - PLA: both AND plane and OR plane are programmable.
  - PAL: Only AND plane is programmable, while OR plane is fixed.

An example of a PAL



$$P_1 = x_1 x_2 \bar{x}_3$$

$$P_2 = \bar{x}_1 x_2 x_3$$

$$P_3 = \bar{x}_1 \bar{x}_2$$

$$P_4 = x_1 x_2 x_3$$

$$f_1 = x_1 x_2 \bar{x}_3 + \bar{x}_1 x_2 x_3$$

$$f_2 = \bar{x}_1 \bar{x}_2 + x_1 x_2 x_3$$

Figure 3.28. An example of a PLA.

Comparison between PLA and PAL

- Comparison between PLA and PAL
  - Drawbacks of PLA
    - PLA were hard to be implemented
    - PLA reduced the speed performance of circuits.
  - Advantage of PAL
    - Simple to manufacturers
    - Less expensive
    - Better performance
  - Disadvantage of PAL
    - Not flexible as compared PLA, because OR plane is fixed.

Complex Programmable Logic Device (CPLDs)

- SPLDs, including PLA, PAL, and etc, are useful for implementing a wide variety of small digital circuits.
- CPLD are used to implement more sophisticated type of chip.

Complex Programmable Logic Device (CPLDs)

- A CPLD comprises multiple circuit blocks on a single chip, with internal wiring resources to connect the circuit blocks.
- Each circuit block is similar to a PLA or a PAL
- We will refer to the circuit blocks as PAL-like blocks.

Complex Programmable Logic Device (CPLDs)

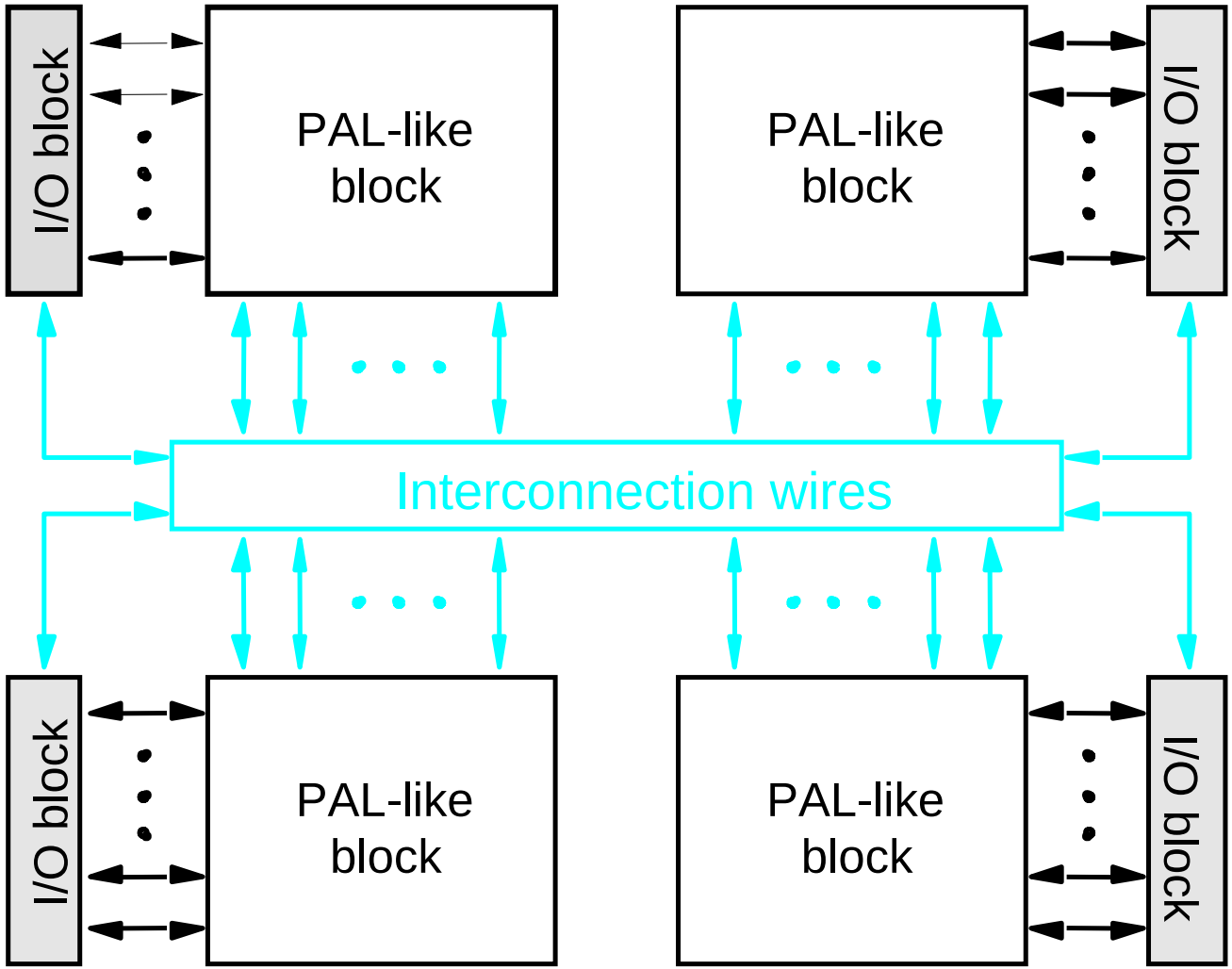


Figure 3.32. Structure of a complex programmable logic device (CPLD).

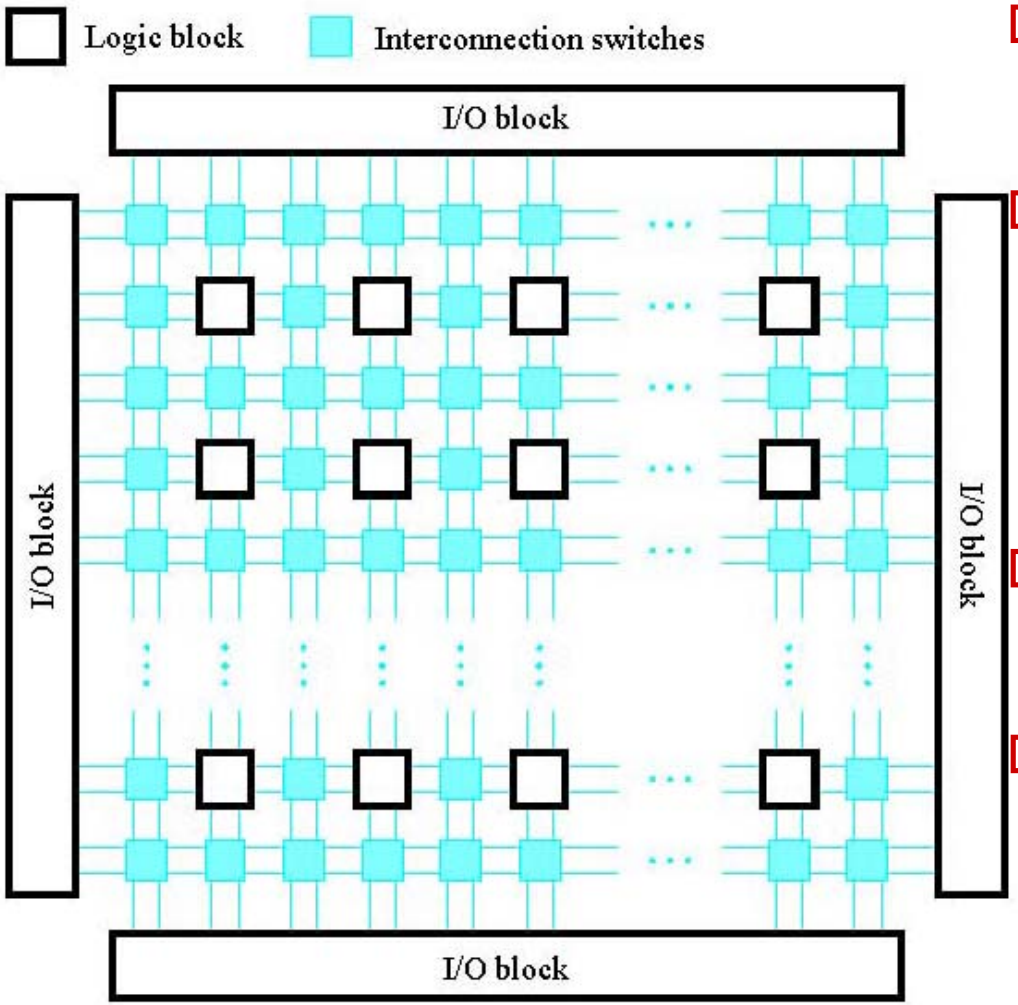
Field-Programmable Gate Arrays (FPGA)

- Larger and larger logic circuits need to accommodate in a single chip.
- One way to quantify a circuit's size is to assume that the circuit is to be built using only simple logic gates and then estimate how many of these gates are needed.
- A commonly used measure is the total number of two-input NAND gates. This measure is often called the number of equivalent gates.
- By modern standards, a logic circuit with 10,000 gates is not large.

Field-Programmable Gate Arrays (FPGA)

- FPGA is a programmable logic device that supports implementation of relatively large logic circuits.
- Not like CPLD, FPGAs do not contain AND or OR planes.
- Instead, FPGAs provide logic blocks for connecting to the pins of the package, and interconnection wires and switches.

General structure of an FPGA



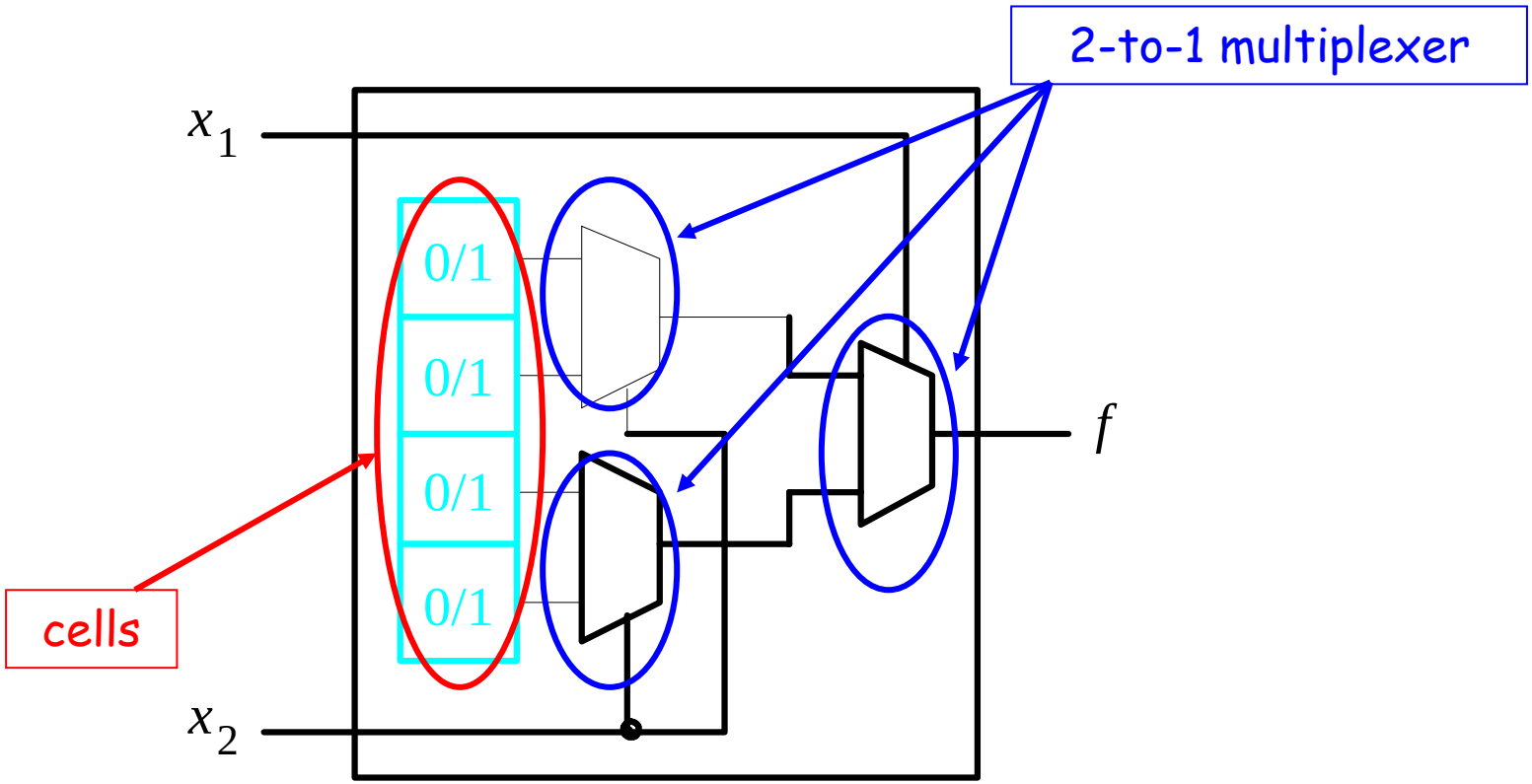
(a) General structure of an FPGA

- The logic blocks are arranged in a two-dimensional array, depicted as hollow black box;
- The interconnection wires, depicted as solid blue box, are organized as horizontal and vertical routing channels between rows and columns of logic blocks.
- Programmable connections also exist between I/O blocks and the interconnection wires.
- FPGA can implement circuit of more than a million equivalent gates in size.

Lookup Table (LUT)

- Lookup table (LUT) is the most commonly used logic block in FPGA.
- A lookup table contains storage cells that are used to implement a small logic function.
- Each cell is capable of holding a single logic value, either 0 or 1.
- LUTs of various sizes may be created, where the size is defined by the number of inputs.
- LUTs are implemented by using multiplexers.

Circuits for a two-input lookup table



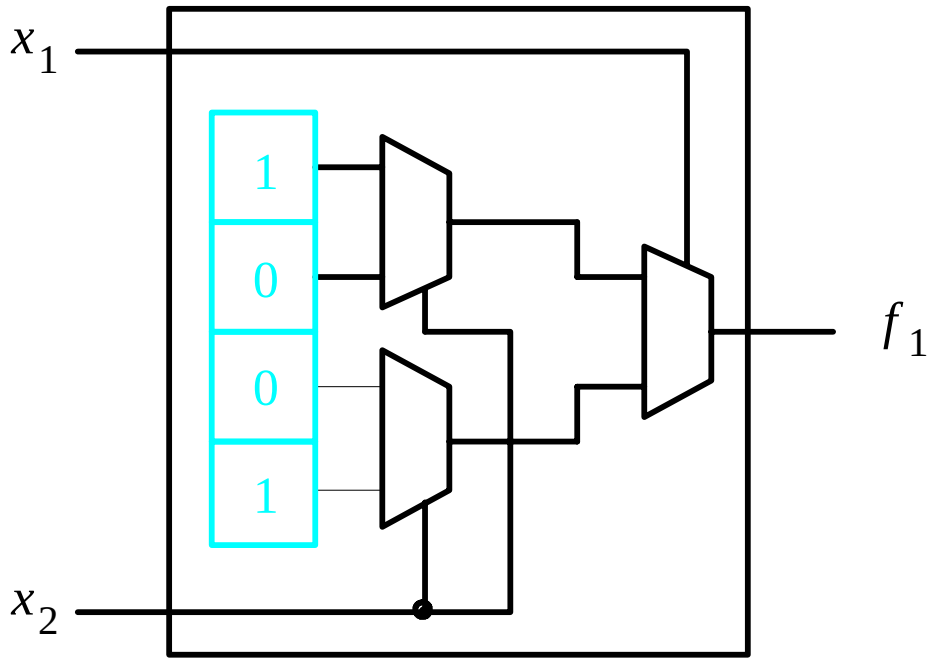
(a) Circuit for a two-input LUT

Figure 3.36. A two-input lookup table (LUT).

Example of a two-input lookup table

x_1	x_2	f_1
0	0	1
0	1	0
1	0	0
1	1	1

(b) $f_1 = \bar{x}_1\bar{x}_2 + x_1x_2$



(c) Storage cell contents in the LUT

Figure 3.36. A two-input lookup table (LUT).

A three-input LUT

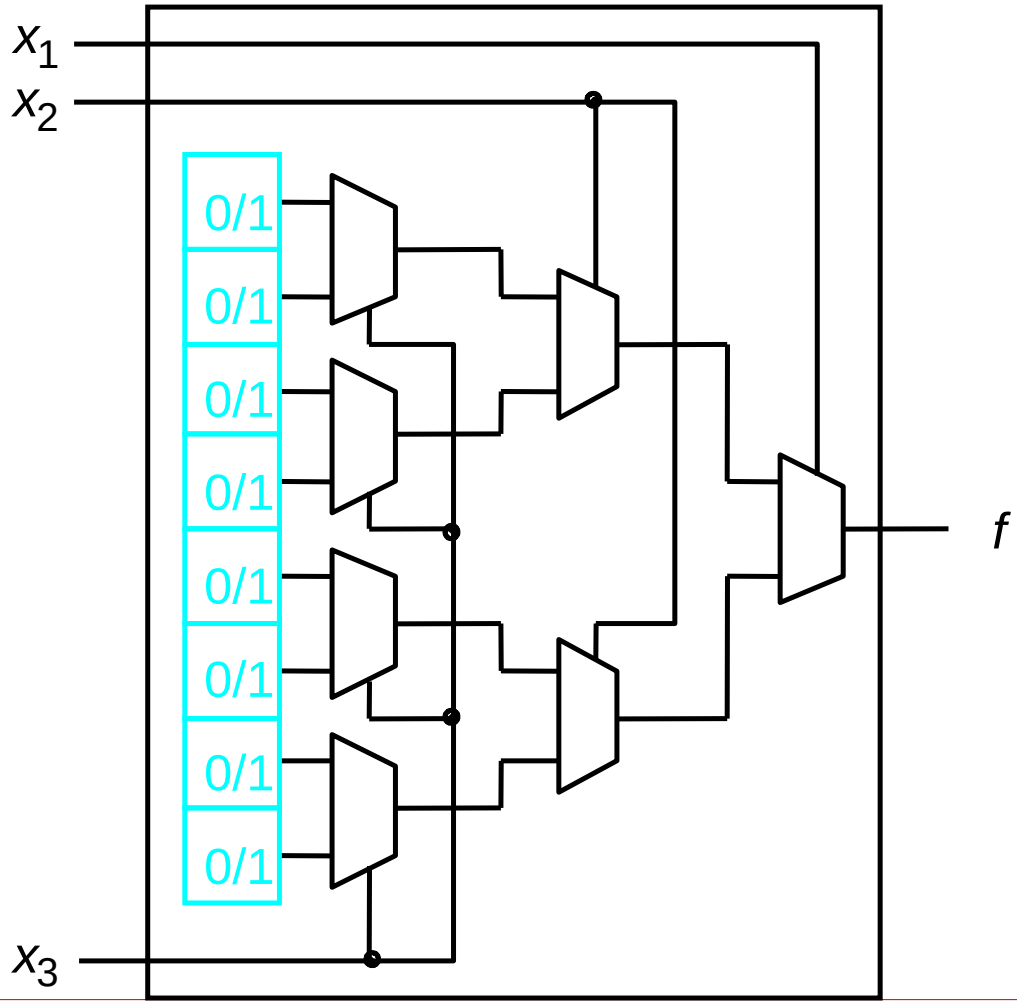
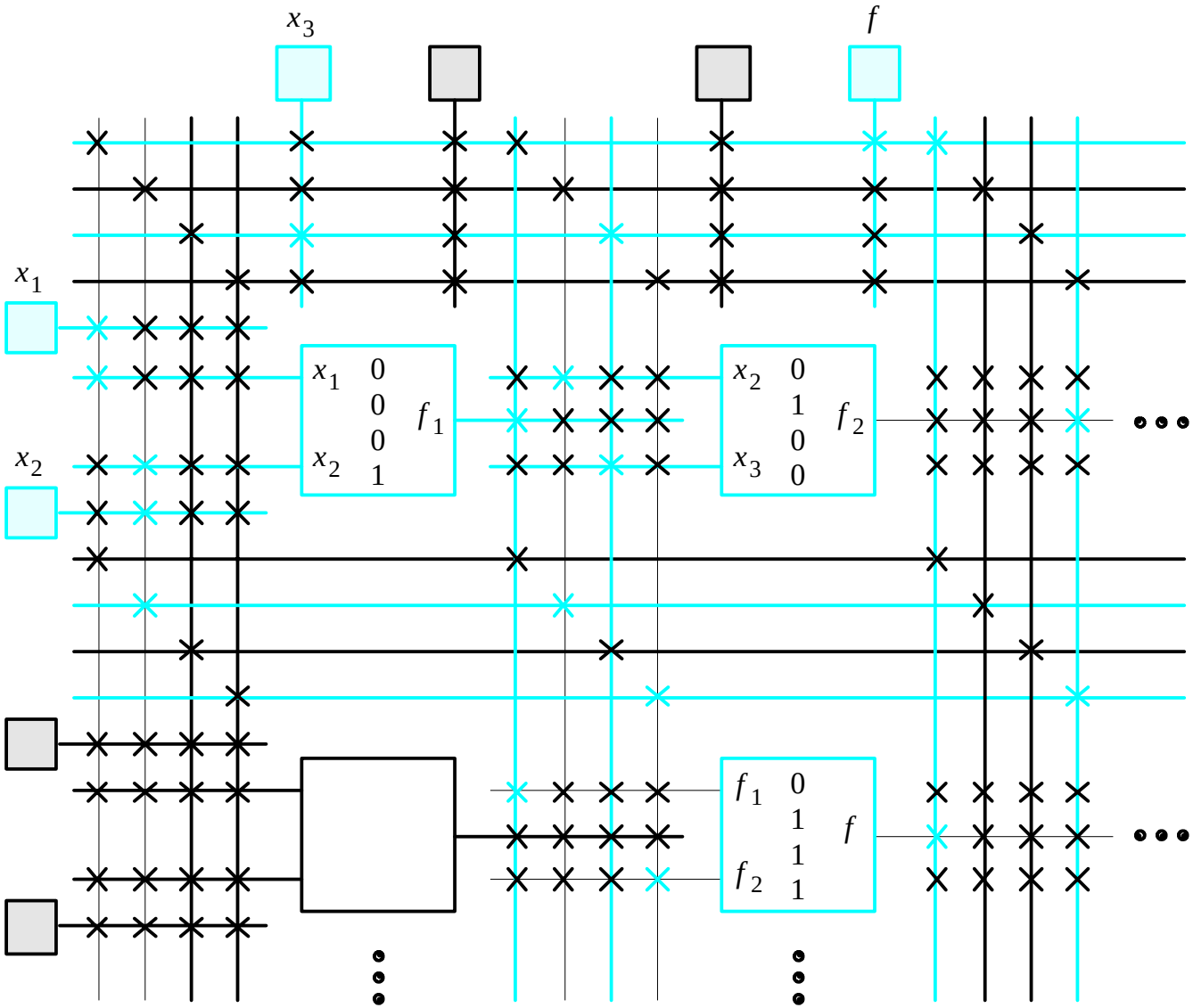


Figure 3.37. A three-input LUT.



- This section includes 3 lookup tables.
- Using the 3 lookup tables, we implement output function *f*.

$$f_1 = x_1 x_2$$

$$f_2 = \overline{x}_2 x_3$$

$$\downarrow$$

$$f = f_1 + f_2$$

Figure 3.39. A section example of a programmed FPGA.