8.5. A minimal state table is

Present state	Next State $w=0$	Next State $w=1$	Output z
A	A	B	0
B	E	C	0
C	D	C	0
D	A	F	1
E	A	F	0
F	E	C	1

8.6. An initial attempt at deriving a state table may be

Present state	Next state		Output z	
	$w=0$	$w=1$	$w=0$	$w=1$
A	A	B	0	0
B	D	C	0	0
C	D	C	1	0
D	A	E	0	1
E	D	C	0	0

States B and E are equivalent; hence the minimal state table is

Present state	Next state		Output z	
	$w=0$	$w=1$	$w=0$	$w=1$
A	A	B	0	0
B	D	C	0	0
C	D	C	1	0
D	A	B	0	1

8.7. For Figure 8.51 have (using the straightforward state assignment):

	Present state $y_3y_2y_1$	Next state $w=0$ $Y_3Y_2Y_1$	Next state $w=1$ $Y_3Y_2Y_1$	Output z
A	0 0 0	0 0 1	0 1 0	1
B	0 0 1	0 1 1	1 0 1	1
C	0 1 0	1 0 1	1 0 0	0
D	0 1 1	0 0 1	1 1 0	1
E	1 0 0	1 0 1	0 1 0	0
F	1 0 1	1 0 0	0 1 1	0
G	1 1 0	1 0 1	1 1 0	0

This leads to

$$\begin{aligned}
Y_3 &= \overline{w}y_3 + \overline{y}_1y_2 + wy_1\overline{y}_3 \\
Y_2 &= wy_3 + w\overline{y}_1\overline{y}_2 + wy_1y_2 + \overline{w}y_1\overline{y}_2\overline{y}_3 \\
Y_1 &= \overline{y}_3\overline{w} + \overline{y}_1\overline{w} + wy_1\overline{y}_2 \\
z &= y_1\overline{y}_3 + \overline{y}_2\overline{y}_3
\end{aligned}$$

For Figure 8.52 have

	Present state y_2y_1	Next state $w=0$ Y_2Y_1	Next state $w=1$ Y_2Y_1	Output z
A	0 0	0 1	1 0	1
B	0 1	0 0	1 1	1
C	1 0	1 1	1 0	0
F	1 1	1 0	0 0	0

This leads to

$$\begin{aligned}
Y_2 &= \overline{w}y_2 + \overline{y}_1y_2 + w\overline{y}_2 \\
Y_1 &= \overline{y}_1\overline{w} + wy_1\overline{y}_2 \\
z &= \overline{y}_2
\end{aligned}$$

Clearly, minimizing the number of states leads to a much simpler circuit.

8.8. For Figure 8.55 have (using straightforward state assignment):

	Present state $y_4y_3y_2y_1$	Next state				Output z
		DN=00	01	10	11	
		$Y_4Y_3Y_2Y_1$				
S1	0 0 0 0	0 0 0 0	0 0 1 0	0 0 0 1	–	0
S2	0 0 0 1	0 0 0 1	0 0 1 1	0 1 0 0	–	0
S3	0 0 1 0	0 0 1 0	0 1 0 1	0 1 1 0	–	0
S4	0 0 1 1	0 0 0 0	–	–	–	1
S5	0 1 0 0	0 0 1 0	–	–	–	1
S6	0 1 0 1	0 1 0 1	0 1 1 1	1 0 0 0	–	0
S7	0 1 1 0	0 0 0 0	–	–	–	1
S8	0 1 1 1	0 0 0 0	–	–	–	1
S9	1 0 0 0	0 0 1 0	–	–	–	1

The next-state and output expressions are

$$
\begin{aligned}
Y_4 &= Dy_3 \\
Y_3 &= Dy_1 + Dy_2 + Ny_2 + \overline{D}y_3\overline{y}_2y_1 \\
Y_2 &= N\overline{y}_2 + y_3\overline{y}_1 + \overline{N}\overline{y}_3y_2\overline{y}_1 \\
Y_1 &= Ny_2 + D\overline{y}_2\overline{y}_1 + \overline{D}\overline{y}_2y_1 \\
z &= y_4 + y_1y_2 + \overline{y}_1y_3
\end{aligned}
$$

Using the same approach for Figure 8.56 gives

	Present state $y_3y_2y_1$	Next state				Output z
		DN=00	01	10	11	
		$Y_3Y_2Y_1$				
S1	0 0 0	0 0 0	0 1 0	0 0 1	–	0
S2	0 0 1	0 0 1	0 1 1	1 0 0	–	0
S3	0 1 0	0 1 0	0 0 1	0 1 1	–	0
S4	0 1 1	0 0 0	–	–	–	1
S5	1 0 0	0 1 0	–	–	–	1

The next-state and output expressions are:

$$
\begin{aligned}
Y_3 &= D\overline{y}_2y_1 \\
Y_2 &= y_3 + \overline{N}y_2\overline{y}_1 + N\overline{y}_2 \\
Y_1 &= \overline{D}\overline{y}_2y_1 + Ny_2\overline{y}_1 + D\overline{y}_3\overline{y}_1 \\
z &= y_3 + y_2y_1
\end{aligned}
$$

These expressions define a circuit that has considerably lower cost that the circuit resulting from Figure 8.55.

8.9. To compare individual bits, let $k = w_1 \oplus w_2$. Then, a suitable state table is

Present state	Next state		Output z	
	$k=0$	$k=1$	$k=0$	$k=1$
A	B	A	0	0
B	C	A	0	0
C	D	A	0	0
D	D	A	1	0

The state-assigned table is

Present state	Next State		Output	
	$k=0$	$k=1$	$k=0$	$k=1$
y_2y_1	Y_2Y_1	Y_2Y_1	z	z
00	01	00	0	0
01	10	00	0	0
10	11	00	0	0
11	11	00	1	0

The next-state and output expressions are

$$
\begin{aligned}
Y_2 &= \overline{k}y_1 + \overline{k}y_2 \\
Y_1 &= \overline{k}\overline{y}_1 + \overline{k}y_2 \\
z &= \overline{k}y_1y_2
\end{aligned}
$$

8.11. A possible minimum state table for a Moore-type FSM is

Present state	Next state		Output z
	$w = 0$	$w = 1$	
A	B	C	0
B	D	E	0
C	E	D	0
D	F	G	0
E	F	F	0
F	A	A	0
G	A	A	1