ECEN 248 –Introduction to Digital Systems Design (Spring 2008)

(Sections: 501, 502, 503, 507)

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Section 8.7 Design of A Counter Using Sequential Circuits

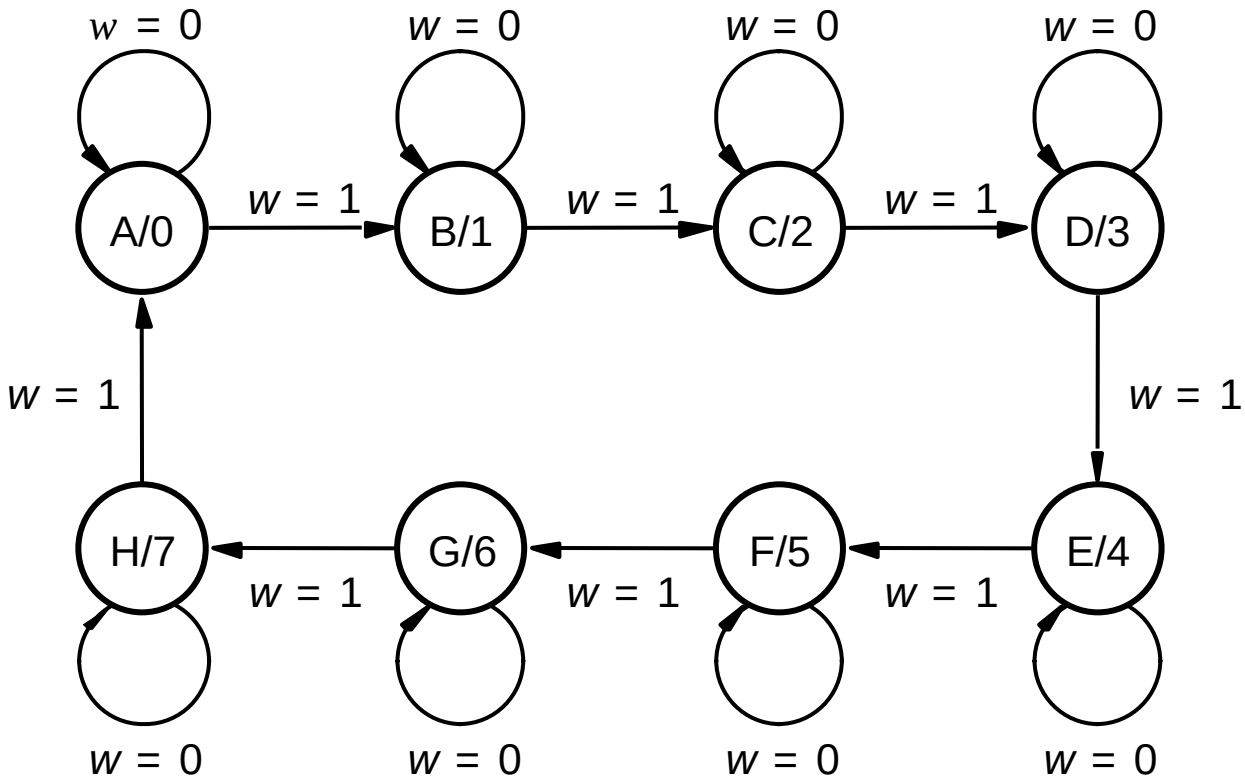

Figure 8.60. State diagram for the counter.

State Diagram and State Table for A Modulo-8 Counter

Present state	Next state		Output
	$w = 0$	$w = 1$	
A	A	B	0
B	B	C	1
C	C	D	2
D	D	E	3
E	E	F	4
F	F	G	5
G	G	H	6
H	H	A	7

Figure 8.61. State table for the counter.

State-assigned table for the counter

	Present state $y_2y_1y_0$	Next state		Count $z_2z_1z_0$
		$w = 0$	$w = 1$	
		$Y_2Y_1Y_0$	$Y_2Y_1Y_0$	
A	000	000	001	000
B	001	001	010	001
C	010	010	011	010
D	011	011	100	011
E	100	100	101	100
F	101	101	110	101
G	110	110	111	110
H	111	111	000	111

Figure 8.62. State-assigned table for the counter.

Karnaugh maps for D flip-flops for the counter

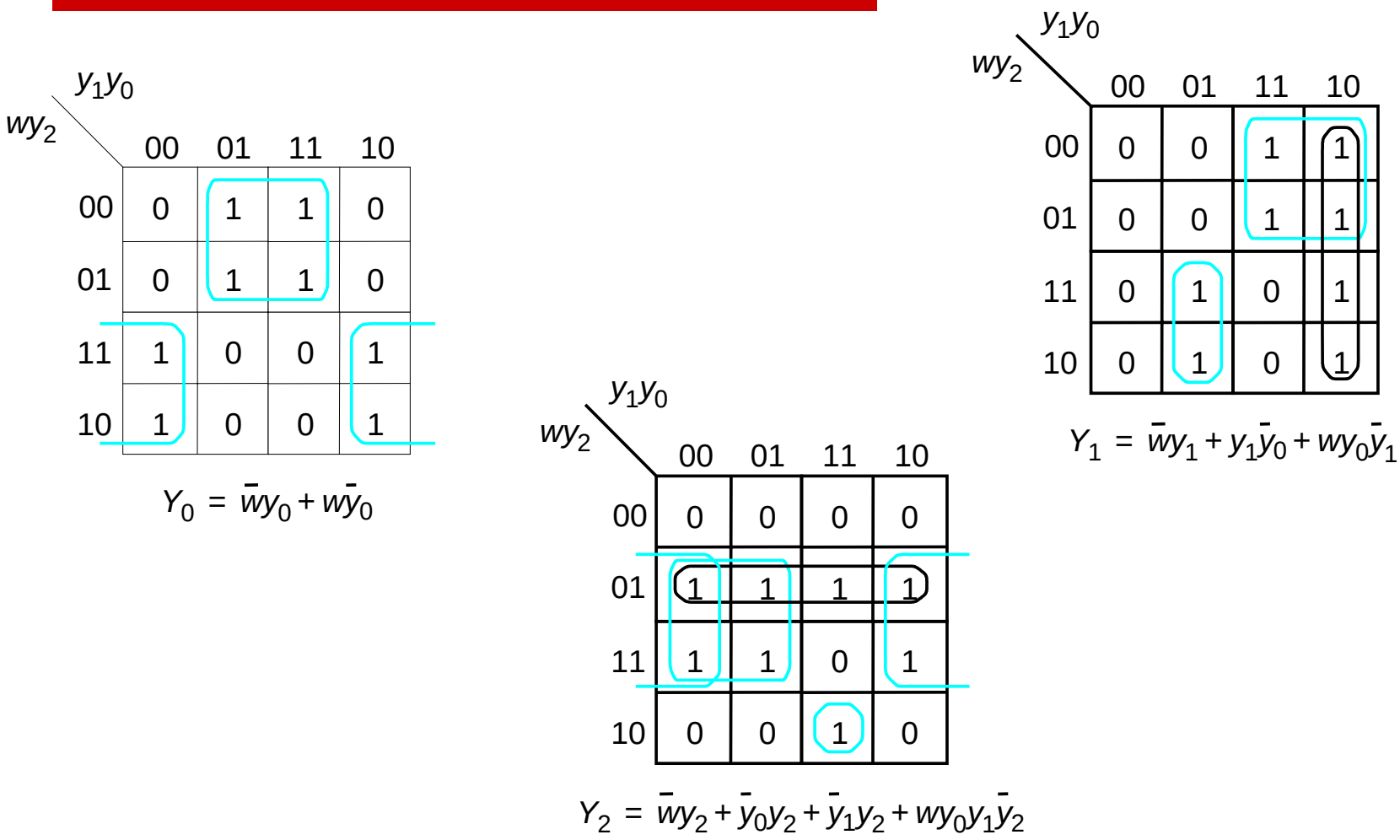

Figure 8.63. Karnaugh maps for D flip-flops for the counter.