ECEN 248 –Introduction to Digital Systems Design (Spring 2008)

(Sections: 501, 502, 503, 507)

Prof. Xi Zhang
ECE Dept, TAMU, 333N WERC
http://dropzone.tamu.edu/~xizhang/ECEN248

FSM for Sequence detector (Mealy Type)

- Unlike the Moore type machine, the output depends not only the current state, but also the current input.

Sequences of input and output signals

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w:	0	1	0	1	1	0	1	1	1	0	1
z:	0	0	0	0	1	0	0	1	1	0	0

Figure 8.22. Sequences of input and output signals.

State diagram of an FSM

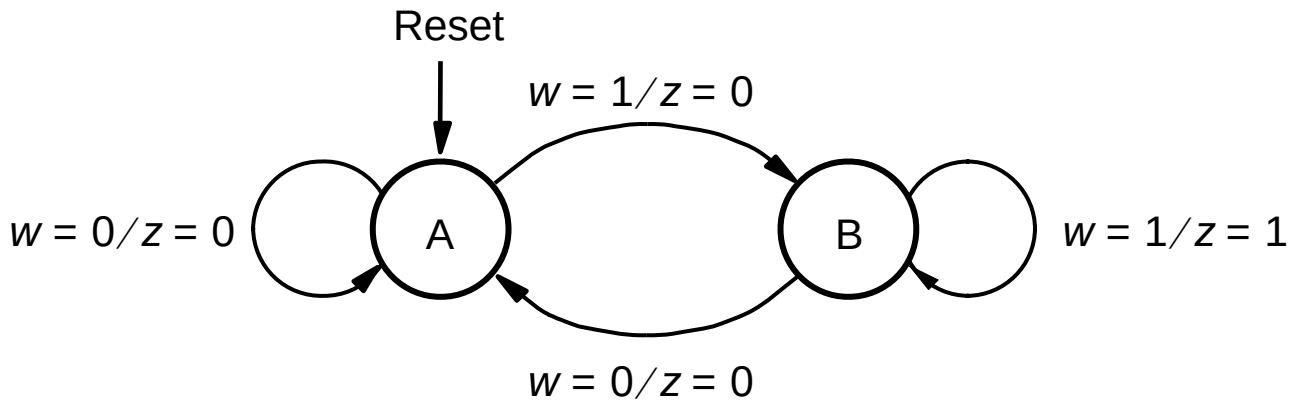
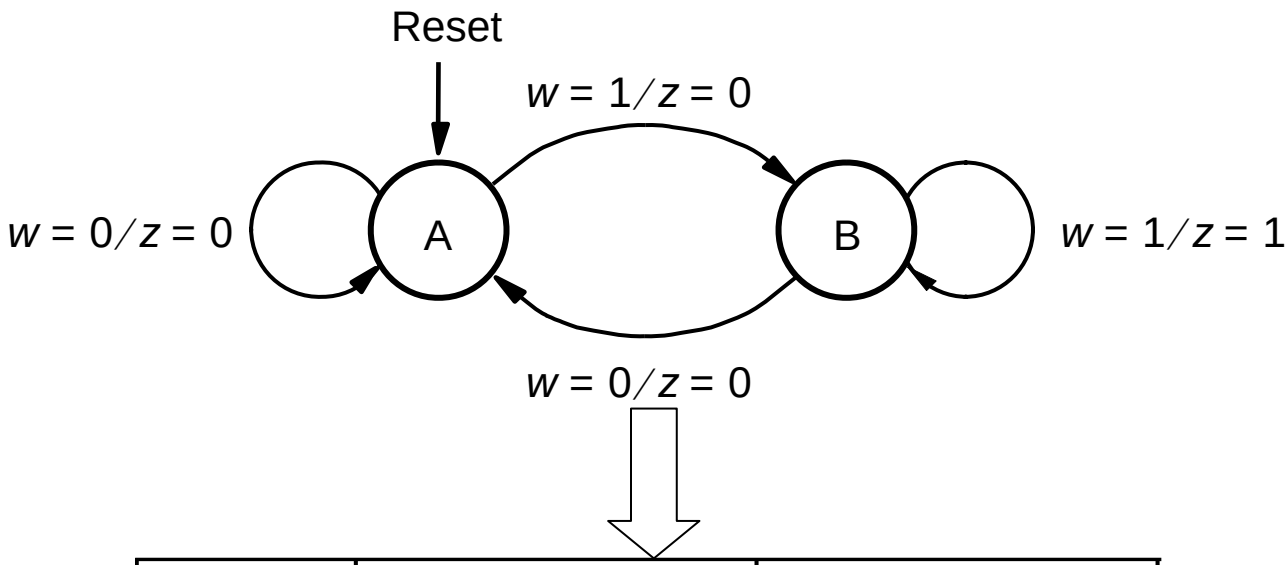


Figure 8.23. State diagram of an FSM that realizes the task in Figure 8.22.

- A: starting state, also the state after an input w=0 is applied.
- B: w=1 in immediately preceding clock cycle.

State table for the FSM

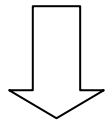


Present state	Next state		Output z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
A	A	B	0	0
B	A	B	0	1

Figure 8.24. State table for the FSM in Figure 8.23.

State-assigned table for the FSM

Present state	Next state		Output z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
A	A	B	0	0
B	A	B	0	1

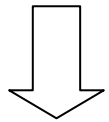


	Present state	Next state		Output	
		$w = 0$	$w = 1$	$w = 0$	$w = 1$
	y	Y	Y	z	z
A	0	0	1	0	0
B	1	0	1	0	1

Figure 8.25. State-assigned table for the FSM in Figure 8.24.

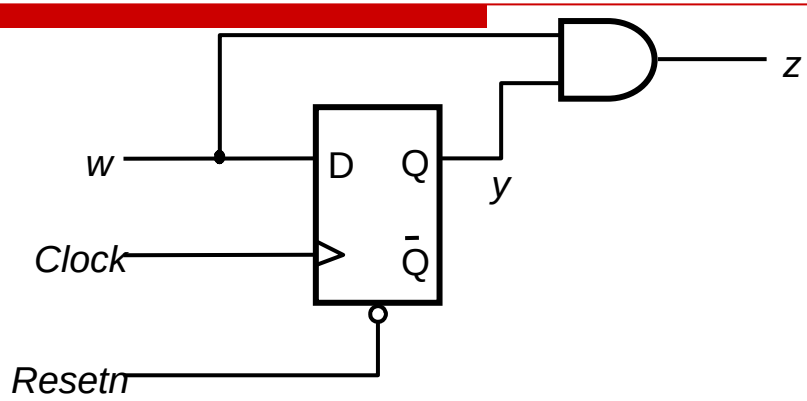
Derivation of the logic expressions

	Present state	Next state		Output	
		$w = 0$	$w = 1$	$w = 0$	$w = 1$
	y	Y	Y	z	z
A	0	0	1	0	0
B	1	0	1	0	1

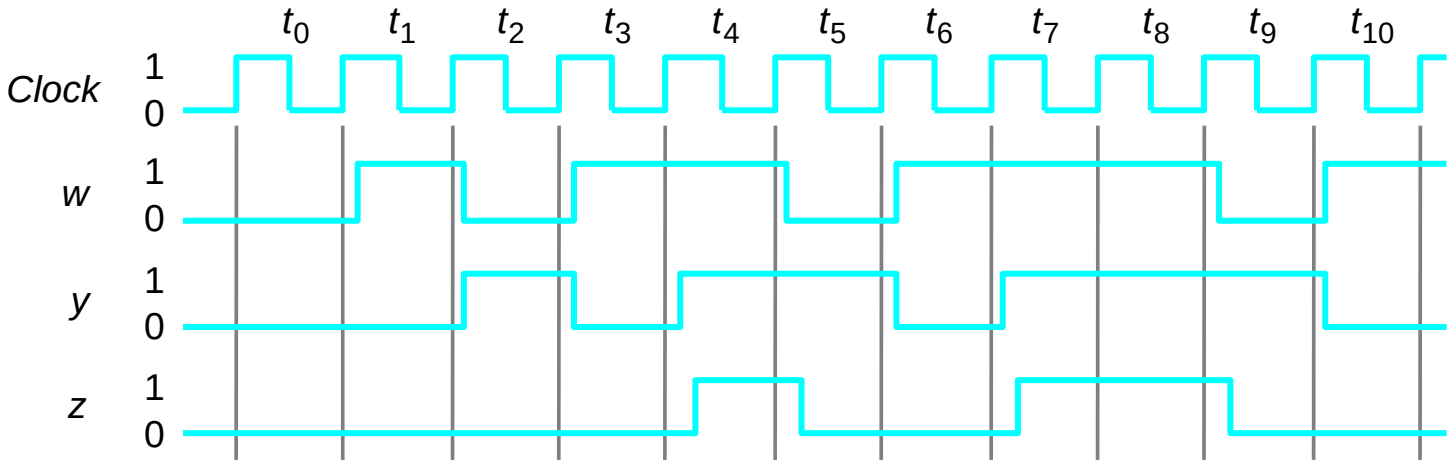


- Y = D = w;
- z = wy;

Implementation of FSM



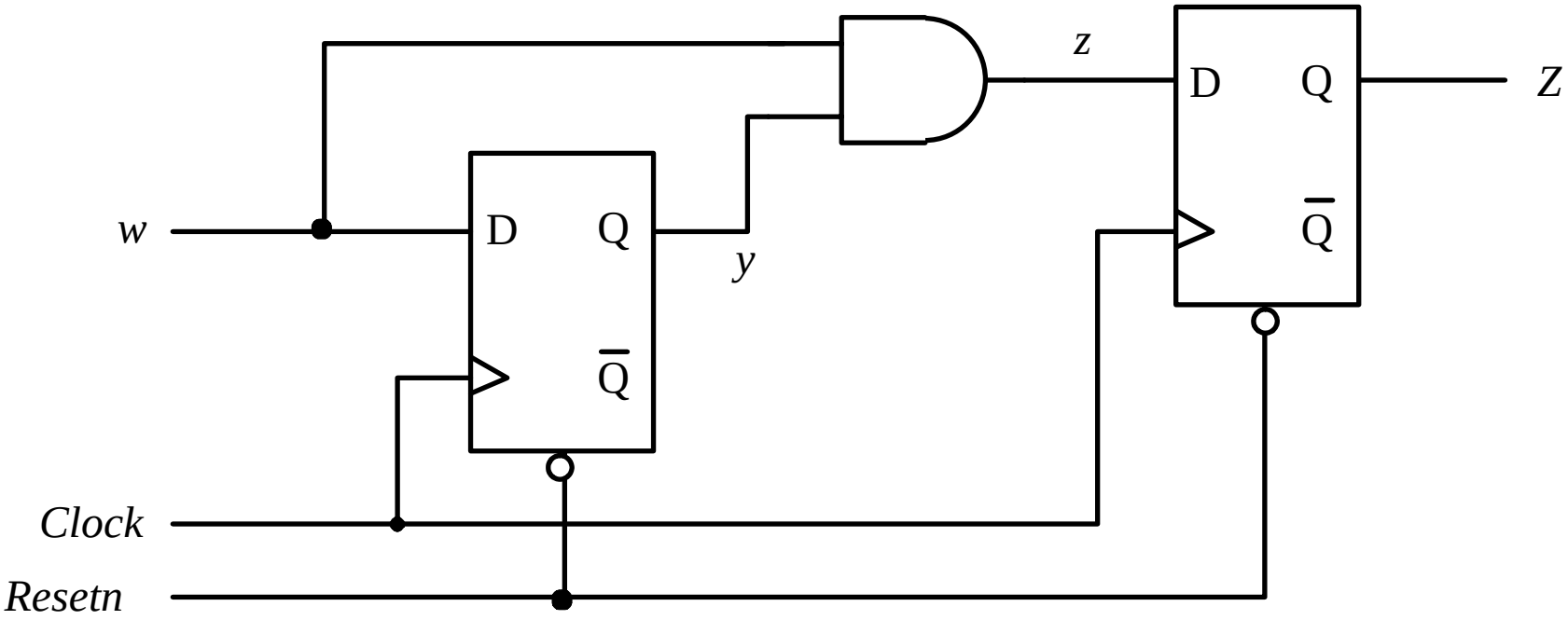
(a) Circuit



(b) Timing diagram

Figure 8.26. Implementation of FSM in Figure 8.25.

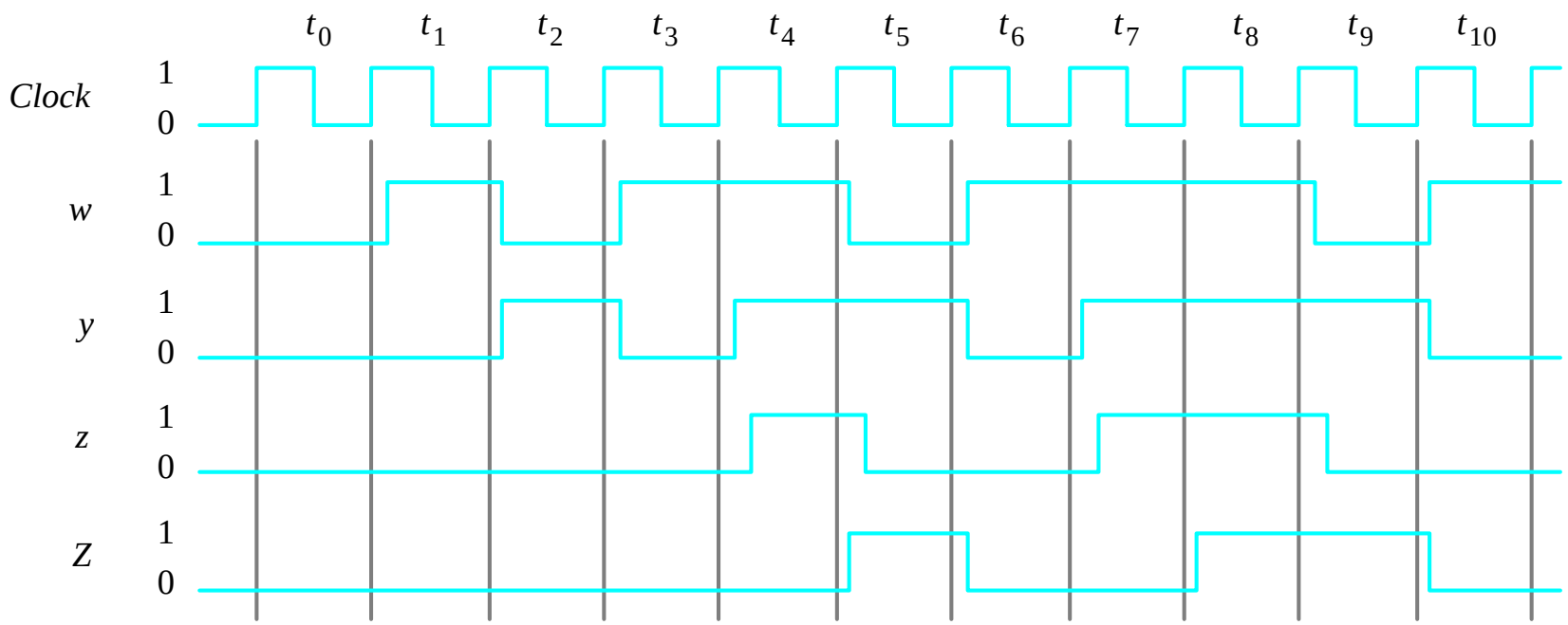
Circuit that implements the specification



(a) Circuit

Figure 8.27. Circuit that implements the specification in Figure 8.2.

Circuit that implements the specification



(b) Timing diagram

Figure 8.27. Circuit that implements the specification in Figure 8.2.

Break page between Ch 8.3 and 8.5

Example of the serial adder

- $A = a_{n-1}\, a_{n-2} \ldots a_0$
- $B = b_{n-1}\, b_{n-2} \ldots b_0$
- $A = s_{n-1}\, s_{n-2} \ldots s_0 = A + B$

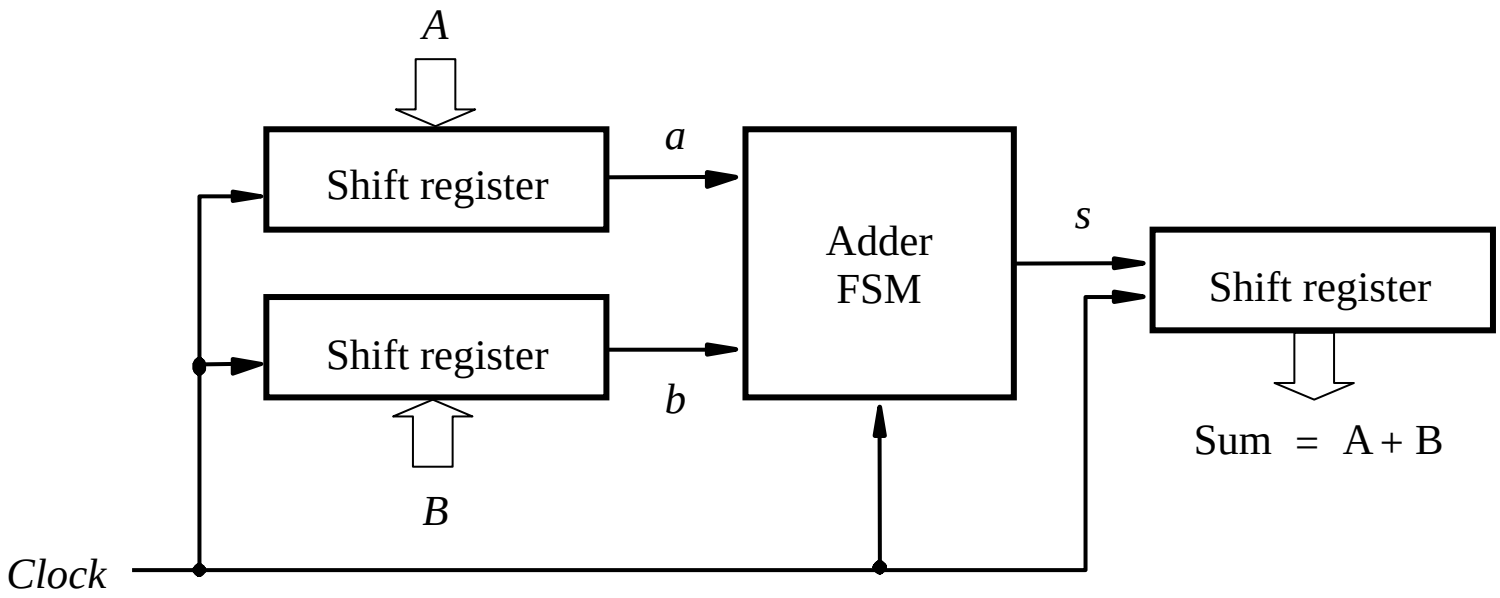


Figure 8.39. Block diagram for the serial adder.

State diagram for the serial adder FSM

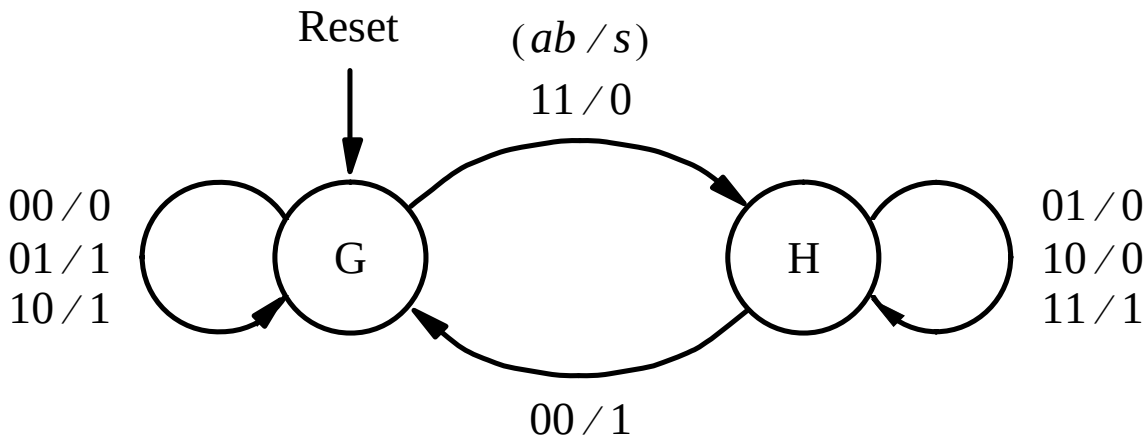
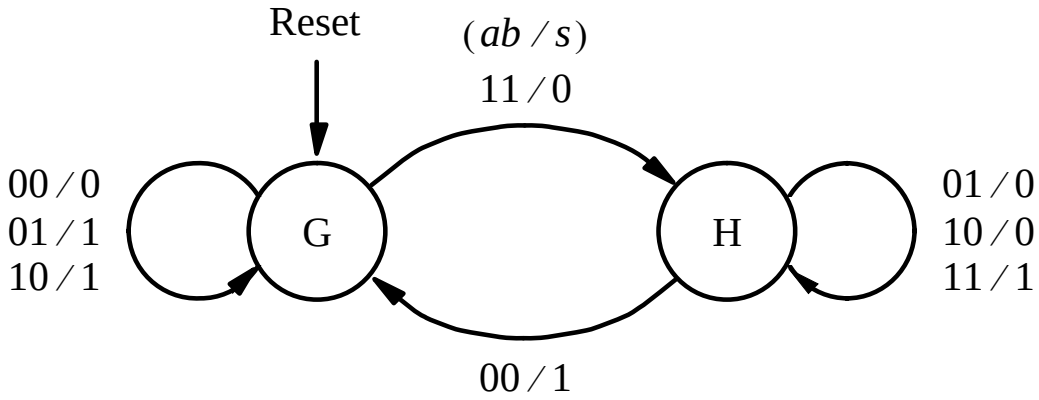


Figure 8.40. State diagram for the serial adder FSM.

State table for the serial adder FSM



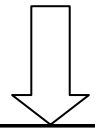
G: carry-in = 0
H: carry-in = 1

Present state	Next state				Output *s*			
	ab =00	01	10	11	00	01	10	11
G	G	G	G	H	0	1	1	0
H	G	H	H	H	1	0	0	1

Figure 8.41. State table for the serial adder FSM.

State-assigned table for the serial adder

Present state	Next state				Output *s*			
	ab =00	01	10	11	00	01	10	11
G	G	G	G	H	0	1	1	0
H	G	H	H	H	1	0	0	1



Present state	Next state				Output			
	ab =00	01	10	11	00	01	10	11
y	*Y*				*s*			
0	0	0	0	1	0	1	1	0
1	0	1	1	1	1	0	0	1

Figure 8.42. State-assigned table for Figure 8.41.

Circuit for the serial adder

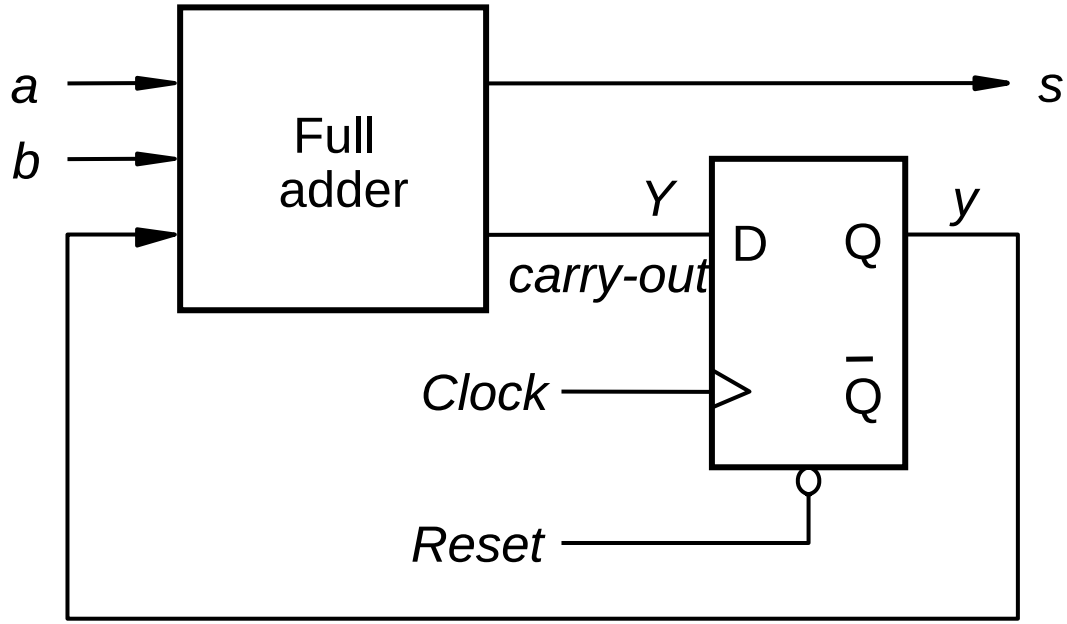


Figure 8.43. Circuit for the adder FSM in Figure 8.39.

State diagram for the serial adder (Moore-type)

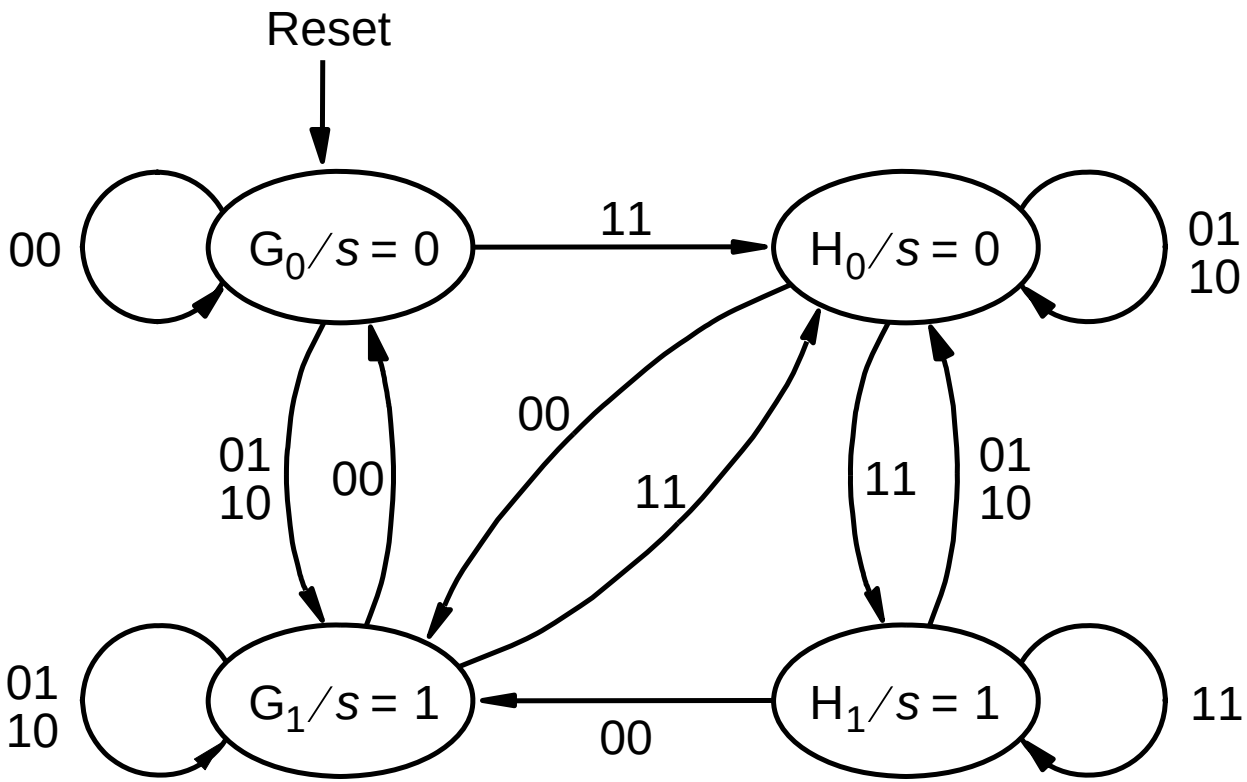
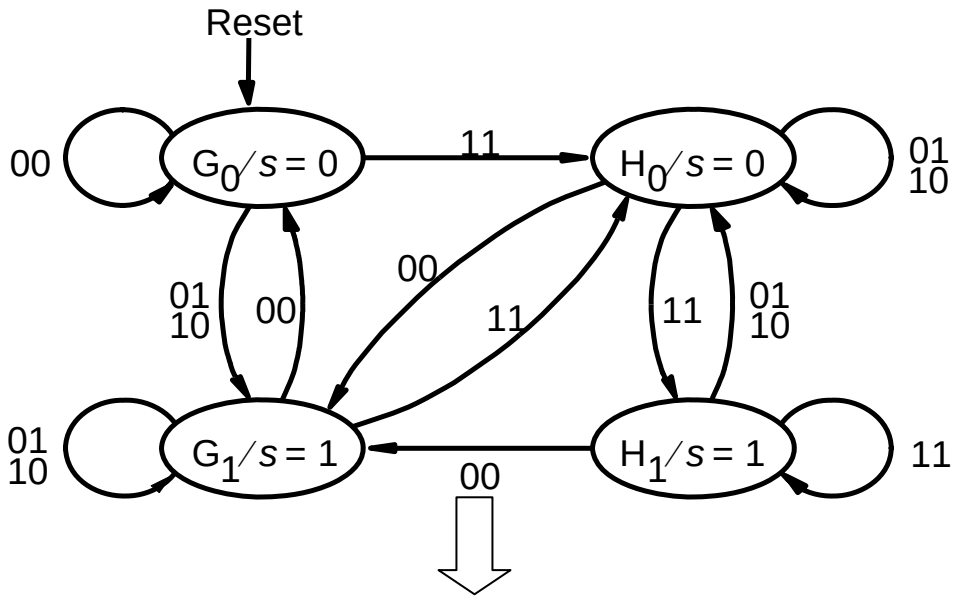


Figure 8.44. State diagram for the Moore-type serial adder FSM.

State table for the Moore-type serial adder

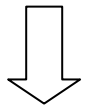


Present state	Nextstate				Output
	ab =00	01	10	11	*s*
G_0	G_0	G_1	G_1	H_0	0
G_1	G_0	G_1	G_1	H_0	1
H_0	G_1	H_0	H_0	H_1	0
H_1	G_1	H_0	H_0	H_1	1

Figure 8.45. State table for the Moore-type serial adder FSM.

State-assigned table serial adder

Present state	Nextstate				Output
	ab =00	01	10	11	*s*
G_0	G_0	G_1	G_1	H_0	0
G_1	G_0	G_1	G_1	H_0	1
H_0	G_1	H_0	H_0	H_1	0
H_1	G_1	H_0	H_0	H_1	1



Present state y_2y_1	Nextstate				Output
	ab =00	01	10	11	*s*
	Y_2Y_1				
00	0 0	01	0 1	10	0
01	0 0	01	0 1	10	1
10	0 1	10	1 0	11	0
11	0 1	10	1 0	11	1

Figure 8.46. State-assigned table for Figure 8.45.

Circuit for the Moore-type serial adder FSM

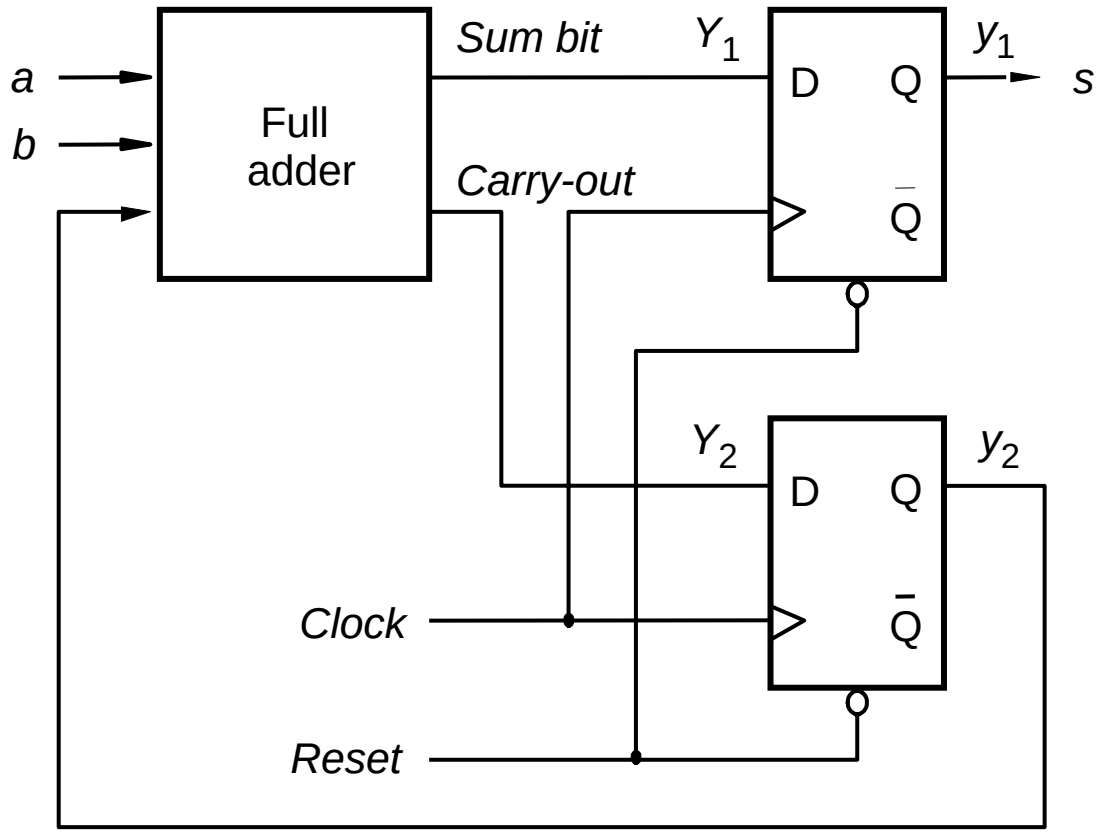


Figure 8.47. Circuit for the Moore-type serial adder FSM.