ECEN 248 – Introduction to Digital Systems Design (Spring 2008) (Sections: 501, 502, 503, 507)

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Chapter 3 Implementation Technology

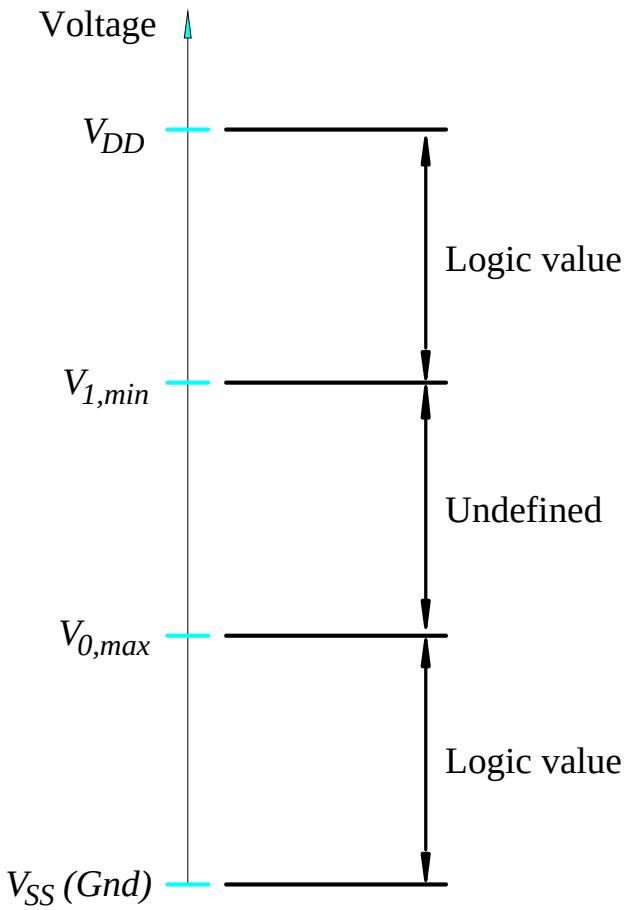
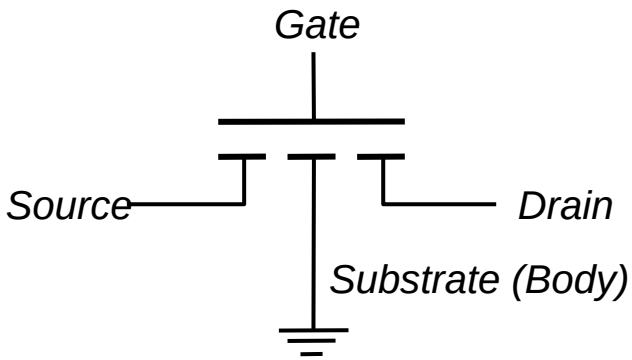


Figure 3.1. Logic values as voltage levels.

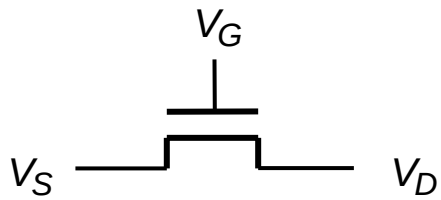
3.1 Transistor Switches

- Most popular type of transistor: Metal Oxide Semiconductor Field-Effect Transistor (MOSFET)
- Two different types of MOSFETs:
  - 1) N-channel => NMOS transistors
  - 2) P-channel => PMOS transistors
- Fig. 3.2b is the symbol of NMOS transistor which has 4 electronic terminals:
  - 1) source; 2) drain; 3) gate; 4) substrate (GND or Body)
- Fig. 3.2c is the simplified symbol of NMOS transistor which the GND connection is omitted where
  - 1) V_S is source terminal; 2) V_G is gate terminal; 3) V_D

(a) A simple switch controlled by the input *x*



(b) NMOS transistor



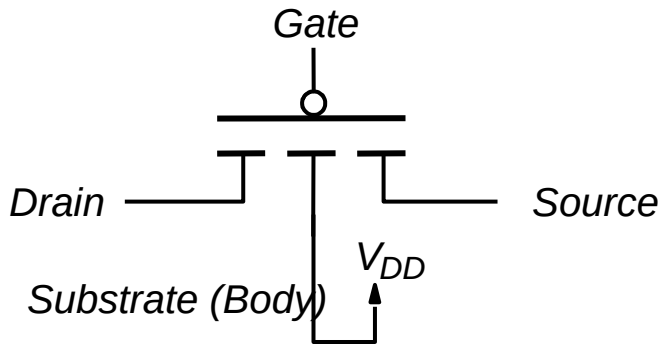
(c) Simplified symbol for an NMOS transistor

Figure 3.2. NMOS transistor as a switch.

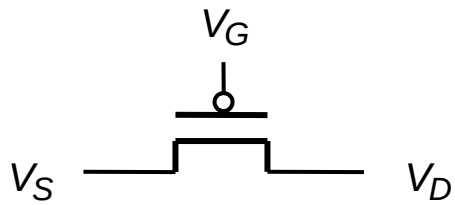
The PMOS Transistors

- PMOS transistors have the opposite behavior of NMOS transistors
- Fig. 3.3a is its logic symbol of PMOS transistor as a logic switch which is "open" if x="high", "close if x= "low".
- Fig. 3.3b is the symbol of PMOS transistor with the substrate terminal always connected to V_{DD}
- Fig. 3.3c is the simplified symbol of PMOS transistor where if VG = "high", PMOS transistor is turned off; if VG = "low", PMOS transistor is turned on – as a switch being closed.

(a) A switch with the opposite behavior of Figure 3.2*a*



(b) PMOS transistor



(c) Simplified symbol for a PMOS transistor

Figure 3.3. PMOS transistor as a switch.

NMOS & PMOS Transistor switch functions/symbols Summary:

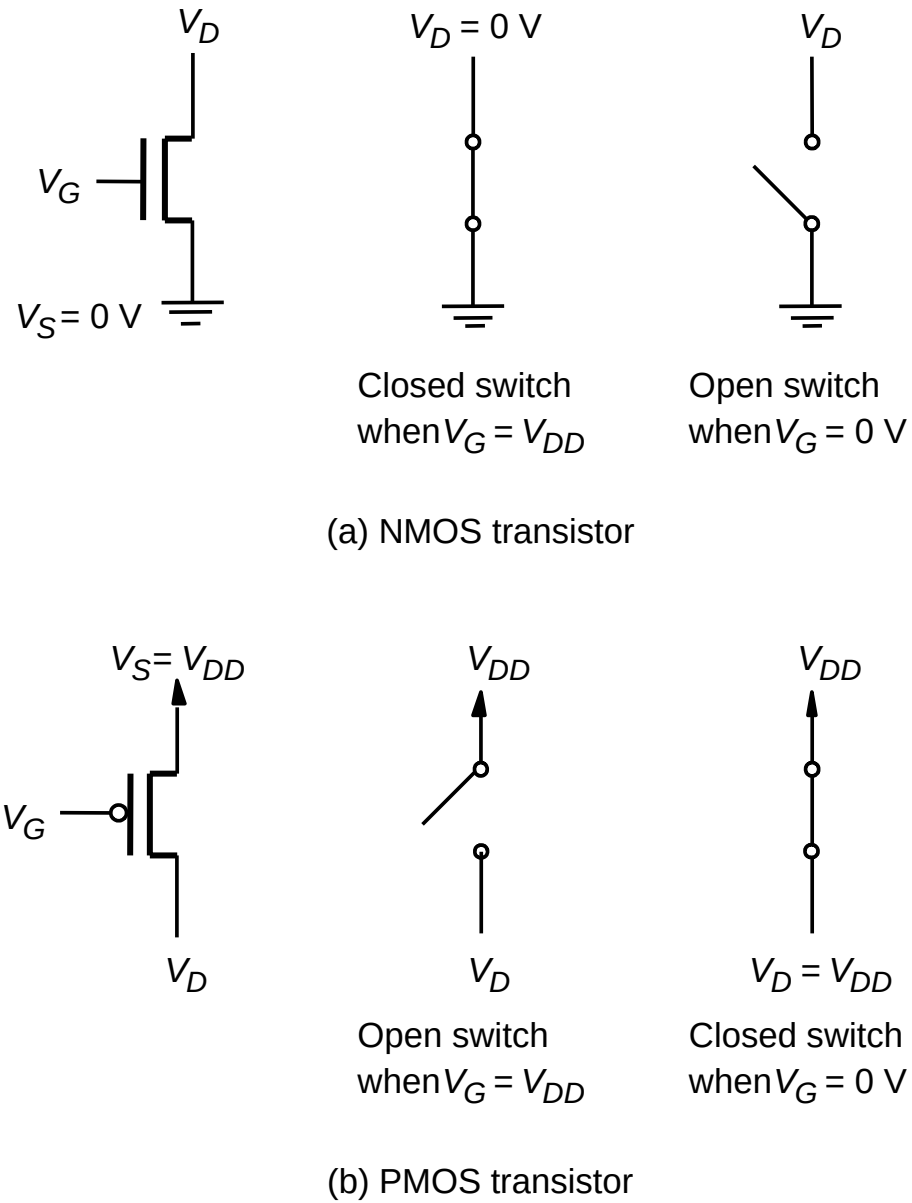
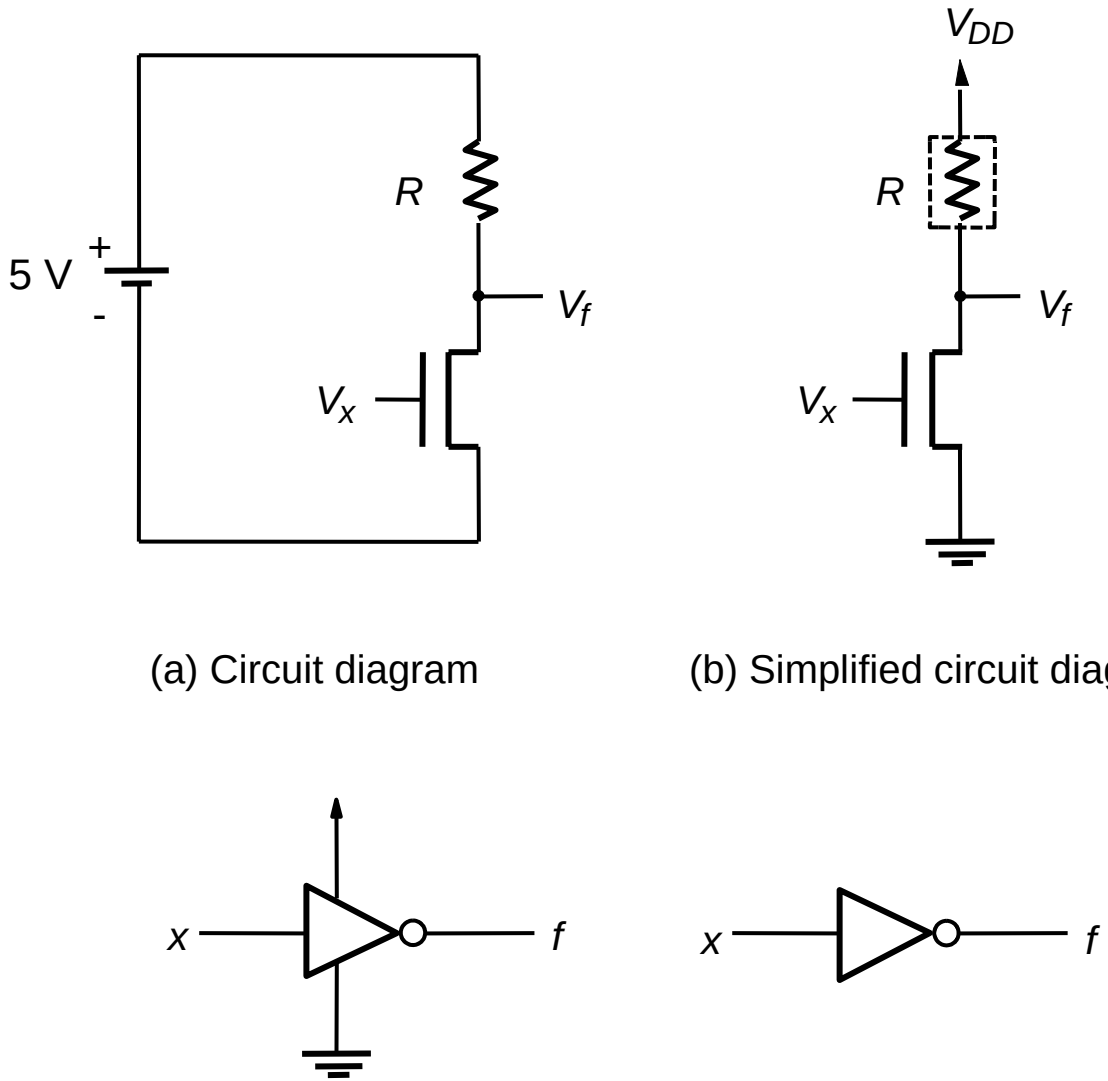


Figure 3.4. NMOS and PMOS transistors in logic circuits.

3.2 Logic Gates/Circuits Built on NMOS and PMOS Transistors

- First, we mainly focus on how to implement logic gates/circuits by using NMOS transistors – called NMOS gates/circuits?
- Then, we concentrate on how to implement logic gates/circuits by combining NMOS and PMOS transistors – called Complementary MOS or CMOS gates/circuits, which are presently most popular technology widely used.

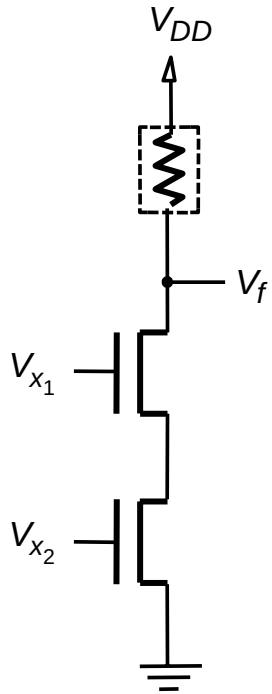


(a) Circuit diagram

(b) Simplified circuit diagram

(c) Graphical symbols

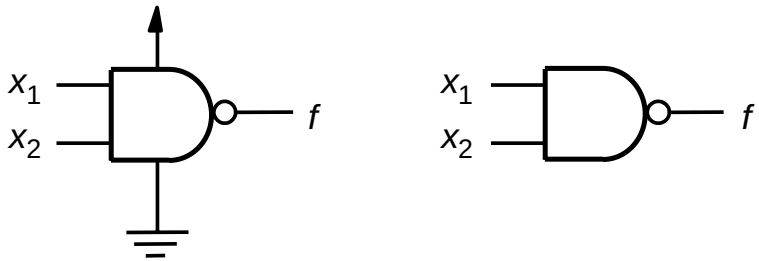
Figure 3.5. A NOT gate built using NMOS technology.



(a) Circuit

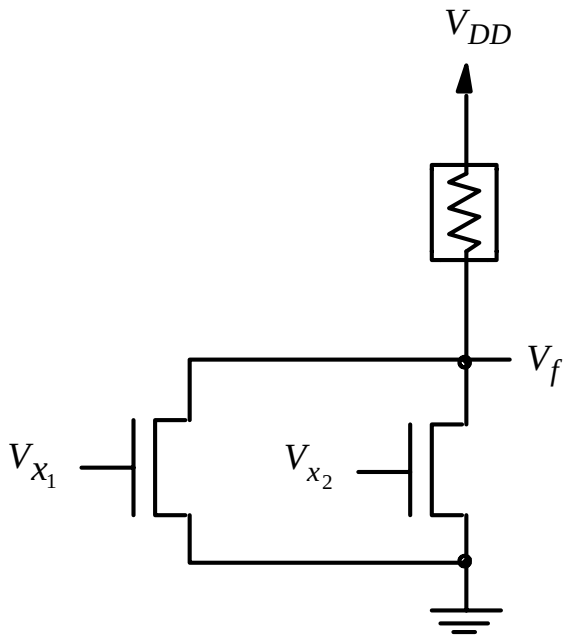
x_1	x_2	f
0	0	1
0	1	1
1	0	1
1	1	0

(b) Truth table



(c) Graphical symbols

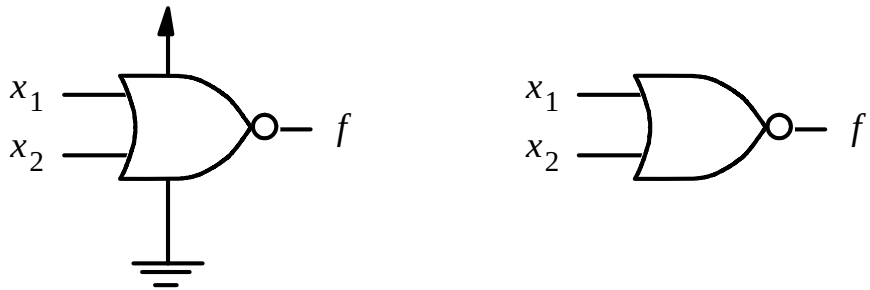
Figure 3.6. NMOS realization of a NAND gate.



(a) Circuit

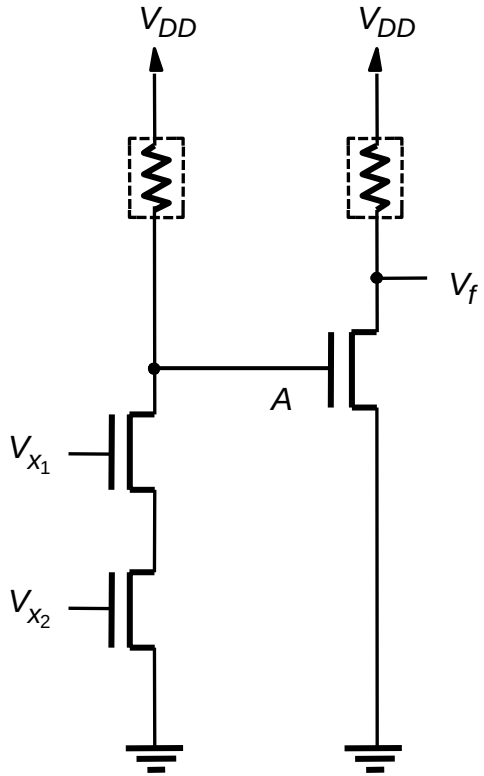
x_1	x_2	f
0	0	1
0	1	0
1	0	0
1	1	0

(b) Truth table



(c) Graphical symbols

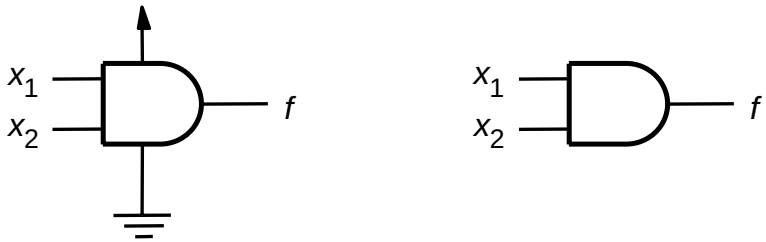
Figure 3.7. NMOS realization of a NOR gate.



(a) Circuit

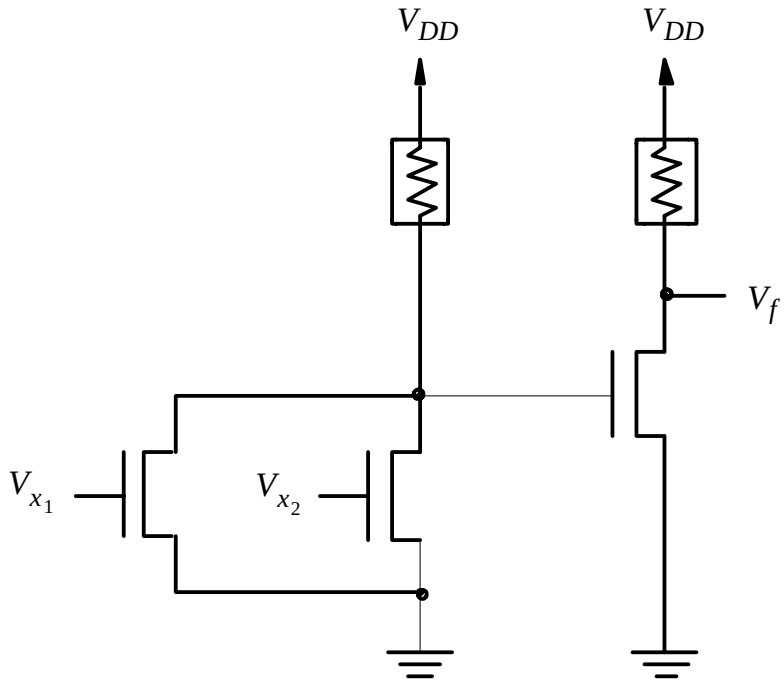
x_1	x_2	f
0	0	0
0	1	0
1	0	0
1	1	1

(b) Truth table



(c) Graphical symbols

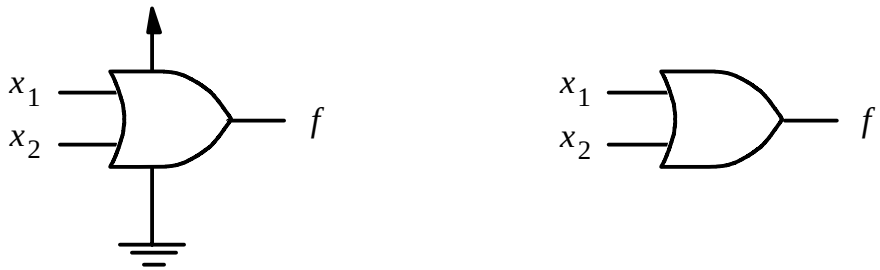
Figure 3.8. NMOS realization of an AND gate.



(a) Circuit

x_1	x_2	f
0	0	0
0	1	1
1	0	1
1	1	1

(b) Truth table



(c) Graphical symbols

Figure 3.9. NMOS realization of an OR gate.

3.3 Logic Gates/Circuits Built on CMOS Transistors

- The logic gates/circuits by combining NMOS and PMOS transistors – called Complementary MOS or CMOS gates/circuits offer some practical implementation advantages over NMOS technology as discussed in Section 3.8.
- In NMOS circuits, the logic functions realized by NMOS transistors combined with a pull-up resistor. We call part of the circuit involving NMOS transistors as the "pull-down network (PDN)". All NMOS based circuits structures, as shown in Fig 3.5~Fig. 3.8 can be characterized by a block diagram as shown in Fig. 3.10.
- The concept of CMOS circuit is based on the replacing the pull-up device/resistor with a "pull-up network (PUN" that is built using PMOS transistors, such that the functions realized by the PDN and PUN networks are complementary as indicated in Fig. 3.11.
- The PDN & PUN have equal number of transistors, which are arranged so that the two networks are "duals" of one another. Whenever the PDN has NMOS transistors connected in series, the PUN has PMOS transistors connected in parallel, and vice versa.

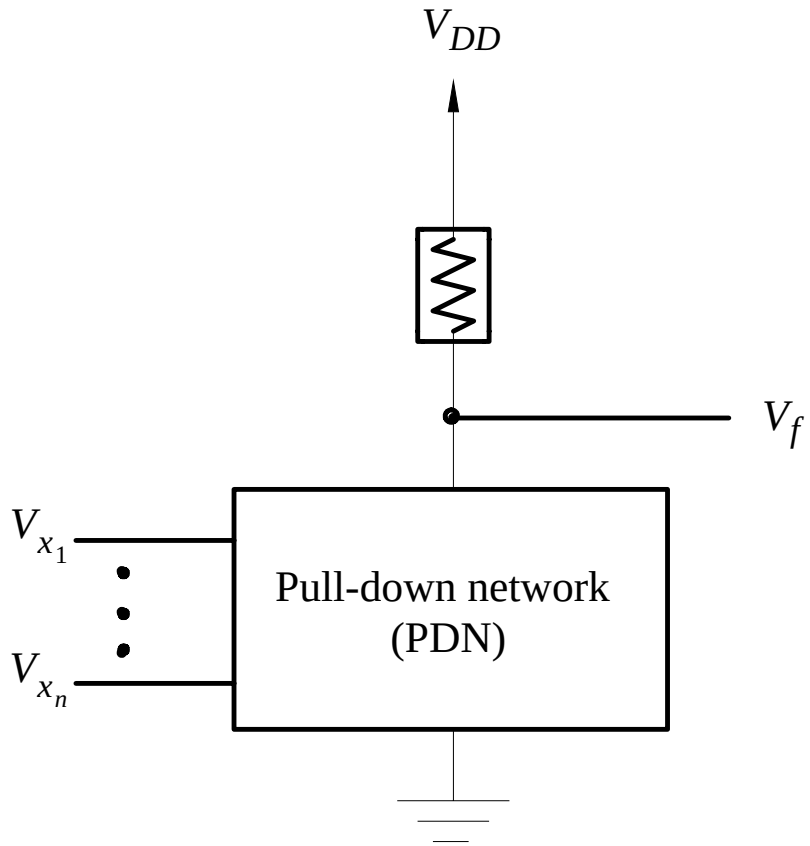


Figure 3.10. Structure of an NMOS circuit.

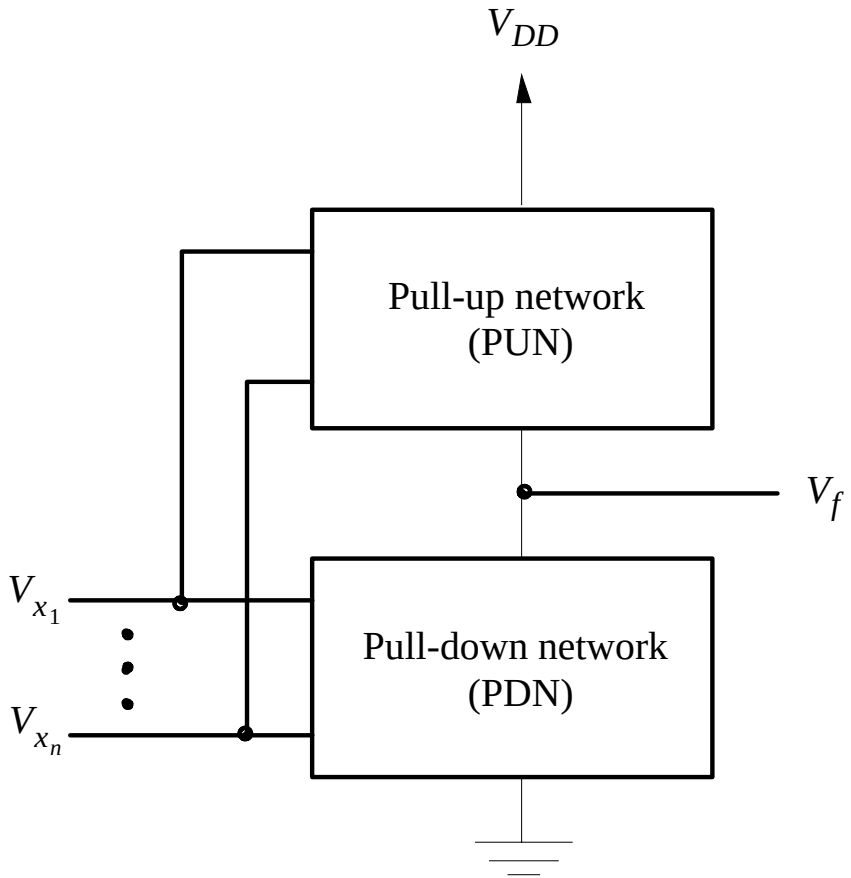
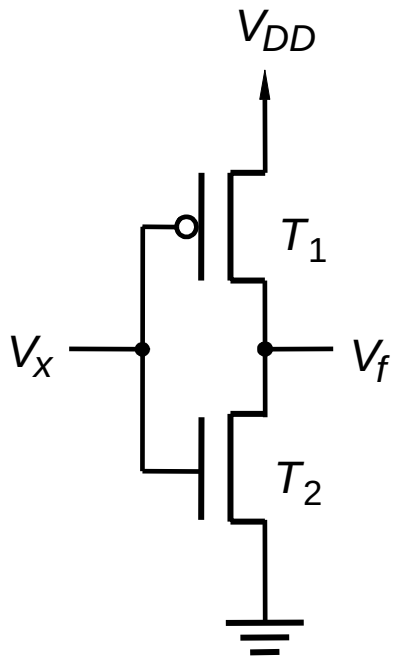


Figure 3.11. Structure of a CMOS circuit.

3.3 Basic Logic Gates/Circuits Built on CMOS Transistors and Their Implementation Cost Parameter

- Basic CMOS based NOT gates, NAND gates, NOR gates, and ANG gates with 1 or 2 inputs
- How to implement logic gates/circuits with more than 2 inputs by using CMOS transistors?
- *The number of transistors* required to build up the gate/circuit with specified functions is the key parameter for implementation expense using the CMOS based logic gates/circuits.

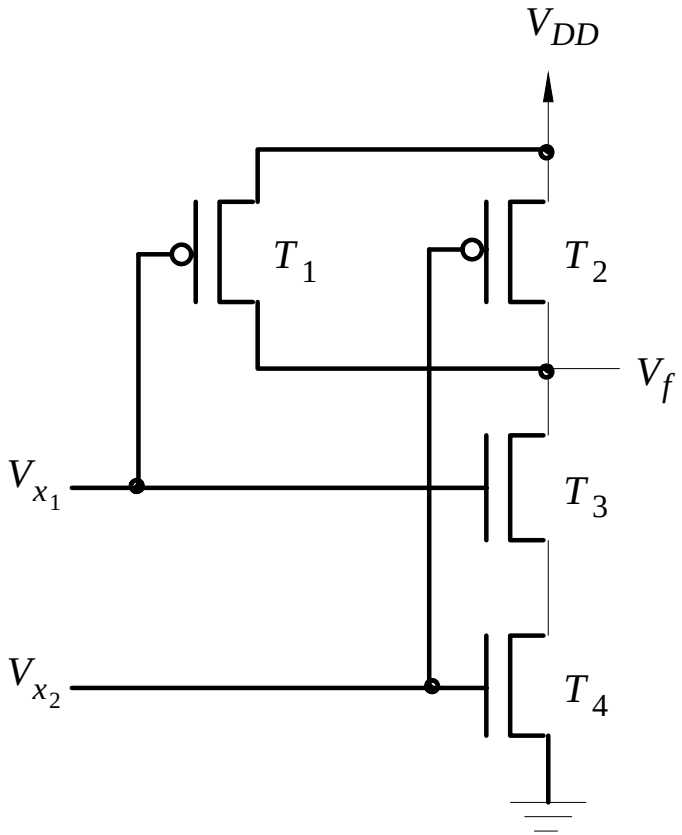


(a) Circuit

x	T_1	T_2	f
0	on	off	1
1	off	on	0

(b) Truth table and transistor states

Figure 3.12. CMOS realization of a NOT gate.

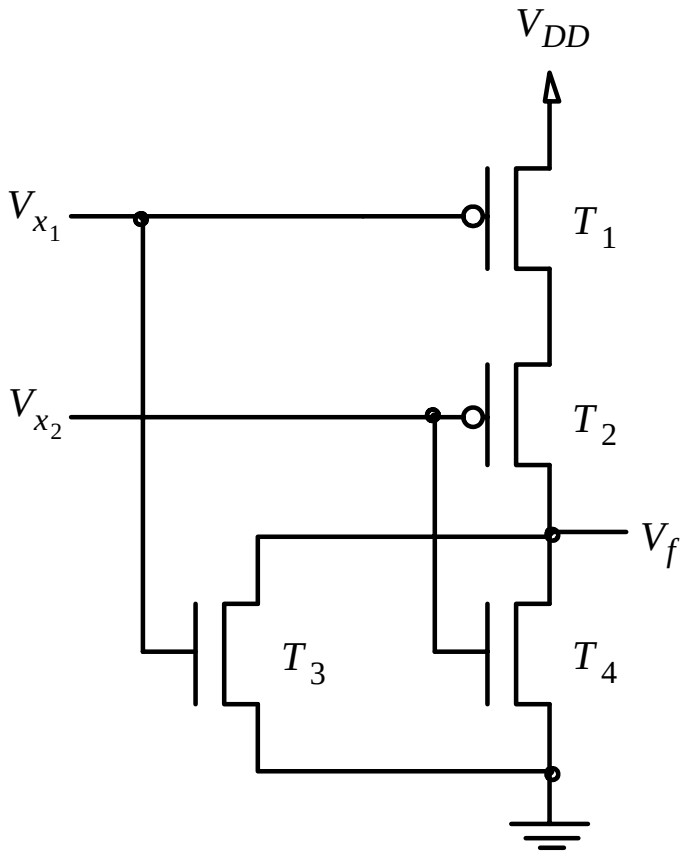


(a) Circuit

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	0

(b) Truth table and transistor states

Figure 3.13. CMOS realization of a NAND gate.



(a) Circuit

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	0
1	0	off	on	on	off	0
1	1	off	off	on	on	0

(b) Truth table and transistor states

Figure 3.14. CMOS realization of a NOR gate.

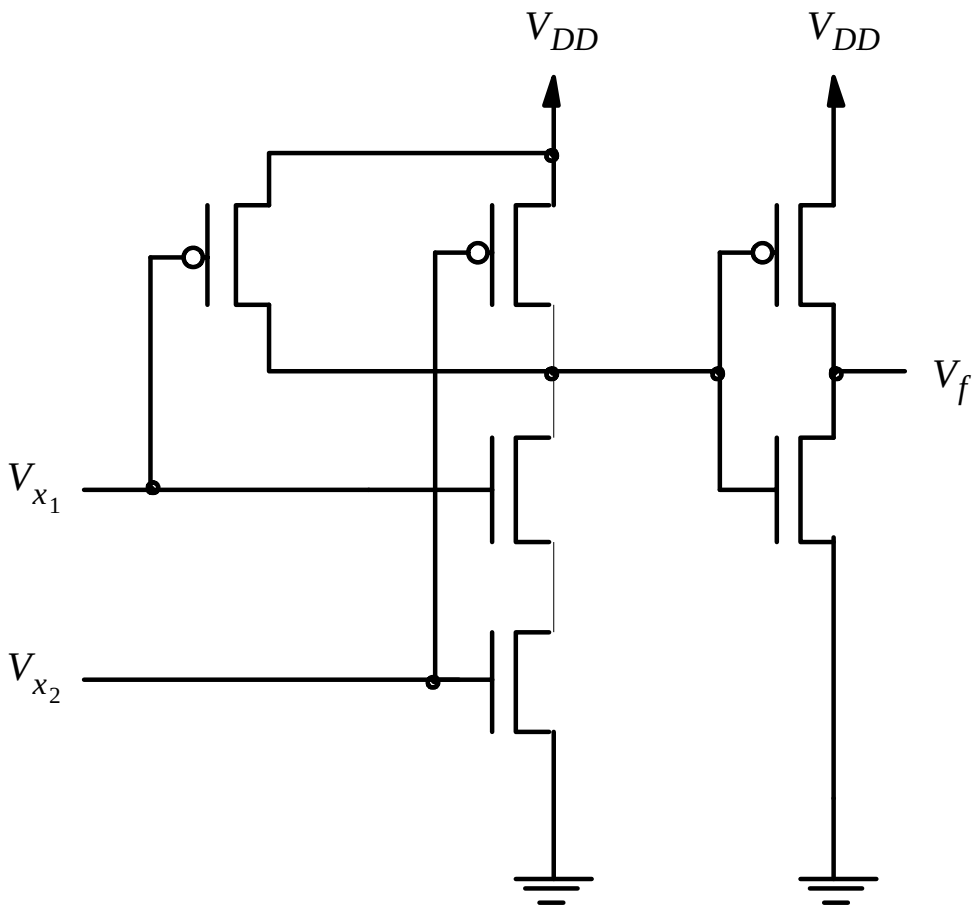


Figure 3.15. CMOS realization of an AND gate using a NAND gate and a NOT gate.