# A Single-supply True Voltage Level Shifter

Rajesh Garg Gagandeep Mallarapu Sunil P Khatri

(rajeshgarg_at_tamu.edu) (gagandeepm_at_tamu.edu) (sunilkhatri_at_tamu.edu)
Department of Electrical & Computer Engineering, Texas A&M University, College Station TX 77843.

## Abstract

*When a signal traverses on-chip voltage domains, a level shifter is required. Inverters can handle a high to low voltage shift with minimal leakage. For a low to high voltage level translation, inverters tend to consume a large amount of leakage power, and hence special circuits have been proposed for this type of translation. This paper reports a novel single-supply "true" (in the sense that it can handle a low to high, or high to low voltage level conversion) voltage level shifter, which can handle low-to-high and high-to-low voltage translation. Such a requirement arises in many modern ICs or Systems-on-Chip (SoCs). The use of single supply voltage reduces circuit complexity by eliminating the need for routing both supply voltages. The proposed circuit was extensively simulated in a 90nm technology using SPICE. Simulation results demonstrate that the level shifter is able to perform voltage level shifting with low leakage for both low to high, as well as high to low voltage level translation. We have validated the correct operation of the proposed level shifter under process and temperature variations as well.*

## 1 Introduction

System-on-chip (SoC) solutions and multi-core computing architectures are becoming increasingly common for many applications. For such computing paradigms, energy and power minimization is a crucial design goal. Both the dynamic and the leakage power consumption of a CMOS circuit depend upon the supply voltage, and they decrease at lease quadratically with decreasing supply voltages. Therefore, in recent times, it is common to decrease the supply voltage value in the non-critical parts of SoCs and multi-core processors, in order to reduce the power and energy consumption. This results in a situation where there are many blocks in an SoC design which operate at different supply voltage levels, in order to minimize system power and energy values [1, 2]. Similarly, multi-core processors have different cores operating at different supply voltage values, depending on computational demand. Moreover, these different blocks/cores may employ dynamic voltage scaling (DVS) to meet the variable speed/power requirements at different times [3, 4, 5]. As a consequence, *many voltage domains are formed on a single IC or SoC*. These voltage domains may operate at different supply voltage values at different times of the computation. Therefore, the voltage level shifters (VLS) required to interface these different voltage domains should be able to efficiently convert any voltage level to any other desired voltage level, since the voltage of the input to the VLS can in general be either greater than or less than the voltage of the output. This is especially true in complex ICs and SoCs. These complex designs use aggressive DVS for power minimization, and hence the voltage of different voltage domains can have an arbitrary relationship.

Conventional voltage level shifters (CVLS), as shown in Figure 1, require two voltage supplies, the input domain voltage supply (VDDI) and the output domain voltage supply (VDDO). The operation of circuit is as follows. When the input signal $in$ is at the VDDI value ($inb$ is at GND value), MN1 turns ON (MN2 is off). Thus pulls the $outb$ signal to GND. This transition of $outb$ signal turns on MP2 which pulls up the $out$ signal to the VDDO value. When $in$ is at GND ($inb$ is at VDDI value), MN1 is off and MN2 is on, which turns on MP1. MP1 pulls up the $outb$ to the VDDO value. Although there are no high leakage paths from VDDO to GND in this circuit, two supply voltages are required for the voltage level conversion. This can be a hard requirement to satisfy, especially if the VDDO and VDDI domains are separated by a large distance. The supply voltage wires typically need to be quite wide (especially if VDDO and VDDI are physically far apart), resulting in a large area penalty. Figure 2 shows a multi voltage system where four modules are interacting with each other using CVLS. A voltage level conversion at the input of a particular voltage domain will require all the supply voltages of signals coming to this voltage domain from other voltage domains whose voltage level is lower than its own voltage level. This may result in routing congestion, excessive area utilization and also may pose restrictions on module placement. From the schematic diagram of the CVLS shown in Figure 1, we can observe that the routing of additional supply voltages can be avoided by sending a signal (which is going to a different voltage domain) in both polarities (i.e. $in$ and $inb$). However, this strategy would require one additional wire per signal and hence could lead to routing congestion. This problem is further aggravated by the increasing number of voltage domains in SoCs and multi-core architectures. Additional complexity is encountered if the voltage domains have *variable* voltages, which requires a domain to receive the supply voltages of *every other* domain. In such a scenario, it is not known apriori whether VDDI $<$ VDDO or VDDI $>$ VDDO. Therefore, a single supply voltage level shifter (SS-VLS), is desired which utilizes the supply voltage of the VDDO domain alone. This would help ease placement and as well as routing constraints enabling efficient physical design of the IC. This would also help in reducing the number of input and output pins of a block. Figure 3 shows a multi-voltage system, where four modules interact with each other using SS-VLS.



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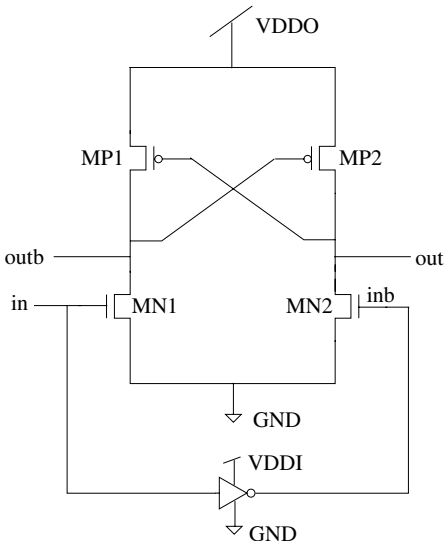


**Figure 1. Conventional voltage level shifter**

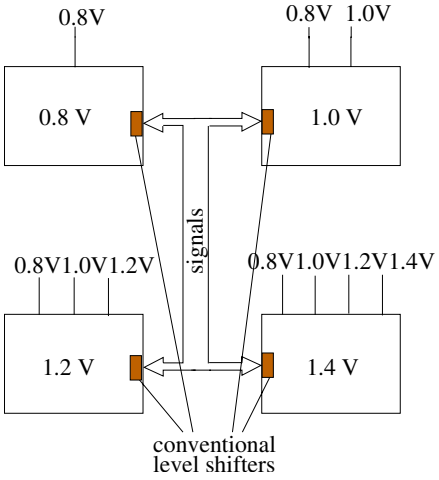


**Figure 2. Multi-voltage system using CVLS**

Suppose we know apriori that VDDI > VDDO. In this case, an inverter is the best level shifter. However, if VDDI < VDDO, the inverter cannot be used, due to the high leakage currents that result in such a conversion. For such a scenario, the best known previous approach [6] yields low leakage currents. In practice, it may not be possible to know apriori if VDDI > VDDO or VDDI < VDDO, as discussed earlier. Our single supply true voltage level shifter (SS-TVLS) allows voltage level shifting in both the above cases. This solution is referred to as "true" in the sense that the same circuit works for both VDDI < VDDO as well as VDDI > VDDO. The use of a single supply voltage reduces layout congestion by eliminating the need for routing both supply voltages. The proposed circuit was simulated using 90nm PTM [7] model cards in SPICE [8]. The simulation results demonstrate that our level shifter is able to shift the input signal from 0.8V to 1.2V and from 1.2V to 0.8V with very low leakage currents (20.8nA and 7.3nA for a high output respectively, and 3.6nA and 3.9nA for a low output respectively) with low delays (22.0ps and 34.9ps respectively for a rising transition, and 33.3ps and 15.7ps respectively for a falling transition). The competing approach to the SS-TVLS is to use an inverter along with the non-true SS-VLS solution of [6], and disable either the inverter or the SS-VLS of [6] depending on whether VDDI < VDDO or VDDI > VDD0 respectively. The leakage currents of combination of an inverter and the solution of [6] are 157.2nA and 32.5nA respectively (for a high output value) and 71.1nA and 36.3nA respectively (for a low output value), with a delay of 122.6ps and 46.5ps respectively (for a rising output), and 50.5ps and 35.2ps respectively (for a falling output). Moreover, the combination of an inverter and the circuit of [6] also require a control signal which indicates if VDDI < VDDO, which is not required for our SS-TVLS approach.

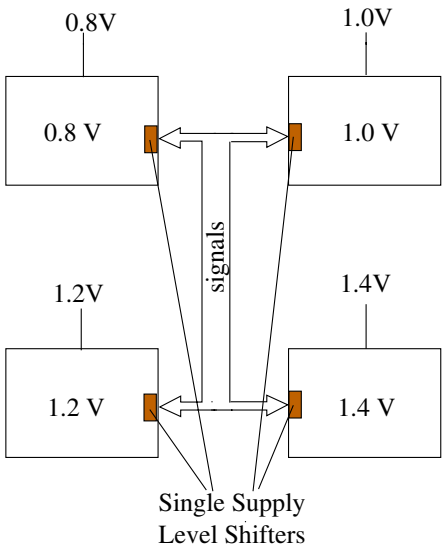


**Figure 3. Multi-voltage system using SS-VLS**

The rest of the paper is organized as follows. Section 2 discusses some previous work in this area. In Section 3 we describe our SS-TVLS design. In Section 4 we present experimental results which demonstrate that SS-TVLS outperforms the best known previous approach. Finally, conclusions are presented in Section 5.

## 2 Previous Work

Several kinds of voltage level shifters have been proposed over the years, to minimize power consumption [9, 10, 11, 12]. Most of these approaches utilize dual supply voltages, which make them unattractive for SoCs and multi-core architectures for reasons already discussed. The work of [9] focused on using bootstrapped gate drive to minimize voltage swings. This helps in reducing the switching power consumption in the conventional level shifter and also helps to increase the speed of the level shifter. In [10], the authors proposed a method of incorporating voltage level conversion into regular CMOS gates by using a second threshold voltage. They proposed a scheme to modify the threshold voltage of the high voltage gates (which are driven by outputs of low voltage gates) to obtain the level shifting operation along with the logic operation. This attempt focused on reducing power by using dual supply voltages. In [11], Wang et. al. proposed a level up-shifter along with a level down-shifter to interface 1.0V and 3.3V voltage domains. The level up-shifters use zero-$V_t$ thick oxide NMOS devices to clamp the voltage, hence protecting the gate oxide of the 1V NMOS switches. The level down-shifter used thick oxide NMOS devices with 1V supplies as both pull-up and pull-down

devices. This approach also requires dual supply voltages. In [12], the authors presented a low to high voltage level shifter for use in a VLSI chip for MEMS applications. The design uses a stack of devices in series between the rail voltages, biased by 5 different bias voltages for the conversion.

The SS-VLS proposed in [13] uses a diode-connected NMOS device between the supply and output to convert a low level to a high voltage level. There is a threshold voltage drop in this diode-connected NMOS device, which reduces the supply voltage to the input inverter. This level shifter has a limited range of operation and suffers from higher leakage currents when the difference in voltage levels of the output supply and the input signal is more than a threshold voltage. In [6], the authors have presented a SS-VLS design which tries to address the issues associated with the design of [13]. However, their SS-VLS is only able to convert a low voltage domain signal to a higher voltage domain (VDDI $<$ VDDO). Also, the leakage currents in the SS-VLS are relatively high. In contrast to these SS-VLS implementations, the SS-TVLS proposed in this paper can convert *any* voltage level to any other desired voltage level (i.e. it is a "true" voltage shifter) *without using any control signals*. At the same time, the leakage currents of the proposed SS-TVLS design are very low.

## 3 Our Approach

In SoCs and multi-core processors, we need a VLS to interface different voltage domains. As the supply voltage of these voltage domains are not known beforehand (this occurs due to the use of DVS), there is a need for voltage level shifters which can convert any voltage level to any other desired voltage level (VDDI $<$ VDDO as well as VDDI $>$ VDDO). The SS-TVLS proposed in this paper can perform this task as described below.

The schematic diagram of the proposed voltage level shifter (i.e. SS-TVLS) is shown in Figure 4. Note that devices with thick channel lines are high-$V_T$ devices. Their $V_T$ is 0.49V for NMOS and -0.44V for PMOS, while the nominal $V_T$ is 0.39V for NMOS and -0.34V for PMOS. Also note that the NOR gate is Figures 4 uses the VDDO supply. The sizes (width/length) of all devices (in $\mu m$) are also shown in the same figure. Note that all PMOS devices in this figure have substrate connected to VDD0. The operation of SS-TVLS can be explained by considering two scenarios. The timing diagram of our SS-TVLS is shown in Figure 5 and it is applicable to both scenarios. In the first scenario, VDDO $>$ VDDI (i.e. the VLS has to convert a low voltage level to a high voltage level). In this case, when the input signal $in$ goes high to the VDDI value, the output node $outb$ starts falling due to the NOR gate. However, the PMOS transistor of the NOR gate whose gate terminal is driven by $in$ is not in complete cut-off region (i.e. it is leaking) because VDDI $<$ VDDO. Thus there is temporary leakage path between VDDO and GND which will be eliminated by the rising of $node2$ (the second input of NOR) to the VDDO value. After the input signal $in$ goes high, M6 turns on and thus pulls down $node1$ to GND. This causes M3 to turn on and hence the $node2$ input node of the NOR gate is pulled to the VDDO value and the output node $outb$ is pulled down to GND, and hence the previously mentioned leakage path between VDDO and GND is removed. During this phase, as $in$ is high and it is at VDDI ($<$ VDDO), M8 is ON along with M2, which results in the charging of the $ctrl$ node (whose capacitance is dominated by the gate capacitance of MC) to a value which is the minimum of VDDI and VDDO-$V_T^{M8}$ (where $V_T^{M8}$ is the threshold voltage of M8). Note that M1, M4, M5 and M7 are turned off when $in$ is at the logic high value.

Now when the $in$ node falls, M6 turns off while M1 turns on (because the gate to source voltage of M1 is more than $V_T^{M1}$). This leads to the discharge of $node2$ (and the charging of $node1$) and thus the NOR output rises to VDDO (since both inputs of NOR are at the GND value). In this phase, M3, M2, M6 and M7 are turned off while M4 and M5 are turned on. The $ctrl$ node discharges through M2 and M8 during the time when M2 is turning off. The node capacitance of $ctrl$ (implemented as the gate capacitance of MC) is selected to be large enough to allow the discharge of $node2$. Note that the NOR gate allows us to balance the rising and the falling delays of the SS-TVLS. It also provides, the SS-TVLS the same load driving capability as a minimum size inverter. Note that the SS-TVLS is an inverting voltage level shifter. An extra inverter is not required at the output of the inverting voltage level shifter because this polarity inversion can be subsumed in the logic of the VDDO voltage domain. In our experiments, the method used for comparison has the same inverting property.

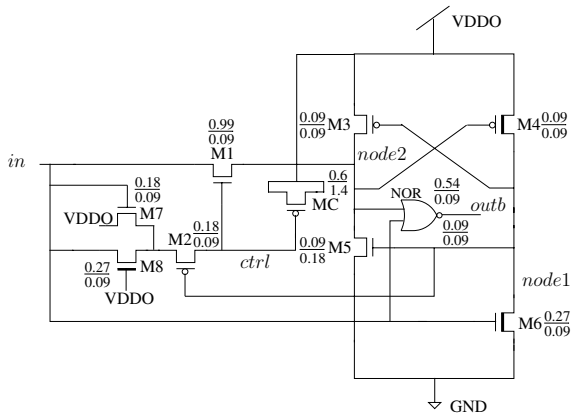


**Figure 4. Novel single supply true voltage level shifter**

In the second scenario, the SS-TVLS performs the conversion of a high voltage level to a low voltage level (i.e. VDDO $<$ VDDI). In this scenario as well, when the input $in$ goes high to the VDDI value then the output node $outb$ falls to the GND value. In this scenario, as VDDI $>$ VDDO, the PMOS transistor of the NOR whose gate terminal is driven by $in$ is in deep cut-off and hence, there is no leakage path between VDDO and GND. After $in$ goes high to VDDI, M6 turns and pulls down its drain node. This turns on M3 which then charges $node2$ to VDDO. During this phase, as VDDI $>$ VDDO therefore, M7 is ON and M2 is also ON. M8 is off in this case. Thus, the $ctrl$ node voltage charges to a value $min$(VDDO, VDDI-$V_T^{M7}$). Here $V_T^{M7}$ is the threshold voltage of M7. Note that M1, M4 and M5 are turned off when $in$ is at VDDI. The rest of the operation of the SS-TVLS when $in$ transitions to GND is identical to the first scenario. Note that the SS-TVLS works for VDDI $>$ VDDO as well as VDDI $<$ VDDO because M1 never turns on when $in$ is logically high (regardless of whether VDDI $>$ VDDO or VDDI $<$ VDDO).

The SS-TVLS exhibits very low leakage currents as compared with the best known voltage level shifter [6] for VDDI $<$ VDDO. There are several reasons for this. Note that the devices M4 and M6 are high $V_T$ devices, to reduce leakage currents. Also, all the devices of the proposed SS-TVLS were carefully sized to re-

duce leakage current while considering the tradeoff between speed and leakage power. As mentioned before, the maximum voltage value that the $ctrl$ node can charge to is the minimum of VDDI and VDDO-$V_T^{M8}$ when VDDI $<$ VDDO, and VDDO and VDDI-$V_T^{M7}$ when VDDI $>$ VDDO. Thus, when the voltage values of the VDDI and VDDO domains are small and close to each other, then the $ctrl$ node charges to VDDO-$V_T^{M8}$. Therefore, a low $V_T$ NMOS device[1] is to used for M8 to ensure that $ctrl$ can charge to a sufficiently large voltage value. This also helps in increasing the voltage translation range of our SS-TVLS. Note that all other transistors (M1, M2, M3, M5, MC and M7 and NOR gate transistors) are nominal $V_T$ devices.

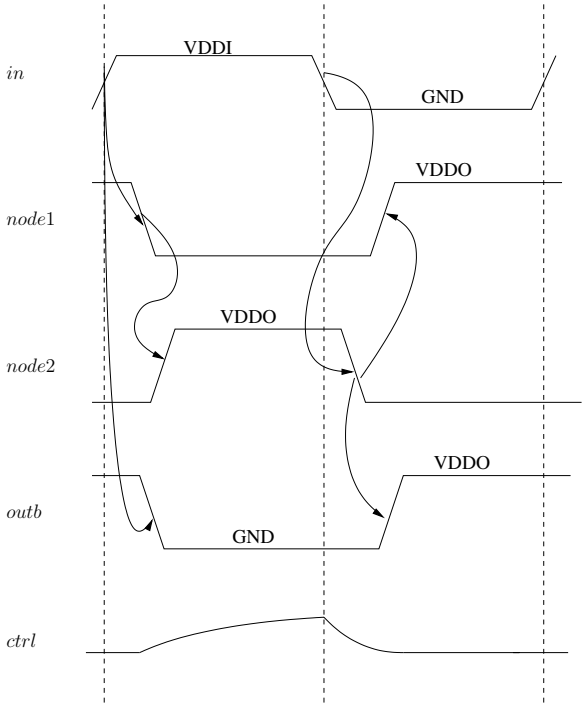


**Figure 5. Timing diagram for our SS-TVLS**

## 4 Experimental Results

We simulated the SS-TVLS proposed in this paper, using SPICE [8], with a 90nm PTM [7] model card. An inverter is the best level shifter when VDDI $>$ VDDO. However, if VDDI $<$ VDDO, the inverter cannot be used, due to the high leakage currents that result in such a conversion. For such a scenario, the best known previous approach [6] yields low leakage currents. Therefore, to compare the performance of our SS-TVLS, we also simulated a combination of an inverter and the SS-VLS of [6] as shown in Figure 6. For the SS-VLS of [6], we used the same sized devices as reported in [6]. Note that the combined VLS of Figure 6 requires a control signal which indicates whether VDDI is greater or smaller than VDDO. Both, our SS-TVLS and combined VLS are driven by same sized inverters.

Note that the delays of the SS-TVLS as well as the SS-VLS of [6] are dependent on the input sequence. The worst-case is a 0-1-0-1-0. . . sequence on the inputs. For this sequence, the voltage achieved at the $ctrl$ node when the input switches to 0, is the lowest across all sequences, resulting in a higher output rising delay. The delay numbers reported in this paper are the worst-case delays across all possible input sequences.

Table 1 reports the results obtained for voltage level shifting from 0.8V to 1.2V at a temperature of 27° C. Column 1 reports the performance parameter under consideration. Column 2 reports the results obtained for the proposed SS-TVLS. Column 3 reports the results obtained for the combined VLS of Figure 6. Note that the rising (falling) delay is defined as the delay of the rising (falling) output signal. Similarly, "Leakage Current High (Low)" in the table represents the leakage current when the output signal is at VDDO (GND) value. We observe that the SS-TVLS performs significantly better than the combined VLS in terms of delay (5.5× faster for a rising output and 1.5× faster for a falling output), power (2.6× lower for a rising output, and 3.5× lower for a falling output) and leakage (7.5× lower for a high output, and 19.5× lower for a low output).

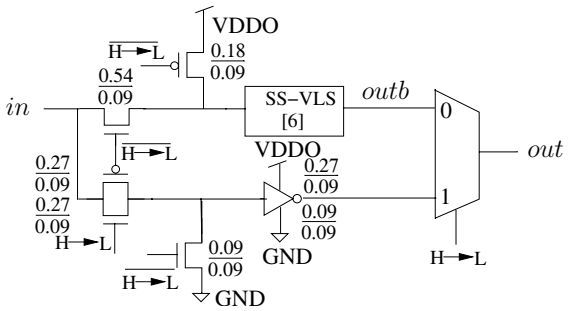


**Figure 6. Combination of an inverter and SS-VLS by Khan et. al. [6]**

| Performance Parameter | Proposed SS-TVLS | Combined VLS of Figure 6 |
|---|---|---|
| Delay Rise (ps) | 22.0 | 122.6 |
| Delay Fall (ps) | 33.3 | 50.5 |
| Power Rise ($\mu$W) | 27.6 | 71.87 |
| Power Fall ($\mu$W) | 33.8 | 119.27 |
| Leakage Current High (nA) | 20.8 | 157.2 |
| Leakage Current Low (nA) | 3.6 | 71.1 |

**Table 1. Low to High Level Shifting**

Table 2 reports the results obtained for voltage level conversion from 1.2V to 0.8V at a temperature of 27° C. Column 1 reports the performance parameter under consideration. Column 2 reports the results obtained for the proposed SS-TVLS. Column 3 reports the results obtained for the combined VLS shown in Figure 6. We observe that our proposed voltage level shifter performs very well compared to the combined VLS of Figure 6 with very low leakage currents (4.4× lower for a high output, and 9.3× lower for a low output). Also it is faster than the combined VLS (1.3× faster for a rising output and 2.2× faster for a falling output). Note that the delay of combined VLS is the summation of the delays of the transmission gate (at the input side), the multiplexer (at the output side) and the inveter. Therefore, the delay of the combined VLS is much larger than the inverter delay alone and hence, it is slower than our TVLS.

We also evaluated the functionality of our SS-TVLS under process and temperature variations. We varied the temperature, the channel width, the channel length and the threshold voltage of all

[1]This is indicated by a dark line at the gate of M8. The $V_T$ value of M8 is 0.19V.

| Performance Parameter | Proposed SS-TVLS | Combined VLS of Figure 6 |
|---|---|---|
| Rise Delay (ps) | 34.9 | 46.5 |
| Fall Delay (ps) | 15.7 | 35.2 |
| Power Rise ($\mu$W) | 27.3 | 20.7 |
| Power Fall ($\mu$W) | 59.3 | 56.8 |
| Leakage Current High (nA) | 7.3 | 32.5 |
| Leakage Current Low (nA) | 3.9 | 36.3 |

**Table 2. High to Low Level Shifting**

| Performance Parameter | Proposed SS-TVLS | | Combined VLS of Figure 6 | |
|---|---|---|---|---|
| | $\mu$ | $\sigma$ | $\mu$ | $\sigma$ |
| Delay Rise (ps) | 22.08 | 1.1 | 129.4 | 27.4 |
| Delay Fall (ps) | 33.2 | 1.9 | 50.4 | 6.0 |
| Power Rise ($\mu$W) | 27.7 | 0.8 | 78.9 | 7.3 |
| Power Fall ($\mu$W) | 33.8 | 0.4 | 114.2 | 7.2 |
| Leakage Current High (nA) | 31.5 | 13.7 | 218.8 | 158.6 |
| Leakage Current Low (nA) | 3.8 | 3.8 | 102.9 | 75.41 |

**Table 3. Process variations simulation results for Low to High Level Shifting at T=$27^\circ$ C**

devices in our SS-TVLS. The temperature of all the devices were varied together while, all other parameters were varied independently. For channel length and width the mean was taken to be equal to the nominal value and the standard deviation used was taken to be 3.34% of $l_{min}$ of the process (i.e. 90nm). For threshold voltage the mean was taken to be equal to the nominal value and the standard deviation used was taken to be 3.34% of the nominal value (so that the three times of the standard deviation is 10% of the nominal value). Three different values of temperature were used ($27^\circ$, $60^\circ$ and $90^\circ$ C). We performed 1000 Monte Carlo simulations for both cases i.e. for high to low and low to high voltage conversion. These simulations were performed at each of the three temperatures mentioned above. In all Monte Carlo simulation, our SS-TVLS was able to convert the voltage level correctly. The outputs of both designs were loaded with a fixed capacitance of 1fF.

The results obtained from the 1000 Monte Carlo simulations conducted at a temperature of $27^\circ$ C are reported in Tables 3 and 4, for a low-to-high and a high-to-low voltage level conversion. In Table 3 (Table 4), Column 1 reports the performance parameter under consideration. Columns 2 and 3 report the mean and the standard deviation of the values obtained for the proposed SS-TVLS. Columns 4 and 5 report the mean and the standard deviation for the combined VLS shown in Figure 6. From these tables, we observe that the mean delay and power are closer to their nominal values. However, the mean value of the leakage current is different from the nominal value. The standard deviation of all performance parameters i.e. delay, power and leakage current is much lower for our SS-TVLS as compared to the combined VLS of Figure 6. This demonstrates that our SS-TVLS is more tolerant to process and temperate variations than the combined VLS. The Monte Carlo simulation results for other temperatures are not reported due to space constraints. Results for these temperatures also give substantially similar results compared to Tables 3 and 4.

To evaluate the effectiveness of our SS-TVLS for SoCs and multi-core processors having multiple voltage domains with DVS, we varied VDDI and VDDO voltage values from 0.8V to 1.4V in steps of 5mV and simulated our SS-TVLS for all VDDI and VDDO combinations. Our SS-TVLS was able to translate voltage

| Performance Parameter | Proposed SS-TVLS | | Combined VLS of Figure 6 | |
|---|---|---|---|---|
| | $\mu$ | $\sigma$ | $\mu$ | $\sigma$ |
| Delay Rise (ps) | 35.1 | 2.4 | 52.0 | 3.9 |
| Delay Fall (ps) | 15.6 | 0.8 | 34.8 | 1.3 |
| Power Rise ($\mu$W) | 27.5 | 1.3 | 22.5 | 1.1 |
| Power Fall ($\mu$W) | 59.5 | 0.6 | 52.5 | 0.1 |
| Leakage Current High (nA) | 8.6 | 3.0 | 41.4 | 14.1 |
| Leakage Current Low (nA) | 3.6 | 1.3 | 32.3 | 9.0 |

**Table 4. Process variations simulation results for High to Low Level Shifting at T=$27^\circ$ C**

level efficiently for all VDDI and VDDO combinations. Figures 8 and 9 show the plot of rising and falling delays when VDDI and VDDO were varied between 0.8V to 1.4V. We can observe from these figures that the rising and the falling delays change smoothly with changing VDDI and VDDO voltage values over the entire voltage range. The plots of power and leakage are not shown due to space constraints, but they are also well behaved across the operating range. Therefore, we conclude that our SS-TVLS can effectively perform voltage level translation over a wide range of VDDI and VDDO voltage values and hence it is very suitable for SoCs and multi-cores processors systems.

The layout of the proposed SS-TVLS was created in the Cadence Virtuoso layout editor and shown in Figures 7. A layout versus schematic (LVS) check was done. The layout area of our SS-TVLS is $4.47\mu m^2$ (the width is $0.837\mu m$ and the height is $5.355\mu m$). The sizes of all the devices of our SS-TVLS are shown in Figure 4. The devices of our SS-TVLS were sized considering the tradeoff between delay and leakage power.

The experimental results clearly demonstrate that the proposed SS-TVLS performs much better than the combined VLS of Figure 6. When it is not known apriori whether VDDI $<$ VDDO or VDDI $>$ VDDO, then our SS-TVLS offers a great advantage over the combined VLS of Figure 6, due to its significantly lower leakage currents ($7.5\times$ ($4.4\times$) lower for a high output, and $19.5\times$ ($9.3\times$) lower for a low output, when VDDI $<$ VDDO (or VDDI $>$ VDDO)). Moreover, our SS-TVLS does not require any control signals. This helps in reducing the circuit complexity and also helps in placement and routing.

## 5 Conclusions

Modern ICs often have several voltage domains. Whenever a signal traverses voltage domains, a level shifter is required. Moreover, these ICs often employ dynamic voltage scaling, due to which it may not be possible to know apriori if a high-to-low or low-to-high voltage level conversion is required.

In this paper we have presented a novel single-supply "true" voltage level shifter (SS-TVLS), which can handle both low-to-high and high-to-low voltage translations. The use of a single supply voltage reduces layout congestion by eliminating the need for routing both supply voltages. The proposed circuit was simulated in a 90nm technology using SPICE. Simulation results demonstrate that the proposed SS-TVLS performs much better than the combined VLS of Figure 6. The combined VLS uses an inverter for high-to-low voltage translation and the best known previous approach [6] for low-to-high voltage level shifting. Also, we experimentally verified that our SS-TVLS operates correctly under

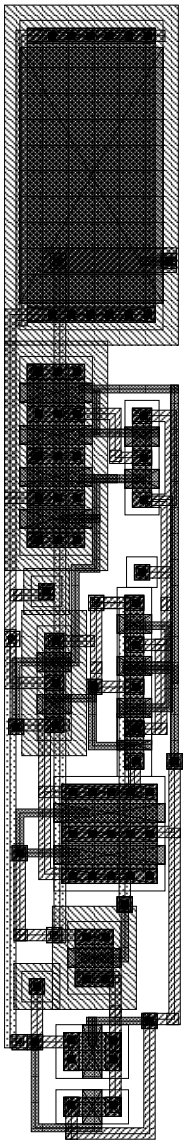

**Figure 7. Layout of our proposed SS-TVLS**

process and temperature variations.

Our SS-TVLS offers a great advantage over the combined VLS of Figure 6, due to its significantly lower leakage currents (7.5× (4.4×) lower for a high output, and 19.5× (9.3×) lower for a low output, when VDDI < VDDO (or VDDI > VDDO)). Our SS-TVLS is also faster than the combined VLS (5.5× (1.3×) faster for a rising output and 1.5× (2.2×) faster for a falling output, when VDDI < VDDO (or VDDI > VDDO)). Moreover, our SS-TVLS does not require any control signals. This helps in reducing the complexity of the circuit, and also helps in reducing the constraints during placement and routing.

## References


[1] D. Lackey, D. E. Lackey, P. S. Zuchowski, T. R. Bednar, D. W. Stout, S. W. Gould, and J. M. Cohn, "Managing Power and Performance for SOC Designs using Voltage Islands," in *Proc. of the Intl. Conf. on Computer-Aided Design*, pp. 195–202, Nov. 2002.

[2] T. H. et. al., "A Power Management Scheme Controlling 20 Power Domains for a Single-Chip Mobile Processor," in *Proc. of IEEE International Solid-State Circuits Conference*, pp. 540–541, Feb. 2006.


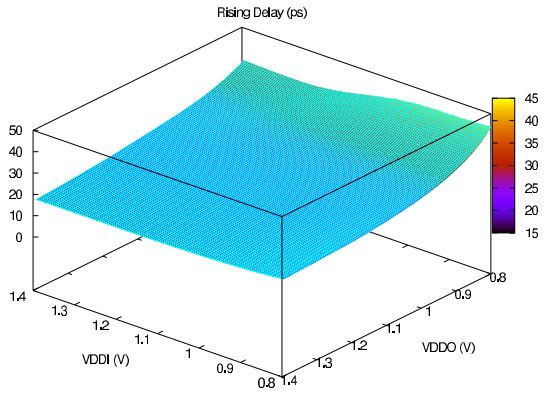


**Figure 8. Rising delay of our SS-TVLS**

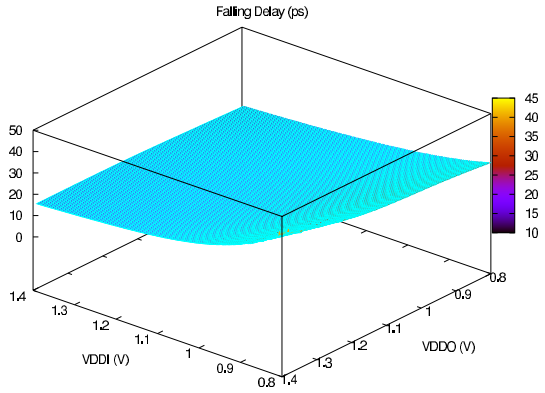


**Figure 9. Falling delay of our SS-TVLS**


[3] W. Kim, D. Shin, H. Yun, J. Kim, and S. Min, "Performance comparison of dynamic voltage scaling algorithms for hard real-time systems," in *Proc. of IEEE Real-Time and Embedded Technology and Applications Symposium*, pp. 219–228, 2002.

[4] B. Zhai, D. Blaauw, D. Sylvester, and K. Flautner, "Theoretical and Practical Limits of Dynamic Voltage Scaling," in *Proc. of the Design Automation Conf.*, pp. 868–873, 2004.

[5] C. Duan and S. P. Khatri, "Computing During Supply Voltage Switching in DVS Enabled Real-time Processors," in *Proc. of the Intl. Symposium on Circuits and Systems*, May 2006.

[6] Q. A. Khan, S. K. Wadhwa, and K. Misri, "A Single Supply level Shifter for Multi Voltage Systems," in *Proceedings of the 19th International Conference on VLSI Design*, Jan. 2006.

[7] PTM http://www.eas.asu.edu/ ptm.

[8] L. Nagel, "Spice: A computer program to simulate computer circuits," in *University of California, Berkeley UCB/ERL Memo M520*, May 1995.

[9] S. Tan and X.W.Sun, "Low power CMOS level shifters by bootstrapping technique," in *Electronics Letters*, pp. 876– 878, August 2002.

[10] A. U. Diril, Y. S. Dhillon, A. Chatterjee, and A. D. Singh, "Level-Shifter Free Design of Low Power Dual Supply Voltage CMOS Circuits Using Dual Threshold Voltages," *IEEE Transcations on VLSI systems*, vol. 13, September.

[11] W.-T. Wang, M.-D. Ker, M.-C. Chiang, and C.-H. Chen, "Level Shifters for High-speed 1-V to 3.3-V Interfaces in a 0.13-pm Cu-Interconnectiod/Low-k CMOS Technology," in *International Symposium on VLSI Technology, Systems, and Applications*, pp. 307– 310, 18-20 April 2001.

[12] D.Pan, H. Li, and B. Wilamowski, "A low voltage to high voltage level shifter circuit for mems application," in *Proceedings of the 15th Biennial University/Government/Industry Microelectronics Symposium*, 30 June-2 July 2003.

[13] R. Puri, L. Stok, J. Cohn, D. S. Kung, D. Z. Pan, D. Sylvester, A. Srivastava, and S. Kulkarni, "Pushing ASIC Performance in a Power Envelope," in *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 788– 793, june 2003.