

Modeling Dynamic Stability of SRAMs in the Presence of Single Event Upsets (SEUs)

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Abstract—SRAM yield is very important from an economics viewpoint, because of the extensive use of memory in modern processors and SOC. Therefore, SRAM stability analysis tools have become essential. SRAM stability analysis based on static noise margin (SNM) often results in pessimistic designs because SNM cannot capture the transient behavior of the noise. Therefore, to improve accuracy, dynamic stability analysis is required. The model presented in this paper performs dynamic stability analysis of an SRAM cell in the presence of an SEU event. The experimental results demonstrate that our model is very accurate, with a critical charge estimation error of 2.5% compared to HSPICE. The run-time of our model is also significantly lower ($1200\times$ lower) than the HSPICE run-time. Thus, our model enables the SRAM designer to quickly and accurately analyze stability during the design phase.

I. Introduction

Static random access memories (SRAMs) are an integral part of modern processors and system on chips (SOCs). Typically, SRAMs occupy more than half of the total chip area [1]. Hence from an economics viewpoint, SRAM yield is very important. In the deep submicron era, the supply voltage is often scaled to reduce power consumption [2], [3], [4]. At the same time noise effects in VLSI designs are increasing [5]. Although voltage scaling reduces the chip dynamic power consumption quadratically, it also reduces the noise tolerance of SRAM cells [3]. Thus SRAM verification and stability analysis has become an essential design task, required to improve the yield of processors and SOC.

Traditionally, static stability analysis is performed for memory designs in nanometer scale technologies. Static noise margin (SNM) [1] is one such metric traditionally used for static stability analysis. SNM is the maximum amplitude of the voltage deviation on an input node that can be tolerated without causing a change in the memory state. SNM is obtained by injecting static noise of constant amplitude (for an infinite time duration). However, not all transient noise will be present for a long duration of time and it is possible that a noise of a larger amplitude may lead to temporary disturbance which may not affect the SRAM state at all. Both the amplitude and the time duration of a noise event together determine whether the SRAM state will flip or not. Therefore, SNM based stability analysis fails to capture the time-dependent properties of specific noise patterns. Hence, the usage of SNM to analyze the stability of an SRAM cell during the design phase unnecessarily reduces design options, making it harder to employ power minimization techniques like dynamic voltage scaling.

To capture the effects of spectral and time-dependent properties of a noise signal on an SRAM cell, dynamic or time-dependent stability analysis needs to be performed. Dynamic noise margin (DNM) is one such analysis metric for time-dependent stability analysis, which allows us to perform more realistic SRAM noise analysis. However, most of the dynamic stability analysis methods proposed so far involve transistor and device level simulations which are quite complex and time-consuming in nature [6], [7]. Moreover these methods provide little insight into the problem of dynamic stability analysis. Recently, a model for dynamic stability of SRAMs was reported in [4]. However, this model assumes a rectangular noise signal which is typically not realistic for practical noise sources. This thus results in a large error compared to SPICE simulations. Therefore, there is a need to develop simple and accurate models for the dynamic stability of SRAMs, which

capture the time-dependent nature of the noise signal more closely.

There are many types of noise like power and ground noise, capacitive coupling noise, single event upsets (SEUs), etc. SEU is becoming a troublesome issue for memory arrays [6], [7] as well as combinational logic circuits [8], [9], [10]. However, SRAMs are less tolerant to radiation particle strikes than combinational logic circuits. Whether an SEU event (or any other transient noise) results in the state of SRAM cell being flipped or not depends upon both the amount of charge dumped as well as the time constants associated with the SEU event. In addition to this, the electric and the geometric parameters of an SRAM cell also play an important role in determining if the SRAM state flips. If the amount of charge dumped by a radiation strike is not sufficient, then the strike will only cause a temporary disturbance and will not result in a state flip. Hence, it is important to develop a compact and accurate model for SRAM cell stability in the presence of SEU events, to predict the result of an SEU particle strike (or error event). Such a model would be very useful to an SRAM designer, allowing them to quickly and accurately evaluate the SEU tolerance of their SRAM cell and make it more reliable. The work presented in this paper develops a model for dynamic stability of a 6-T SRAM cell in holding state, in the presence of SEU events. Our model can predict the effect of error events quite accurately, and the average critical charge estimation error of our model is just 2.5% compared to SPICE simulation. The extension of this work to other modes (read mode and write mode) of the SRAM cells is straight forward.

The rest of the paper is organized as follows. Section II briefly discusses some previous work in this area. In Section III we describe our model of SRAM cell in the presence of an SEU event. In Section IV we present experimental results, followed by conclusions in Section V.

II. Previous Work

Stability analysis of SRAM cell has been a topic of great interest for more than a couple of decades, due to its importance in obtaining high yields for microprocessor and SOC designs. A rich and well developed theory exists for static stability analysis of an SRAM cell [11], [12], [1]. In [12], the authors proved the formal equivalence of four different criterion for worst-case static noise margin. In [1], explicit analytical expressions were presented for the static-noise margin (SNM), as a function of device parameters and supply voltage. Several studies have also been performed to evaluate the effects of process variations on SRAM cell stability, using the SNM [13], [14]. Although a lot of work has been done in static stability analysis, not much work has been reported for dynamic stability analysis of SRAM cells. Most of the previous work on evaluating the effect of SEUs or transient noise on SRAM stability have used either device level or transistor level simulations [6], [7]. Thus, these methods are time consuming and cumbersome to apply. Recently, in [4], an analytical model of SRAM dynamic stability was presented for a rectangular pulse noise signal. The authors used non-linear system theory to derive the equation for the minimum time duration of the noise current which results in the flip of the SRAM cell state, given the amplitude of the noise current. The authors also tried to apply their approach to perform transient noise analysis due to SEUs, but the error of their approach is quite large compared to SPICE. Also they used a single exponential noise current to model SEUs. However, the current due to SEUs is modeled more

accurately by a double exponential [6], [7], [8], [9], [10] noise current. The model presented in this paper utilizes a double exponential current equation for SEUs, and it is able to predict more accurately whether an SEU event will result in a state flip in a 6T-SRAM cell.

III. Our Approach

In this paper, we present a model for the dynamic stability of a 6-T SRAM cell in the presence of an SEU event. During an SEU event, when an ion particle strikes the diffusion region of a transistor, it deposits charge, which results in voltage spike on the affected node. The current pulse that results from such a particle strike is traditionally modeled as a double exponential function [8], [10]. The expression for this pulse is

$$i_{noise}(t) = \frac{Q}{(\tau_\alpha - \tau_\beta)} (e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}) \quad (1)$$

Here Q is the amount of charge deposited as a result of the ion strike, while τ_α is the collection time constant for the junction and τ_β is the ion track establishment constant. Since SEU strikes are random events, when such an event occurs, an SRAM cell will most likely be in a holding state. Thus, our model is presented only for the holding state. However, the extension of our approach to other states of the SRAM is straightforward.

Our approach to model the dynamic stability of an SRAM is inspired by the non-linear system theory presented in [4]. Due to space constraints, we will provide a limited description of the theoretical concepts used in the approach of [4]. Figure 1 shows the schematic of a 6-T SRAM cell (note that the access transistors are not shown) with the noise current ($i_{noise}(t)$) due to the SEU event being injected into node $n2$. The total capacitances seen at node $n1$ and $n2$ are modeled by capacitors of value C , connected between these nodes and ground. The state of the SRAM cell shown in Figure 1 is described by a pair of node voltages (V_{n1}, V_{n2}). From the voltage transfer characteristics (VTC) of Inverter 1 and Inverter 2, the equilibrium points of the SRAM cell are (VDD,GND), (GND,VDD) and (VDD/2,VDD/2). Out of these equilibrium points, (VDD,GND) and (GND,VDD) are the stable equilibria whereas (VDD/2,VDD/2) is the metastable point. The two VTCs (drawn on one plot) of the inverters in the SRAM cell also form the state space for the SRAM cell system. In the state space of the SRAM cell, the region of attraction for the (VDD,GND) equilibrium point is the region described by $V_{n1} > V_{n2}$. This means that if the node voltages of the SRAM cell satisfy the condition $V_{n1} > V_{n2}$, then under no external input, the state of SRAM will reach the (VDD,GND) equilibrium point. Similarly, $V_{n1} < V_{n2}$ is the region of attraction for the (GND,VDD) state. The metastable equilibrium point represents the condition $V_{n1} = V_{n2}$. Therefore, when a SRAM cell is in the metastable state, a small amount of noise at the node $n1$ or $n2$ can take the state of the SRAM cell to either one of the stable equilibrium points. Thus, an SEU event can flip the SRAM cell state if the noise current induced by the SEU event can change the state of the SRAM cell from a stable equilibrium point to the region of attraction of the other stable equilibrium point, or atleast to the metastable point. This criterion is used to evaluate the dynamic stability of SRAM.

An SRAM cell is a non-linear system [4] due to the presence of a back-to-back inverter connection. It is very often the case that mathematical tools are unable to analytically solve such non-linear system equations. Therefore, to ensure that the model for SRAM's dynamic stability is manageable, we use a simple linear gate model [15] for the inverters. This model assumes that at any given time, either the NMOS or the PMOS device conducts (i.e. the short circuit current of an inverter is negligible). Let the input and output voltages of the inverter be V_{in} and V_{out} . Then the driving current (current flowing through the output node) of an inverter can be written as

$$I_{inv}(V_{in}, V_{out}) = \begin{cases} 0 & \text{cutoff} \\ V_{out}/R & \text{linear} \\ g_m(V_{in} - V_T) & \text{saturation} \end{cases}$$

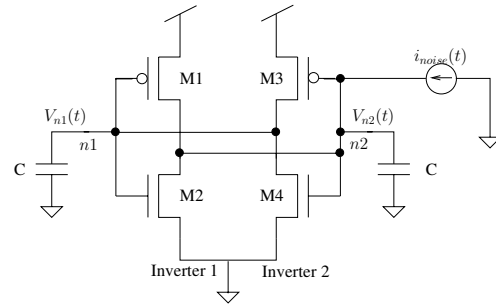


Fig. 1. Schematic of SRAM cell with Noise current (access transistors are not shown)

Here, g_m , R and V_T represent the transconductance, linear-region resistance and threshold voltage of the transistor of the inverter depending (PMOS or NMOS) which is conducting.

Without loss of generality, the analysis presented in this paper will assume that initially $V_{n1} = \text{VDD}$ and $V_{n2} = \text{GND}$. Therefore, the SRAM cell is in the (VDD,GND) state before the noise current is injected. The same analysis can also be applied when the initial SRAM state is (GND, VDD). Consider the SRAM cell of Figure 1. If a sufficiently large noise current is injected into node $n2$ then the SRAM node voltages V_{n1} and V_{n2} change as shown in Figure 2. Note that Figure 2 is provided for the purpose of explanation only. In practice the temporal trajectory of V_{n1} and V_{n2} may be different from what is shown in Figure 2, and will depend heavily on the value of Q . The goal of our model is to test whether a SRAM cell will indeed encounter a state flip, for a given value of Q . Initially, V_{n2} increases. However, V_{n1} remains almost at VDD. Then after the node voltage V_{n2} crosses V_{dsat} (the saturation voltage of NMOS transistor), V_{n1} starts decreasing rapidly. The first phase, where V_{n2} is increasing and V_{n1} is constant is referred to as the weak coupling mode (WCM), since the change in V_{n2} does not affect V_{n1} . The second phase, where both V_{n1} and V_{n2} change, is called strong feedback mode (SFM).

Figure 3 shows the flowchart of our model, which determines whether an SEU event results in the state of the SRAM cell being flipped or not. The SRAM cell starts in WCM mode when the noise current is injected into node $n2$. If the noise current is sufficiently large, then the SRAM will enter SFM otherwise, the SRAM continues to stay in WCM and therefore the SRAM state does not change. After the SRAM cell enters SFM, and if the noise current is large enough then V_{n1} can become greater than or equal to V_{n2} , resulting in an error condition. Otherwise, the SRAM cell does not flip and it comes back to its initial state of (VDD,GND). The steps of our model are explained in detail in the following sub-sections.

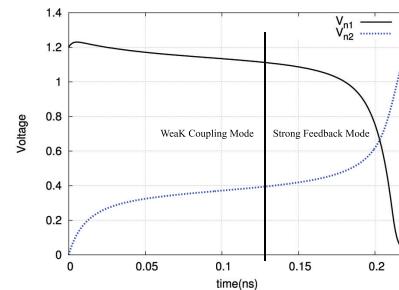


Fig. 2. SRAM node voltages for the noise injected at node $n2$

A. Weak Coupling Mode Analysis

In weak coupling mode, M2 is in the linear region while M4 is in cutoff. M4 is assumed to remain in cutoff during this mode if the threshold voltage of the NMOS transistor (V_{TN}) does not differ much from V_{dsat} . This is true for deep sub-micron technologies (due to short channel effects). As mentioned earlier, the node voltage V_{n1} remains

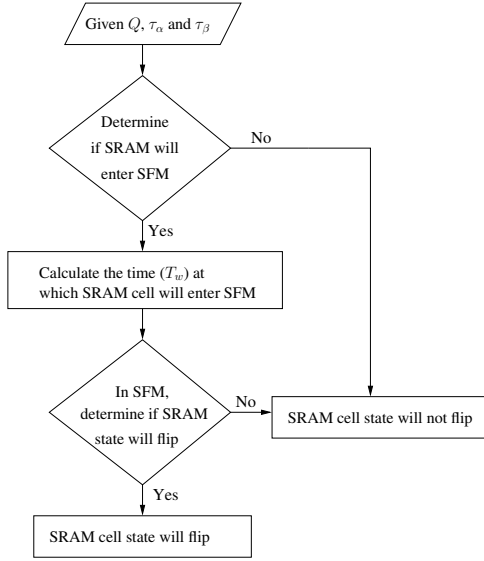


Fig. 3. Flowchart of our model for SRAM cell stability

almost at VDD in weak coupling mode. The equations governing the temporal behavior of the SRAM cell of Figure 1 are as follows:

$$dV_{n2}(t)/dt = -V_{n2}(t)/R_nC + i_{noise}(t)/C \quad (2)$$

$$V_{n1}(t) = VDD \quad (3)$$

Here, $i_{noise}(t)$ represents the current injected by an SEU event, as described by Equation 1. Given the current injected by an SEU, we have to determine whether this noise current will take the SRAM cell to strong feedback mode or not. To do this, we will compute the minimum value of charge (Q_{wc}) required to take an SRAM cell to SFM for the given values of time constants (τ_α and τ_β). To simplify the expression for Q_{wc} , we ignore the e^{-t/τ_β} term in the noise current of Equation 1. This is reasonable since τ_α is usually 3-4 times of τ_β and therefore e^{-t/τ_β} approaches 0 much faster than the e^{-t/τ_α} term. Hence, the e^{-t/τ_β} term contributes very little to the total noise current compared to e^{-t/τ_α} . Note that this assumption results in a lower bound value of Q_{wc} to be computed, and hence does not lead to any error in predicting the SRAM state flip. Integrating Equation 2 with initial condition $t = 0$, $V_{n2} = 0$, we get:

$$V_{n2}(t) = \frac{Q}{C(\tau_\alpha - \tau_\beta)X} (e^{-t/\tau_\alpha} - e^{-t/R_nC}) \quad (4)$$

where $X = \frac{1}{R_nC} - \frac{1}{\tau_\alpha}$

Now, we differentiate Equation 4 and equate $dV_{n2}(t)/dt$ to zero, to calculate the time $t_{V_{n2}M}$ at which V_{n2} reaches its maximum value if $V_{n2} \geq V_{dsat}$, we know that the cell has entered SFM. Substituting the expression for $t_{V_{n2}M}$ for the value of t in Equation 4 and V_{n2} by V_{dsat} we obtain the expression for Q_{wc} .

$$Q_{wc} = CX(\tau_\alpha - \tau_\beta) \frac{V_{dsat} e^{t_{V_{n2}M}/R_nC}}{e^{t_{V_{n2}M}/X} - 1}, t_{V_{n2}M} = \frac{1}{X} \ln\left(\frac{\tau_\alpha}{R_nC}\right) \quad (5)$$

If the charge dumped (Q) by an SEU event is greater than Q_{wc} then the SRAM cell will enter SFM, otherwise it stays in WCM. If SRAM enters SFM, then the state of SRAM cell can flip. To determine if it indeed flip, we need to calculate the time (T_w) at which the SRAM cell enters SFM. Again, consider Equation 2, integrate it using $i_{noise}(t)$ from Equation 1. The resulting equation for $V_{n2}(t)$ is:

$$V_{n2}(t) = \frac{I_n}{C} \left(\frac{e^{-t/\tau_\alpha}}{X} - \frac{e^{-t/\tau_\beta}}{Y} - Ze^{-t/R_nC} \right) \quad (6)$$

where $Y = \frac{1}{R_nC} - \frac{1}{\tau_\beta}$, $I_n = \frac{Q}{\tau_\alpha - \tau_\beta}$

$$Z = \frac{1}{X} - \frac{1}{Y}$$

To obtain T_w (the time when the SRAM enters SFM), we can substitute $V_{n2} = V_{dsat}$ and $t = T_w$ in Equation 6 and solve it for t . However, Equation 6 is a transcendental equation in t and hence it is not possible to obtain the expression for T_w analytically. Therefore, we linearly expand Equation 6 in t around the point T_w^{ini} (which is expected to be close to the actual value of T_w). To obtain a good expansion point T_w^{ini} , we approximate the noise current due to an SEU event by a rectangular pulse of magnitude I_{max} (which is the maximum value of $i_{noise}(t)$) and pulse width of a Q/I_{max} . Then the value of T_w^{ini} can be obtained using Equation 7 which was reported in [4] for a rectangular noise current pulse for the same SRAM cell as in Figure 1.

$$T_w^{ini} = -R_nC \ln[1 - V_{dsat}/(I_{max}R_n)] \quad (7)$$

Note that the manner in which we have modeled the SEU current pulse ensures that the T_w^{ini} is always smaller than the actual time (T_w) when the SRAM cell enters SFM. This is due to the fact that a rectangular noise current pulse of magnitude I_{max} , depositing a charge Q has more severe effects on the node voltages than the actual SEU current pulse of Equation 1 dumping the same amount of charge. It is critical to model the actual SEU current pulse because we don't want to miss detecting the SRAM cell state flip. This ensures that we avoid an optimistic SRAM cell design. From Equation 7, we also note that another condition which must be satisfied for an SRAM cell to enter SFM is $I_{max}R_n > V_{dsat}$. This condition is checked after the condition imposed by Q_{wc} is satisfied.

To obtain expression for T_w , first we perform the linear expansion of Equation 6 in t around the point T_w^{ini} (which is obtained from Equation 7) and then we solve for $t (=T_w)$. The resulting expression for T_w is as given below.

$$T_w = T_w^{ini} + \frac{V_{dsat} - \frac{I_n}{C} \left(\frac{e^{-T_w^{ini}/\tau_\alpha}}{X} - \frac{e^{-T_w^{ini}/\tau_\beta}}{Y} - Ze^{-T_w^{ini}/R_nC} \right)}{\frac{I_n}{C} \left(-\frac{e^{-T_w^{ini}/\tau_\alpha}}{\tau_\alpha X} + \frac{e^{-T_w^{ini}/\tau_\beta}}{\tau_\beta Y} + \frac{Z}{R_nC} e^{-T_w^{ini}/R_nC} \right)} \quad (8)$$

B. Strong Feedback Mode Analysis

When the SRAM cell of Figure 1 enters strong feedback mode, the transistors M2 and M4 are in the saturation region. In this mode, the node voltage V_{n2} increases (due to the noise current injected at node n2) which decreases the value of V_{n1} . The decrease in V_{n1} further helps in increasing the value of V_{n2} . Therefore, the node voltage V_{n1} depends upon V_{n2} and vice-versa and hence, the equations governing the time-domain behavior of the SRAM cell in the SFM are cross-coupled and non-linear in nature. These equations are given below.

$$dV_{n1}(t)/dt = -g_{mn}V_{n2}(t)/C + g_{mn}V_{TN}/C \quad (9)$$

$$dV_{n2}(t)/dt = -g_{mn}V_{n1}(t)/C + g_{mn}V_{TN}/C + \frac{Q}{C(\tau_\alpha - \tau_\beta)} (e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}) \quad (10)$$

Subtracting Equation 10 from Equation 9 and using transformation $u(t) = V_{n1}(t) - V_{n2}(t)$, we get.

$$du(t)/dt = g_{mn}u/C - \frac{Q}{\tau_\alpha - \tau_\beta} (e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}) \quad (11)$$

As mentioned earlier, for the SRAM cell to flip, the noise current should change the state of SRAM cell from the stable equilibrium point to the metastable equilibrium point ($V_{n2} = V_{n1}$), or change the SRAM state to the region of attraction of the other equilibrium point ($V_{n2} > V_{n1}$). Therefore, $u(t)$ (or $V_{n1}(t) - V_{n2}(t)$) should become equal to or less than 0. Now, we integrate Equation 11 with the initial condition $t = T_w$ and $u(T_w) = VDD - V_{dsat}$ and then applying the limit time t going to infinity. This is done because $u(t)$ may become equal to 0 (i.e. $V_{n1} = V_{n2}$) after the entire charge (or most of the charge) has been deposited on node n2. Also, the feedback from node n1 may also increase the node voltage V_{n2} after a large amount of time. Therefore,

the condition which must be satisfied for an SEU event to flip the SRAM state is as given below.

$$Q \geq C(\tau_\alpha - \tau_\beta)e^{-g_{mn}T_w/C} \frac{VDD - V_{dsat}}{e^{-T_w X'/X'} - e^{-T_w Y'/Y'}} \quad (12)$$

$$\text{where } X' = \frac{g_{mn}}{C} + \frac{1}{\tau_\alpha}, Y' = \frac{g_{mn}}{C} + \frac{1}{\tau_\beta}$$

IV. Experimental Results

We compared the accuracy of our model for the dynamic stability of the SRAM cell with HSPICE [16]. We designed the SRAM cell of Figure 1 using PTM 90nm [17] model card with VDD=1.2V. The device sizes are (W/L)=0.18 μ m/0.09 μ m for M2 and M4 and (W/L)=0.27 μ m/0.09 μ m for M1 and M3. The total node capacitance of nodes $n1$ and $n2$ is 4.8fC. The gate model characterization (computation of g_{mn} , R_n and V_{dsat}) was done for different VDD values in HSPICE.

We define Q_{cri} as the minimum amount of charge required to be deposited by an SEU event, in order to flip the SRAM state. Figure 4 compares the critical charge values (Q_{cri}) obtained using HSPICE and our model (for $\tau_\alpha=20$ ps, $\tau_\beta=5$ ps and for different values of VDD). To obtain the Q_{cri} value, we start with a small value of Q (i.e. 5fC) for the noise current of Equation 1. Then, we iteratively use any of 2 methods (HSPICE or ours) with increasing Q , to determine the value (Q_{cri}) at which SRAM cell state flips. From Figure 4, we can observe that our model is much more accurate and closer to HSPICE compared to the model of [4]. The average estimation error of our model is 4.5% whereas the error of the model of [4] is 11%. The error of our model is lower than that of [4] because unlike [4], we do not model the current due to an SEU event by a rectangular noise current pulse. Hence, our model can capture the time-dependent nature of the SEU current more closely, which improves the accuracy of our model. Note that the error of our model increases with increasing VDD values. We conjecture that this is due to the short channel effects and the drain induced barrier lowering. These effects result in an increase in the drain to source current of M2 and hence, a larger amount of charge is required to flip the SRAM state. Therefore, the error of our model increases with increasing VDD value.

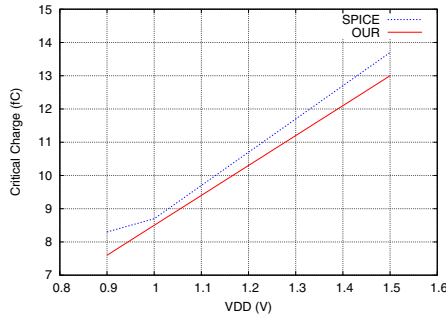


Fig. 4. Comparison of critical charge obtained using SPICE and our model

Table I compares the critical charge (Q_{cri}) obtained using our model and HSPICE for various values of τ_α , τ_β and VDD. In Table I, Columns 1 and 2 report the values of τ_α , τ_β under consideration. Column 3 reports the value of VDD. Column 4 reports the critical charge value (Q_{cri}^{HSPICE}) obtained using HSPICE. The critical charge value evaluated by our model (Q_{cri}^{OUR}) is reported in Column 5. Column 6 reports the percentage error in the critical charge value obtained using our model, compared to HSPICE. The ratio of the run-time of HSPICE and our model is reported in Column 7. Note that our model is able to obtain Q_{cri} value very accurately (with a small average error of 2.5%). Note that the error of the model reported in [4] was 11%. Also the run-time of our model is 1200 $\times$ better than the HSPICE run-time. The run-time of HSPICE is in the order of tens of seconds compared to the run-time of our model which is in the order of 10ms. Since SRAM design is an iterative process, it is valuable to use our model to evaluate the stability of an SRAM cell due to the significantly lower run-time

τ_α	τ_β	VDD	Q_{cri}^{HSPICE} (fC)	Q_{cri}^{OUR} (fC)	% ERROR	Run-time ratio
20	5	1.1	9.7	9.4	3.09	715
20	5	1.2	10.7	10.3	3.74	863
20	5	1.3	11.7	11.2	4.27	1030
20	5	1.4	12.7	12.1	4.72	1187
30	10	1.1	12.1	11.9	1.65	1066
30	10	1.2	13.4	13.1	2.23	1251
30	10	1.3	14.7	14.3	2.72	1402
40	10	1.1	13.7	13.7	0	1288
40	10	1.2	15.2	15.0	1.31	1514
40	10	1.3	16.7	16.5	1.20	1732
AVG					2.50	1205

TABLE I
COMPARISON OF MODEL WITH HSPICE

of our method compared to HSPICE.

V. Future Work and Conclusions

SRAMs are extensively used in modern processors and SOC's. Hence SRAM yield is very important from an economics viewpoint. As a result SRAM stability analysis has become quite important in recent times. SRAM stability analysis based on static noise margin (SNM) often results in pessimistic designs, because SNM cannot capture the transient behavior of the noise. Thus, SNM reduces design options, making it harder to employ aggressive power minimization techniques to SRAM. Therefore, to improve SRAM design, dynamic stability analysis is required. The model developed in this paper performs dynamic stability analysis of an SRAM cell in the presence of an SEU event. The experimental results demonstrate that our model is compact and very accurate, with a low critical charge estimation error of 2.5% compared to HSPICE. The run-time of our model is also significantly lower (1200 $\times$ lower) than the HSPICE run-time. Thus our model enables SRAM designers to quickly and accurately validate the stability of their SRAMs during the design phase.

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