A Fast, Analytical Estimator for the SEU-induced Pulse Width in Combinational Designs

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ABSTRACT

Single event upsets (SEUs) are becoming increasingly problematic for both combinational and sequential circuits with device scaling, lower supply voltages and higher operating frequencies. To design radiation tolerant circuits efficiently, techniques are required to analyze the effects of a particle strike on a circuit early in the design flow and also to evaluate the circuit's resilience to SEU events. In this paper, we present an analytical model for SEU induced transients in combinational circuits. The pulse width of the voltage glitch due to an SEU event is a good measure of SEU robustness and our model efficiently computes it for any combinational gate. The experimental results demonstrate that our model is very accurate with a very low pulse width estimation error of 4% compared to SPICE. Our model gains its accuracy by using a non-linear transistor current model, and by considering the effect of τ_β of the radiation induced current pulse. Our analytical model is very fast and accurate, and can therefore be easily incorporated in a design flow to implement SEU tolerant circuits.

Categories and Subject Descriptors: B.8.2 [Performance and Reliability]: Performance Analysis and Design Aids

General Terms: Design, Reliability

Keywords: Analysis, Model, Single Event Upset (SEU)

1. INTRODUCTION

In the deep sub-micron (DSM) era, continuously decreasing feature sizes, lower supply voltages and higher operating frequencies cause a reduction in the noise margins of VLSI designs. Thus VLSI circuits are becoming more vulnerable to noise effects such as crosstalk, power supply variations and single event upsets (SEU) or soft errors. SEUs are a particularly troublesome issue for memory arrays [1, 2] as well as combinational logic circuits [3, 10, 4]. SEUs occur when high energy protons or alpha particles strike diffusion regions in VLSI designs and deposit sufficient charge to modify the affected circuit node voltage. SEU may cause an erroneous computation by the circuit which can be latched by flip-flops and hence lead to system failure. Earlier, SEUs were considered problematic mainly for memories however, it is expected that the soft errors in combinational logic will dominate in future technologies [5, 6, 7].

Many critical applications such as biomedical, space and military electronics demand reliable circuit functionality. Therefore, the circuits used in these application must be tolerant to SEU events. To design SEU tolerant circuits, it is important to know the nature of SEU-induced transients and their effect on a circuit. It is also important to evaluate the SEU tolerance of a circuit using robustness metrics. Therefore, techniques are required to analyze a circuit early in the design flow and evaluate its resilience to SEU

events. Based on the results of this analysis, circuit hardening approaches can be implemented to achieve the level of protection required while satisfying area, delay and power constraints. This will remove the need of implementing radiation hardening during later design stages and thus it will reduce the number of design iterations. However, this can be achieved only if these techniques can quickly and accurately simulate the effects of SEU events of different particle energies for different gates with different loading conditions.

An exhaustive SPICE based simulation of SEU events in a combinational circuit would be accurate; however it would require a large number of simulations since the circuit can have a large number nodes and a radiation particle strike can occur at any one of these nodes. Also, the transient pulse resulting from an SEU event depends upon the node (node capacitance and the sizing characteristics of the gate driving that node), the amount of charge dumped by a radiation particle strike and the state of the circuit inputs. Therefore, it will be computationally intractable to use SPICE-based simulators for simulating the effect of SEU event at early stages in the design flow. Thus, there is a need for efficient and accurate models for SEU events.

The current pulse that results from a particle strike is traditionally described as a double exponential function [8, 9]. The expression for the pulse is

$$i_{seu}(t) = \frac{Q}{(\tau_\alpha - \tau_\beta)}(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}) \tag{1}$$

Here Q is the amount of charge deposited as a result of the ion strike, while τ_α is the collection time constant for the junction and τ_β is the ion track establishment time constant. Time constants τ_α and τ_β depends upon several process related parameters, and typically τ_α is on the order of 200ps and τ_β is on the order of tens of picoseconds [10, 6].

The modeling of SEU events in either combinational or sequential circuits involves solving non-linear differential equations. Because of this, not much success has been achieved in developing accurate and efficient models which are applicable across different scenarios (such as different gate power levels, dumped charge, fanout loading, etc). Modeling approaches in the past (as explained in Section 2) have made several assumptions and approximations which limit the applicability of the model due to the large error involved.

In this paper we present an analytical model for SEU induced transients in combinational circuits. Our model efficiently computes the pulse width of the voltage glitch[1] that results from a SEU particle strike. The main contributions of this paper are:

- A closed form analytical expression is presented for the pulse width of a voltage glitch induced by an SEU particle strike. The pulse width of the voltage glitch can be used as a measure of SEU robustness.

- The transistor I_{DS} model is being used for our analysis, which increases the analysis accuracy. In contrast, existing approaches [11, 12] model the electrical behavior of gate using linear RC circuit.

- Our model can be used for any combinational gate.

[1] The pulse width of the SEU induced voltage glitch is computed as the width of the voltage glitch, measured at half the supply voltage.

- Our model can be used for the analysis of SEU events with different amounts of charge deposited, different gate sizes and different gate loading.
- In contrast to [11, 12], we consider the effect of the ion track establishment constant (τ_β) of the SEU induced current pulse. This improves the accuracy of our method.

The pulse width of the voltage glitch due to an SEU event is a good measure of SEU robustness because, if a gate is more susceptible to SEU events, then a particle strike at the output node of that gate would result in a voltage glitch with a larger pulse width. On the other hand, if a gate is less susceptible to SEU events, then pulse width of the voltage glitch will be lower. The computation of the pulse width of the voltage glitch at a gate using our model is very fast and accurate; therefore, it can be easily incorporated in a design flow to implement SEU tolerant circuits. We envision that our approach can be used to quickly determine if the gates in a design result in positive pulse width. Such gates would be up-sized while accounting for logical masking [10]. This flow would be iterated until all primary outputs of the circuit are glitch-free. As a result, the *pulse shape is not required* to be computed.

In [6], it was mentioned that if the circuit response is faster than the time constants of the SEU event, then the SEU current pulse shape is critically important to accurately model the SEU event. For the 65nm PTM [13] model card, the delay of a minimum size inverter driving a fanout of three minimum size inverters is about 13ps which is much smaller than the typical time constants[2] associated with a radiation particle strike. Therefore, neglecting the contribution of the τ_β term of the current pulse of Equation 1 will lead to an inaccurate analysis. We have experimentally validated this and the results are presented in Section 4. Thus, it is critically important to model the contribution of both τ_α and τ_β. Our paper is the first to model the effect of both τ_α and τ_β. The average error in pulse width estimation is 4% compared to SPICE based simulation.

2. PREVIOUS WORK

The simulation and analysis of SEU-induced transients has been a topic of interest for many years. Much work has been done on this topic for combinational and sequential circuit elements [14, 1, 2, 11, 15, 9, 12]. Most of this work can be classified under three categories: device-level, circuit-level and logic-level.

Device based simulation approaches involve solving device physics equations to evaluate the effect of a radiation particle strike. In [16], three-dimensional numerical simulation is used to study the charge collection mechanism in silicon n^+/p diodes. Although device-level approaches result in very accurate analysis, they are extremely time-consuming in nature. Also, these techniques provide very little direct insight into the problem of circuit hardening.

For circuit-level and logic-level simulation approaches, a double exponential current pulse (Equation 1) is used to model a particle strike [8, 9, 4]. Logic-level based approaches [15] are utilized when the accuracy of the analysis is not very important compared to the speed of the analysis. In these approaches, the electrical nature of transient faults are abstracted into logic-level models, which are then used in gate-level timing simulations to propagate the effects of particle strikes to the memory elements at the outputs of the circuit. The high level of inaccuracy of these approaches makes them unattractive for robustness evaluation of circuits under SEU transients.

Circuit-level simulation approaches provide accuracy and run-times which are intermediate between device and logic based methods. SPICE based circuit simulation provides an accurate analysis, however it is still very time consuming since a large number of simulations are required to be performed due to the reasons mentioned in previous section. In [17], the authors presented a methodology to analyze compound noise effects in circuits. Their approach utilizes look-up tables and a database generated using SPICE for all the cells in a library. Many approaches [18, 12, 11] have been reported which attempt to solve a non-linear differential equation (this equation is called Ricatti differential equation) of the transistor to ob-

tain a closed-form expression for SEU-induced transients. However, due to non-linear nature of the differential equation, it is not possible to obtain a closed-form solution. Thus, many approximations have been proposed to model the SEU transients. The authors of [18] presented an exact solution of the Ricatti equation using a computationally expensive infinite power series solution. In [12], a switch-level simulator is presented, where fault simulation is performed in two steps. In the first step, a first order RC model is used to compute the pulse width due to a radiation particle strike and then in the second step, a set of rules are used for the propagation of the transient pulse through basic CMOS blocks. Electrical-level simulations are performed to obtain pulse widths for given resistance (R) and capacitance (C) values that model a gate. Then the pulse width for other R and C values are obtained using linear relationships between the obtained pulse width and the new R and C values. In [11], a closed form model is reported for SEU induced transient simulation for combinational circuits. Again, a linear RC gate model is used, which is derived using a SPICE-based calibration of logic gates for a range of values of fanout, charge deposited and scale factor. In [11, 12], the circuit simulation approaches *assume a linear RC gate model* which is not a valid assumption as will be explained in Section 3. Also, these approaches neglect the contribution of the ion track establishment constant (τ_β) of the SEU-induced current pulse of Equation 1, which further increases the inaccuracy in the analysis. In this paper, our model incorporates a transistor I_{ds} model along with the double exponential current pulse of Equation 1 to evaluate the pulse width of the voltage glitch. Our model can be used to evaluate the SEU robustness of a circuit, and hence determine which gates need to be hardened.

3. OUR APPROACH

In Section 3.1, we discuss the effect of a radiation particle strike at the output of an inverter, using SPICE [19] simulations. The inverters used in this discussion are implemented using a 65nm PTM [13] model card with $VDD = 1V$. Based on this discussion, we classify the radiation transient into 4 cases, in Section 3.2. Our model for an radiation-induced glitch, based on these cases, is introduced in Section 3.3. In Section 3.4, we provide details about our method to determine the pulse width of the radiation-induced voltage glitch.

3.1 Radiation Particle Strike at the Output of an Inverter

Consider an inverter INV1 driving three identical inverters as shown in Figure 1(a). These inverters are implemented using a 65nm PTM [13] model card with VDD=1V. Let node a be at logic value 0 when a radiation particle strikes the diffusion of INV1. This is modeled by the injection of $i_{seu}(t)$ (described by Equation 1) at node a. The voltage glitch that results from the radiation particle strike is shown in Figure 1(b) for four different inverter sizes (1X, 7X, 8X and 10X) and for Q=150fC, τ_α = 150ps and τ_β = 50ps. Note that all 4 inverters of Figure 1(a) are identical.
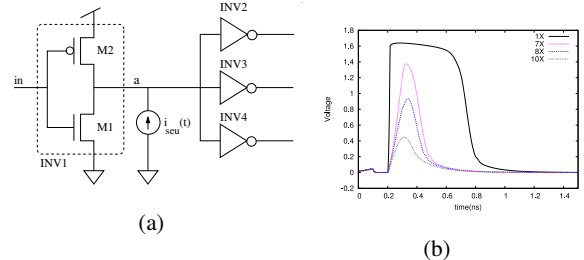

Figure 1: a) SEU current injected at the output of inverter INV1, b)Voltage glitch at node a

From Figure 1(b) we note that in case of 10X inverters, the radiation particle strike does not flip the node voltage and hence the logic value does not change (since the voltage glitch magnitude is less than 0.5V). Hence the radiation particle strike will not cause any error in circuit operation. In case of the 8X inverter, the node voltage at a rises to a value around 0.9V. As the voltage of node a starts rising, the NMOS transistor M1 of INV1 is in the linear

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[2]Typical rise times of an SEU event are in the range of 10-50ps and fall times are of the order of 200ps [6, 10]

region of operation. When the node voltage reaches V_{dsat}^{NMOS}, M1 enters the saturation region of operation. For this case, the PMOS transistor is always in cut-off (since its $V_{GS} = 0$). When the radiation particle strike occurs at the diffusion of the 7X inverter, the magnitude of the voltage glitch is around 1.4V. In this case also, M1 starts out in the linear-region, and enters the saturation region when the node voltage at a rises above V_{dsat}^{NMOS}. However, in this case, the PMOS transistor M2 of INV1 also turns on (in saturation mode) when the voltage of node a reaches $VDD + |V_{TP}|$ (here V_{TP} is the threshold voltage of the PMOS transistor) because the V_{GS} of M2 becomes smaller than V_{TP}. Note that in this case, the terminal of M2 which is connected to the output node a becomes the *source* terminal for M2 (when the node a voltage becomes greater than $VDD + |V_{TP}|$). In case of the 1X inverter, the diode between the source diffusion and the bulk of M2 also turns on (M1 and M2 both conduct in the saturation region under this condition) when the voltage of node a reaches a value greater than 1.6V. Therefore, the voltage of node a gets clamped to a value around 1.6V. Based on the above discussion, we note that M1 and M2 operate in different modes of operation (cut-off, linear and saturation) during the radiation-induced transient. Therefore, *it will not be accurate to model INV1 by a linear RC gate model*, as in the case [11, 12].

Based on the above discussion, we note that inverters of four different sizes operate quite differently during the radiation-induced transient, and the maximum voltage glitch magnitude (V_{GM}) determines their behavior at different times during the transient. In fact, when a radiation particle strikes the output node of INV1, there are 4 cases to consider. In the next section, we describe each of these cases based on the V_{GM} value. Based on this classification, we derive our analytical closed form expression for the pulse width of the SEU induced voltage glitch, in Section 3.4.

3.2 Classification of Radiation Particle Strikes

Without loss of generality, the analysis presented in this paper is for an inverter with its input at VDD and its output at GND. The radiation particle strike results in a positive voltage glitch at the output of the gate. However, the same analysis and the same analytical model can be used for any type of gate (NAND, NOR, etc), and for any logic values applied to its inputs. Handling of NAND, NOR, etc. gates is achieved by constructing an equivalent inverter for the gate. The size of this inverter depends on the given input values of the gate. The applicability of our model to different gates is verified by applying our model to a 2-input NAND gate (for all four input combinations). These results are presented in Section 4. Note that for multiple input gates, we do not consider the radiation particle strike at intermediate nodes of the gate, because the worst-case transient occurs when the particle strike occurs at the output node of the gate.

Again consider the inverter INV1 of Figure 1(a). INV1 can operate in 4 different *cases* during the radiation event transient, based on the maximum voltage glitch magnitude V_{GM}. The value of V_{GM} depends upon the sizes of the devices M1 and M2, the gate loading at the output node a and the value of Q, τ_α and τ_β. The pulse width of the voltage glitch is computed differently for different cases, due to the different behavior of M1 and M2 (Figure 1(a)) for these cases. Also, out of these 4 cases, the radiation event causes a node voltage flip for Cases 1, 2 and 3, and hence we present our analysis for these cases (i.e. for Cases 1, 2 and 3). The classification of INV1 operating in different cases is as follows.

- *Case 1 - $V_{GM} \geq VDD + 0.6V$*: In this case, with the increasing voltage of node a (V_a), M1 starts conducting in the linear region and enters the saturation region when the V_a becomes more than V_{dsat}^{NMOS}. M2 starts conducting in the saturation mode once V_a crosses $VDD + |V_{TP}|$. Eventually when V_a reaches $VDD + 0.6V$, the voltage between the source diffusion and the bulk terminal of the PMOS transistor M2 becomes $\geq 0.6V$. Therefore, the diode between these two terminals get forward biased and it starts conducting heavily. Thus V_a gets clamped to a value around $VDD + 0.6V$.

- *Case 2 - $VDD + |V_{TP}| \leq V_{GM} < VDD + 0.6V$*: In this case as well, both M1 and M2 conduct similar to Case 1. However, the diode between the diffusion and the bulk terminals of M2 remains off.

- *Case 3 - $VDD/2 \leq V_{GM} < VDD + |V_{TP}|$*: Only M1 conducts in this case. M1 starts conducting in the linear region and when V_a crosses V_{dsat}^{NMOS}, M1 enters the saturation region. M2 remains off in this case.

- *Case 4 - $V_{GM} < VDD/2$*: The voltage glitch of magnitude less than $VDD/2$ and hence the radiation event does not result in node voltage flip.

3.3 Overview of Our Model for Determining the Pulse Width of the Voltage Glitch

Figure 2(a) (shown at the top left portion of Figure 2) schematically illustrates a voltage glitch that results from a radiation strike at the output node a of INV1. As shown in Figure 2(a), the node voltage rises and reaches $VDD/2$ at time t_1, and the node voltage falls to $VDD/2$ (after reaching a maximum value of V_{GM}) at the time t_2. Hence the width of the voltage glitch of Figure 2(a) is $t_2 - t_1$. Our goal is to compute t_2, t_1 and therefore, the width of the glitch. Before we can use our model to compute pulse width, we characterize all the gates of different types and sizes in our library using SPICE [19]. For each gate (for all input combinations), we compute the current through the pull-down and pull-up stacks as a function of the gate output voltage, and store this in a look-up table. We also compute the input gate capacitance (C_G) and the output node diffusion capacitance (C_D) as a function of the input (output) node voltage and store them in a look-up table. For these lookup table entries, we discretize the voltages in steps of 0.1V. For example, for INV1 of Figure 1(a), we compute I_{DS} through M1 for different V_{DS} voltage values across M1, when node in is at VDD. Also we compute the I_{DS} value for M2 when in is at the GND value, for different values of V_{DS} across M2. Thus, the number of current look-up tables (the pull-up and the pull-down current tables) for any gate is equal to 2^n (where n is the number of inputs of a gate). Similarly, C_D is also computed depending upon the input state of the gate. We also obtain V_{dsat} for both NMOS and PMOS transistors for the nominal supply voltage value. Our model can be used for a circuit employing voltage scaling by obtaining V_{dsat} values for the different supply voltage values. This gate characterization step is performed once for each gate in a library and thus it does not affect the run-time of our model.
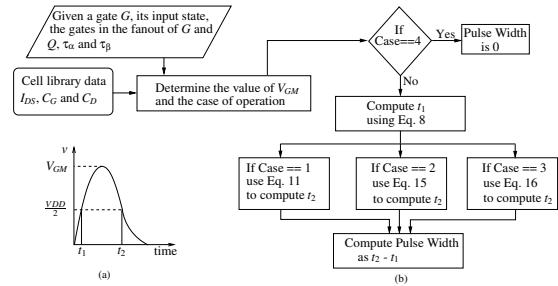

Figure 2: Flowchart of our model for Pulse Width Calculation

Figure 2(b) shows the flowchart of our algorithm to compute the values of t_1 and t_2 (and hence estimate the pulse width of the voltage glitch). The input to our model is a gate G (the radiation event is to be simulated at the output node of gate G), its input state, the list of gates which are driven by the gate G, and the values of Q, τ_α and τ_β. Our algorithm first computes V_{GM} and then determines the case that is applicable. If $V_{GM} < VDD/2$ (i.e. Case 4 applies), then the pulse width is 0 else t_1 is computed. Note that the expression of t_1 is the same for cases 1, 2 and 3. After this, the time t_2 is computed using case specific expressions. Finally the pulse width of the voltage glitch is returned ($t_2 - t_1$). The steps of our algorithm are explained in detail in the following sub-sections.

3.4 Derivation of Our Model for Determining the Pulse Width of the Voltage Glitch

As mentioned earlier, the analysis presented in this paper is for INV1 (Figure 1(a)) with its input node in at VDD and the output node a at GND. A radiation particle strike results in a positive voltage glitch at node a. To ensure that the model for radiation events in combinational circuit elements is manageable, we use a simple

drain-source current (I_{DS}) expression. Consider an NMOS transistor with the input gate terminal at VDD, then I_{DS} as a function of V_{DS} can be written as:

$$I_{DS}^{V_{DS}} = \begin{cases} V_{DS}/R_n & \text{linear } (V_{DS} < V_{dsat}^{NMOS}) \\ K_3 + K_4 \cdot V_{DS} & \text{saturation } (V_{DS} \geq V_{dsat}^{NMOS}) \end{cases}$$

Here, R_n is the linear region resistance, which is calculated using the I_{DS} versus V_{DS} lookup table for V_{DS} values less than V_{dsat}^{NMOS}. Similarly, the constants K_3 and K_4 are obtained by using the I_{DS} versus V_{DS} lookup table for V_{DS} values greater than V_{dsat}^{NMOS}.

To determine the applicable case, we first need to find V_{GM}. The method of finding V_{GM} is described next.

3.4.1 Voltage glitch magnitude V_{GM}

A radiation event can result in a voltage glitch with positive pulse width only if $I_{seu}^{max} > I_{DS}^{VDD/2}$, where I_{seu}^{max} is the maximum value of SEU-induced current pulse of Equation 1. This condition is used to check whether a radiation event will result in a voltage glitch of positive pulse width or not. The differential equation for the radiation-induced voltage transient at the output of INV1 of Figure 1(a) is given by:

$$C \frac{dV_a(t)}{dt} + I_{DS}^{V_a} = i_{seu}(t) \tag{2}$$

where, C is the capacitance[3] at node a. Equation 2 is accurate for values of V_a between 0V and $VDD + |V_{TP}|$. It is used to calculate V_{GM}. Note that if the estimated V_{GM} from Equation 2 is greater than $VDD + 0.6V$, we assume Case 1 applies. In some instances, a Case 2 V_{GM} value can be diagnosed as a Case 1 situation, which results in a pessimistic pulse width estimate. The above equation can be integrated with the initial condition $V_a(t) = 0$ at $t = 0$ to obtain $V_a(t)$. For deep sub-micron processes, V_{dsat} is much lower than $V_{GS} - V_T$ due to short channel effects. For the 65nm PTM [13] model card used in this paper, V_{dsat} for both NMOS and PMOS transistors is lower than $VDD/2$. Therefore, to obtain the V_{GM} value, we first integrate Equation 2 from the initial condition using the linear region equation for $I_{DS}^{V_a}$ till V_a reaches V_{dsat}^{NMOS} value. Then we again integrate Equation 2 using the saturation region equation for $I_{DS}^{V_a}$ to obtain the $V_a(t)$ expression. The equation for $V_a(t)$ is then used to calculate the value of V_{GM}. Now integrating Equation 2 using the linear region equation for $I_{DS}^{V_a}$ and with the initial condition $V_a(t) = 0$ at $t = 0$, we get:

$$V_a(t) = \frac{I_n}{C}\left(\frac{e^{-t/\tau_\alpha}}{X} - \frac{e^{-t/\tau_\beta}}{Y} - Ze^{-t/R_nC}\right) \tag{3}$$

$$where \quad X = \frac{1}{R_nC} - \frac{1}{\tau_\alpha}, Y = \frac{1}{R_nC} - \frac{1}{\tau_\beta}, I_n = \frac{Q}{\tau_\alpha - \tau_\beta}, Z = \frac{1}{X} - \frac{1}{Y}$$

To obtain the time T_{sat} when $V_a(t)$ reaches the V_{dsat}^{NMOS} value from Equation 3, we linearly expand Equation 3 around the initial guess T_{sat}^a. The expression for T_{sat} thus obtained is:

$$T_{sat} = T_{sat}^a + \frac{V_{dsat}^{NMOS} - \frac{I_n}{C}\left(\frac{e^{-T_{sat}^a/\tau_\alpha}}{X} - \frac{e^{-T_{sat}^a/\tau_\beta}}{Y} - Ze^{-T_{sat}^a/R_nC}\right)}{\frac{I_n}{C}\left(-\frac{e^{-T_{sat}^a/\tau_\alpha}}{\tau_\alpha X} + \frac{e^{-T_{sat}^a/\tau_\beta}}{\tau_\beta Y} + \frac{Z}{R_nC}e^{-T_{sat}^a/R_nC}\right)} \tag{4}$$

To obtain the initial guess T_{sat}^a, we approximate the rising part of the SEU-induced current by a line between the origin and the point where $i_{seu}(t)$ of Equation 1 reaches its maximum value I_{seu}^{max}. The SEU-induced current $i_{seu}(t)$ reaches I_{seu}^{max} at T_{seu}^{max}. Then we substitute this approximated SEU current in the RHS of Equation 2 and integrate it from the initial condition $V_a(t) = 0$ at $t = 0$ to $V_a(t) = V_{dsat}^{NMOS}$ at $t = T_{sat}^a$ using the linear region equation for $I_{DS}^{V_a}$. After this we solve for T_{sat}^a by performing a quadratic expansion of the resulting equation around the origin. The expression we get for T_{sat}^a is:

$$T_{sat}^a = \sqrt{\frac{2V_{dsat}^{NMOS} \cdot C \cdot T_{seu}^{max}}{I_{seu}^{max}}} \tag{5}$$

$$where \quad T_{seu}^{max} = \frac{\tau_\alpha \tau_\beta}{\tau_\alpha - \tau_\beta} \log \frac{\tau_\alpha}{\tau_\beta} \quad and \quad I_{seu}^{max} = i_{seu}(T_{seu}^{max})$$

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[3]The value of C is obtained by the addition of the average value of $n \cdot C_G$ and C_D over the operating voltage range. The factor of n occurs due to the fact that we assume a fanout of n.

So far we know T_{sat}, the time when $V_a(t)$ reaches V_{dsat}^{NMOS}, or the time when M1 enters the saturation mode. Now we again integrate Equation 2 with the initial condition $V_a(t) = V_{dsat}^{NMOS}$ at $t = T_{sat}$, and using the saturation region current equation for $I_{DS}^{V_a}$. The expression we get for $V_a(t)$ is:

$$V_a(t) = \frac{I_n}{C}\left(\frac{e^{-t/\tau_\alpha}}{X'} - \frac{e^{-t/\tau_\beta}}{Y'}\right) - \frac{K_3}{K_4} + Z'e^{-K_4t/C} \tag{6}$$

$$where \quad X' = \frac{K_4}{C} - \frac{1}{\tau_\alpha}, Y' = \frac{K_4}{C} - \frac{1}{\tau_\beta} and Z' = V_{dsat}^{NMOS}e^{K_4T_{sat}/C} -$$

$$\frac{I_n}{C}e^{K_4T_{sat}/C}\left(\frac{e^{-T_{sat}/\tau_\alpha}}{X'} - \frac{e^{-T_{sat}/\tau_\beta}}{Y'}\right) + \frac{K_3}{K_4}e^{K_4T_{sat}/C}$$

To calculate the value of V_{GM}, first we differentiate Equation 6 and equate $dV_a(t)/dt$ to zero and solve for $T_{V_{GM}}$ (the time at which $V_a(t)$ reaches its maximum value). Since the equation $dV_a(t)/dt = 0$ is also transcendental equation, hence we linearly expand $dV_a(t)/dt = 0$ around T_{seu}^{max} and solve for $T_{V_{GM}}$. We get:

$$T_{V_{GM}} = T_{seu}^{max} + \frac{\frac{e^{-T_{seu}^{max}/\tau_\alpha}}{\tau_\alpha X'} - \frac{e^{-T_{seu}^{max}/\tau_\beta}}{\tau_\beta Y'} + \frac{K_4Z'}{C}e^{-K_4T_{seu}^{max}/C}}{\frac{e^{-T_{seu}^{max}/\tau_\alpha}}{\tau_\alpha^2 X'} - \frac{e^{-T_{seu}^{max}/\tau_\beta}}{\tau_\beta^2 Y'} + \frac{K_4^2Z'}{C^2}e^{-K_4T_{seu}^{max}/C}} \tag{7}$$

Now, we calculate V_{GM} by substituting $T_{V_{GM}}$ obtained from Equation 7, in to Equation 6. Note that by using this method, V_{GM} can be evaluated to be greater than $VDD + 0.6V$, because the diode is not modeled in Equation 2. Therefore, if $V_{GM} > VDD + 0.6V$ then we set $V_{GM} = VDD + 0.6V$. Also note that we do not include the effect of the turning on of M2 (when $V_a(t)$ reaches a value above $VDD + |V_{TP}|$). This is done to keep the analysis simple. We found that neglecting the contribution of M2's current affects the accuracy of our model minimally. Based on the value of V_{GM}, we can decide the case which is applicable. If Case 4 applies, then the pulse width is 0 since the radiation event does not flip the logic level of the affected node. Otherwise, we compute the times t_1 and t_2 to calculate the pulse width of the voltage glitch at node a.

3.4.2 Derivation of the expression for t_1

As shown in the flowchart of our algorithm in Figure 2, the method to compute t_1 is identical for cases 1, 2 or 3. To obtain the expression for t_1, we substitute $t = t_1$ and $V_a(t_1) = VDD/2$ in Equation 6 and then solve for t_1 after expanding Equation 6 linearly around the point t_1^a (which is an initial guess for t_1). Here $t_1^a = T_{sat}VDD/(2V_{dsat}^{NMOS})$. The expression for t_1 is therefore:

$$t_1 = t_1^a + \frac{\frac{e^{-t_1^a/\tau_\alpha}}{X'} - \frac{e^{-t_1^a/\tau_\beta}}{Y'} + \frac{C}{I_n}(Z'e^{-K_4t_1^a/C} - \frac{K_3}{K_4} - \frac{VDD}{2})}{\frac{e^{-t_1^a/\tau_\alpha}}{X'\tau_\alpha} - \frac{e^{-t_1^a/\tau_\beta}}{Y'\tau_\beta} + \frac{K_4Z'}{I_n}e^{-K_4t_1^a/C}} \tag{8}$$

Using Equation 8, we can calculate the time at which the voltage at node a reaches to $VDD/2$. Note that we *do not ignore* τ_β in the calculation of t_1 (unlike [11, 12]).

3.4.3 Derivation of the expression for t_2

The method of obtaining the value of t_2 depends upon the value of V_{GM} (i.e. the case that is applicable). The derivation of the expression for t_2, for the different cases is as follows:

Case 1: We observed from voltage and current waveforms of the 1X inverter during radiation event that when $i_{seu}(t)$ becomes equal to the I_{DS} of M1 in Figure 1, then at that instant, the I_{DS} of M2 is approximately equal to 0 and the voltage at node a is $VDD + |V_{TP}|$. This is an important observation because this information will be used as the initial condition when integrating the INV1 output node voltage differential equation (Equation 2). Let $i_{seu}(t)$ become equal to the I_{DS} of M1 at time t_3. Then $V_a(t_3) = VDD + |V_{TP}|$. To calculate t_3, we ignore the contribution of the e^{-t/τ_β} term of $i_{seu}(t)$. This is reasonable since τ_α is usually 3-4 times of τ_β and therefore e^{-t/τ_β} approaches 0 much faster than the e^{-t/τ_α} term. Thus the value of e^{-t/τ_β} around t_3 (which is greater than T_{seu}^{max}) will be approximately equal to 0. The expression of t_3 thus obtained by equating $i_{seu}(t)$ (ignoring the e^{-t/τ_β} term) and $I_{DS}^{VDD+|V_{TP}|}$ is:

$$t_3 = -\tau_\alpha \log \frac{I_{DS}^{VDD+|V_{TP}|}}{I_n} \qquad (9)$$

Now, we model the radiation-induced current after time t_3 by a line, one of whose end-points has a current value of $I_{DS}^{avg} = 0.5 \cdot (I_{DS}^{VDD+|V_{TP}|} + I_{DS}^{VDD/2})$ at a time value of t_3. The other end-point has its current value as 0, and its time value t^* is obtained by equating the charge deposited by the actual SEU current $i_{seu}(t)$ from time t_3 to infinity and the charge deposited by linearized radiation-induced current equation. Hence the expression for the radiation-induced linear current model is:

$$i_{seu}^m(t) = I_{DS}^{avg}(1 - \frac{t - t_3}{t^* - t_3}) = K_1 - K_2 t \qquad (10)$$

$$where, t^* = t_3 + 2 \frac{I_n(\tau_\alpha e^{-t_3/\tau_\alpha} - \tau_\beta e^{-t_3/\tau_\beta})}{I_{DS}^{avg}}$$

Now we substitute $i_{seu}^m(t)$ for $i_{seu}(t)$ in Equation 2, use the saturation region equation for $I_{DS}^{V_a}$ and then integrate the resulting differential equation from time t_3 to t_2 (where $V_a(t_3) = VDD + |V_{TP}|$ and $V_a(t_2) = VDD/2$). The resulting equation is solved for t_2 by performing a quadratic expansion around the t_2^{a1} point. The resulting expression for t_2 is:

$$t_2 = t_2^{a1} + \frac{-Q + \sqrt{Q^2 - 4PR}}{2P} \qquad (11)$$

$$where, P = \frac{MK_4^2 e^{-K_4 t_2^{a1}/C}}{2C^2}, Q = \frac{K_2}{K_4} - \frac{MK_4 e^{-K_4 t_2^{a1}/C}}{C}, R = N + \frac{K_2 t_2^{a1}}{K_4} + Me^{-K_4 t_2^{a1}/C},$$

$$N = \frac{VDD}{2} - \frac{K_1 - K_3}{K_4} - \frac{K_2 C}{K_4^2}, M = e^{-K_4 t_3/C}(-VDD - |V_{TP}| + \frac{K_1 - K_3}{K_4} - \frac{t_3 K_2}{K_4} + \frac{K_2 C}{K_4^2})$$

To obtain the value of t_2^{a1}, we again integrate Equation 2 but this time we substitute $I_{DS}^{V_a}$ by a constant current of value $I_{DS}^{VDD+|V_{TP}|}$. The radiation-induced current is again modeled by a line with one end-point having a current value of $I_{DS}^{VDD+|V_{TP}|}$ at a time value of t_3. The other end-point is again found by equating the charge deposited by the actual SEU current $i_{seu}(t)$ from time t_3 to infinity and the charge deposited by linearized radiation-induced current equation. Equation 2 is integrated from time t_3 to t_2^{a1}. A closed form expression can be obtained for t_2^{a1}. The resulting expression for t_2^{a1} is:

$$t_2^{a1} = t_3 + \sqrt{\frac{C \cdot (VDD/2 + |V_{TP}|) \cdot (t^* - t_3)}{I_{DS}^{VDD+|V_{TP}|}}} \qquad (12)$$

Case 2: In this case, both M1 and M2 conduct because the magnitude of the voltage glitch is between $VDD + |V_{TP}|$ and $VDD + 0.6V$. Similar to Case 1, at time t_3, $i_{seu}(t)$ becomes equal to $I_{DS}^{VDD+|V_{TP}|}$ and the voltage of node a is $VDD + |V_{TP}|$. The value of t_3 is again obtained using Equation 9. To obtain the expression for t_2, we integrate Equation 2 with the initial condition $V_a(t_3) = VDD + |V_{TP}|$, using the saturation region current equation for the I_{DS} of M1. The resulting equation of $V_a(t)$ is:

$$V_a(t) = \frac{I_n}{C}(\frac{e^{-t/\tau_\alpha}}{X'} - \frac{e^{-t/\tau_\beta}}{Y'}) - \frac{K_3}{K_4} + Z''e^{-K_4 t/C} \qquad (13)$$

$$where, Z'' = (VDD + |V_{TP}|)e^{K_4 t_3/C} - \frac{I_n}{C}e^{K_4 t_3/C}(\frac{e^{-t_3/\tau_\alpha}}{X'} - \frac{e^{-t_3/\tau_\beta}}{Y'}) + \frac{K_3}{K_4}e^{K_4 t_3/C}$$

Now we use Equation 13 to compute t_2. For this we substitute $t = t_2$ and $V_a(t_2) = VDD/2$ in Equation 13, expand it around the initial guess point t_2^{a2} and then solve for t_2. Based on our observation, we find that t_2^{a2} (the time when $i_{seu}(t)$ falls to $I_{DS}^{VDD/2}$ after reaching I_{seu}^{max}) can be used as an initial guess for t_2 since the node voltage at that time will be close to $VDD/2$. We again ignore the contribution of the e^{-t/τ_β} term of $i_{seu}(t)$ when calculating t_2^{a2}. The expression for t_2^{a2} is:

$$t_2^{a2} = -\tau_\alpha \log \frac{I_{DS}^{VDD/2}}{I_n} \qquad (14)$$

Now we equate Equation 13 to VDD/2, expand it around t_2^a (from Equation 14) and then solve it for t_2. The expression for t_2 that we get is:

$$t_2 = t_2^{a2} + \frac{\frac{e^{-t_2^{a2}/\tau_\alpha}}{X'} - \frac{e^{-t_2^{a2}/\tau_\beta}}{Y'} + \frac{C}{I_n}(Z''e^{-K_4 t_2^{a2}/C} - \frac{K_3}{K_4} - \frac{VDD}{2})}{\frac{e^{-t_2^{a2}/\tau_\alpha}}{X'\tau_\alpha} - \frac{e^{-t_2^{a2}/\tau_\beta}}{Y'\tau_\beta} + \frac{K_4 Z''}{I_n}e^{-K_4 t_2^{a2}/C}} \qquad (15)$$

Case 3: In this case, only M1 of Figure 1(a) conducts because the magnitude of the glitch voltage is less than $VDD + |V_{TP}|$. Therefore, the voltage of node a from Equation 6 can be used to compute t_2. The initial guess for t_2 is obtained in the same manner as Case 2 using Equation 14. Now we equate Equation 6 to VDD/2, expand it around t_2^{a2} (from Equation 14) and then solve it for t_2. The expression for t_2 that we get is:

$$t_2 = t_2^{a2} + \frac{\frac{e^{-t_2^{a2}/\tau_\alpha}}{X'} - \frac{e^{-t_2^{a2}/\tau_\beta}}{Y'} + \frac{C}{I_n}(Z'e^{-K_4 t_2^{a2}/C} - \frac{K_3}{K_4} - \frac{VDD}{2})}{\frac{e^{-t_2^{a2}/\tau_\alpha}}{X'\tau_\alpha} - \frac{e^{-t_2^{a2}/\tau_\beta}}{Y'\tau_\beta} + \frac{K_4 Z'}{I_n}e^{-K_4 t_2^{a2}/C}} \qquad (16)$$

Using the values of t_1 and t_2 obtained in this section (for Cases 1, 2 and 3), we can find the pulse width of the voltage glitch at node a. Note that we *do not ignore* τ_β in the calculation of t_2 as well as t_1. We ignored the contribution of the e^{-t/τ_β} term of $i_{seu}(t)$ only during the *calculation of the initial guess* for t_2.

4. EXPERIMENTAL RESULTS

We compared the accuracy of our model for determining the pulse width of the voltage glitch induced by a radiation particle strike with SPICE [19]. Our method is implemented in *perl* and is much faster than SPICE simulation. In particular, for the results shown in this section, the SPICE simulations for the inverter with input 1 (input 0) took 12.6s (10.9s) while the perl script generated the result for input 1 as well as input 0 in 0.008s. Thus, our method is more than 1000X faster. Note that all our experiments were conducted on a Linux-based 3.6GHz Pentium 4 machine, with 3 GB of RAM. We implemented a cell library using a 65nm PTM [13] model card with $VDD = 1V$. Our cell library contains INV, NAND and NOR gates of different sizes and different numbers of inputs. As mentioned in Section 3.3, before we can use our model to compute the pulse width, we need to obtain look-up tables for the current through both the pull-up and down stacks, the input gate capacitance C_G and the output node diffusion capacitance C_D (for all input combinations) for all the gates in our library. The method to obtain the stack current, C_G and C_D look-up tables is explained in Section 3.3. For all experimental results reported in this paper, $Q = 150fC$, $\tau_\alpha = 150ps$ and $\tau_\beta = 50ps$. We have experimented with other values of Q, τ_α and τ_β, and have obtained similar results (which are omitted for brevity).

We applied our model to inverters of different sizes (with both possible input values) for determining the pulse width of the voltage glitch induced by a radiation particle strike. The circuit under consideration is similar to Figure 1(a) where INV1 is driving either 1 or 3 inverters of the same size, and a radiation particle strike occurs at the output node of INV1. The results thus obtained from SPICE and our model are reported by Table 1. In Table 1, Column 1 reports the number of inverters (of the same size as INV1) present in the fanout of INV1. Column 2 reports the size of INV1 in terms of multiples of a minimum-sized inverter. Columns 3 to 9 report the results when the input of INV1 is at the logic value 1. Columns 3 and 4 report the values of times t_1 and t_2 obtained using SPICE. Column 5 reports the pulse width (PW^S) of the voltage glitch that results from the radiation particle strike obtained from the SPICE. Columns 6, 7 and 8 report the values of t_1, t_2 and the pulse width (PW^M) calculated by our model. The percentage error of our model in the estimation of the pulse width compared to SPICE is reported in Column 9. Columns 10 to 16 report the same results as Columns 3 to 9 but for the input value of 0. We observe from Table 1 that our model estimates the pulse width of the voltage glitch due to radiation events quite accurately. The absolute average estimation error of our model is just 2.07% and 2.15% for the INV1 input values 0 and 1.

To demonstrate the applicability of our model to multiple input gates, we applied our model to a 2-input NAND gates of different sizes (for all input combinations). The 2-input NAND gate drive either 1 or 3 inverters of the same size as the equivalent inverter of

		INV1 with input 1							INV1 with input 0						
		SPICE			Our Model				SPICE			Our Model			
Load	Size	t_1(ps)	t_2(ps)	PW^S(ps)	t_1(ps)	t_2(ps)	PW^M(ps)	% Error	t_1(ps)	t_2(ps)	PW^S(ps)	t_1(ps)	t_2(ps)	PW^M(ps)	% Error
1	1	7	540	533	7	540	533	0.00	7	524	517	6	529	522	0.97
1	2	12	426	414	12	427	415	0.24	11	415	404	11	421	410	1.49
1	4	22	314	292	22	319	296	1.37	20	305	285	19	317	298	4.56
1	6	33	246	213	35	258	223	4.69	30	238	208	29	261	231	11.06
1	8	50	192	142	49	195	146	2.82	44	184	140	43	184	141	0.71
3	1	10	562	552	9	563	553	0.18	9	544	535	9	542	533	-0.37
3	2	16	448	432	15	450	434	0.46	15	435	420	14	434	420	0.00
3	4	28	336	308	27	342	315	2.27	25	326	301	24	330	306	1.66
3	6	42	269	227	42	281	239	5.29	37	258	221	36	257	221	0.00
3	8	62	209	147	61	214	152	3.40	53	200	147	51	199	148	0.68
AVG								2.07							2.15

Table 1: Pulse Width for INV1 Gate for $Q = 150fC$, $\tau_\alpha = 150ps$ and $\tau_\beta = 50ps$

		Inputs 11			Inputs 00			Inputs 01			Inputs 10		
Load	Size	PW^S(ps)	PW^M(ps)	% Error	PW^S(ps)	PW^M(ps)	% Error	PW^S(ps)	PW^M(ps)	% Error	PW^S(ps)	PW^M(ps)	% Error
1	1	497	501	0.80	404	402	-0.5	521	523	0.38	531	531	0.00
1	2	382	388	1.57	284	288	1.41	408	410	0.49	417	418	0.24
1	4	259	270	4.25	140	141	0.71	289	297	2.77	298	304	2.01
1	6	172	192	11.63	-	-	-	211	228	8.06	220	220	0.00
3	1	512	518	1.17	413	415	0.48	539	538	-0.19	548	548	0.00
3	2	396	404	2.02	292	300	2.74	423	424	0.24	432	434	0.46
3	4	271	285	5.17	145	145	0.0	304	310	1.97	312	318	1.92
3	6	183	191	4.37	-	-	-	224	225	0.45	232	233	0.43
AVG				3.87			0.97			1.82			0.63

Table 2: Pulse Width for NAND2 gate for $Q = 150fC$, $\tau_\alpha = 150ps$ and $\tau_\beta = 50ps$

the NAND2 gate, and a radiation particle strike occurs at the output node of the NAND2 gate. The results obtained from SPICE and our model are reported in Table 2 for all possible input states. Note that a '-' entry in Table 2 means that a Case 4 situation was found (no glitch). From Table 2, we observe that the absolute average estimation error of our model is no larger than 3.87%. For other input states, the inaccuracy of our model is even lower. The slight inaccuracy of our model is due to two reasons: i) sometimes we wrongly diagnose Case 2 situation as Case 1 as mentioned in Section 3.4.1; ii) the Miller feedback from the output node of the loading gates (like INV2 of Figure 1) to the node where radiation particle strike affects the the pulse width of the voltage glitch. We have not accounted for the effects due to this feedback in our model and hence, our model has a slight inaccuracy.

From Tables 1 and 2, we conclude that our model for the pulse width of the voltage glitch due to a radiation event is very accurate. The worst case average estimation error for inverters and 2-input NAND gate is less than 4%. We do not report the results for the other gates (like 3/4-input NANDs and NORs, etc) or the results for other values of Q, τ_α and τ_β due to the lack of the space.

As mentioned in Section 2, all previous approaches [18, 12, 11] have omitted the effect of τ_β in their analysis. To verify that ignoring τ_β impacts accuracy, we carried out SPICE simulations with and without τ_β and measured the pulse width. The percentage error by ignoring τ_β was found to be 9.7% for the inverter (averaged over all the cases in Table 1) and 9.2% for the NAND2 (averaged over all the cases in Table 2. Thus, it is essential to take τ_β into account, as our method does.

5. CONCLUSIONS

With the increasing demand for reliable systems, it is necessary to design radiation tolerant circuits efficiently. To achieve this, techniques are required to analyze the effects of a radiation particle strike on a circuit and evaluate the circuit's resilience to such events. By doing this early in the design flow, significant design effort and resources can be saved. In this paper, we present an analytical model for radiation-induced transients in combinational circuits. The pulse width of the voltage glitch due to an radiation event is a good measure of SEU robustness of a design. Our model efficiently computes the pulse width of the radiation-induced voltage glitch for any combinational gate. Our approach uses a transistor current model and also considers the effect of ion track establishment constant τ_β of the radiation induced current pulse, to improve the accuracy of the analysis. Experimental results demonstrate that our model is very accurate, with a very low pulse width estimation error of 4% compared to SPICE. Thus, our analytical model is very fast and accurate and can therefore be easily incorporated in a design flow to implement SEU tolerant circuits.

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