Circuit-level Design Approaches for Radiation-hard Digital Electronics

Rajesh Garg
(rajeshgarg_at_tamu.edu)

Nikhil Jayakumar
(nikhil_at_ece.tamu.edu)

Sunil P Khatri
(sunilkhatri_at_tamu.edu)

Gwan Choi
(gchoi_at_ece.tamu.edu)

Department of Electrical & Computer Engineering, Texas A&M University, College Station TX 77843.

Abstract

In this paper, we present a novel circuit design approach for radiation hardened digital electronics. Our approach is based on the use of shadow gates, whose task it is to protect the primary gate in case it is struck by a heavy cosmic ion. We locally duplicate the gate to be protected, and connect a pair of diode-connected transistors (or diodes) between the outputs of the original and shadow gates. These transistors turn on when the voltages of the two gates deviate during a radiation strike. Our experiments show that *at the level of a single gate*, our circuit structure has a delay overhead about 1.76% on average, and an area overhead of 277%. At the circuit level, however, we do not need to protect all gates. We present a methodology to selectively protect specific gates of the circuit in a manner that guarantees radiation tolerance for the entire circuit. With this methodology, we demonstrate that *at the circuit level*, the average delay overhead is about 3% and the average placed-and-routed area overhead is 28%, compared to an unprotected circuit (for delay mapped designs). We also propose an improved circuit protection algorithm to reduce the area overhead associated with our approach. With this approach for circuit protection, the area and delay overheads are further lowered.

I. Introduction

In recent times, there has been an increased interest in the radiation immunity of electronic circuits [1], [2], [3], [4], [5], [6], [7], [8], [9]. This has been an area of significant interest and research for space or military electronics [8], [7], [10], [11] for many years, due to the significantly larger rate of radiation bombardment in such applications. For space applications, neutrons, protons and heavy cosmic ions which are trapped in geomagnetic belts [10] produce intense showers of such radiation. When such ions strike diffusion regions in VLSI designs, they can deposit charge, resulting in a voltage spike on the affected circuit node. If the magnitude of this spike is sufficiently large, an erroneous value may be computed by the circuit. This is particularly problematic for memories, which can flip their stored state as a result of such a radiation strike. Combinational logic may also be affected by such strikes, if the resulting glitch occurs at the time the circuit outputs are being sampled. Such bit reversals are referred to as Single Event Upsets (SEUs) [12], or soft errors in the case of memory.

The charge deposition rate is also referred to as the Linear Energy Transfer (LET). Cosmic ions have varying LETs, and they result in the deposition of a charge Q in a semiconductor diffusion region of depth t by the following formula [11].

$$Q = 0.01036 \cdot L \cdot t$$

Here L is the LET of the ion (expressed in MeV/cm^2/mg), t is the depth of the collection volume (expressed in microns),

and Q is charge in pC. The amount of charge that is required to cause a bit to be sampled incorrectly is referred to as the critical charge, Q_C [13]. With diminishing process feature sizes and supply voltages, SEU problems are a concern even for terrestrial electronics today, particularly for mission critical applications. Atmospheric neutrons as well as alpha particles which are created by unstable isotopes in the IC packaging materials can also cause SEU problems. For reference, the LET of a 5 MeV alpha particle is 1 MeV/cm^2/mg [5]. Also, the probability distribution of energetic particles drops off rapidly with increasing LETs [2]. The largest population of particles have an LET of 20 MeV/cm^2/mg or less, and particles with an LET greater than 30 MeV/cm^2/mg are exceedingly rare [2], [3].

The current pulse that results from a particle strike is traditionally described as a double exponential function [14], [15]. The expression for this pulse is

$$I(t) = \frac{Q}{(\tau_\alpha - \tau_\beta)}(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}) \tag{1}$$

Here Q is the amount of charge deposited as a result of the ion strike, while τ_α is the collection time constant for the junction and τ_β is the ion track establishment constant. For the simulations reported in this paper, we used values of τ_β = 45ps, τ_α =145ps, and Q =24fC.

The remainder of this paper is organized as follows: Section II discusses some previous work in this area. In Section III we describe our radiation hardened design approach for digital electronics. In Section IV we present experimental results, while conclusions and future work are discussed in Section V.

II. Previous Work

There has been a great deal of work on radiation hardened circuit design approaches. Several papers report on experimental studies in this area [11], [13], [4], [16], [8], while others have focused on memory design [12], [13], [9], [17], [6], [7]. Since memories are particularly susceptible to SEU events, these efforts were crucial to space and military applications. Yet other approaches perform modeling and simulation of radiation events [15], [2], [5]. In [1], the authors address the sizing of transistors in a digital design in order to improve the radiation hardness of the design. In [9], the authors provide a built-in current sensor (BICS) to detect SEU events in an SRAM. A radiation hardened DRAM design was proposed in [17], while a FLASH memory based FPGA for space applications was introduced in [8].

Many techniques have been proposed earlier to selectively hardened gates in a logic circuit [18], [19], [20], [21]. These techniques try to harden those gates in a circuit which have higher soft error susceptibility i.e., the gates that contribute the most to the soft error failure of the logic circuit. Note that our gate level hardening approach presented in this paper can also be used with the selective hardening approaches reported in [18], [19], [20], [21]. Heijmen et al. proposed in [22] to selectively duplicate the sensitive logic gates (i.e. connecting two gates in parallel) to reduce Soft Error Rate (SER). Since this scheme involves a determination of sensitive gates (not all gates are protected), the tolerance achieved is not 100%. The authors reported that SER can be improved by 50% with an area penalty of 30%. Thus their approach does not provide 100% SEU protection whereas our approach offers 100% SEU tolerance, with a similar area penalty.

The aproaches which selectively hardened gates based on logical masking, electrical masking and latching window [18], [22] to improve the soft error susceptibility of a logic circuit cannot guarantee 100% SEU protection. In contrast to these approaches, we partition the gates of the circuit into protected gates (which are near the primary outputs) and unprotected gates, such that: a) If there is a SEU event in the unprotected gates, the latched values are unaffected due to electrical masking. b) If there is a SEU event in the protected gates, our circuit modification guarantees that the latched values are unaffected. Hence we are guarantee 100% SEU protection by electrical masking. The overhead of our scheme could be reduced by exploiting logical masking. But this is not possible for our circuits (without reducing 100% SEU protection) since we perform redundancy removal on our design to start with. Similarly, if we attempt to exploit latch window masking, the 100% SEU protection coverage of our scheme would drop.

Other radiation hard design approaches, such as triple modular redundancy, tackle the problem of correcting errors at the system level. In contrast to these approaches, we provide a circuit-level method to design radiation hard combinational logic. It can be used for memory elements as well. Our approach uses the notion of a clamping circuit which protects the output of a gate from an SEU event. We also present a methodology to selectively protect a standard-cell based design, in a manner which requires a minimum number of gates to be modified. Our experimental results demonstrate that the area and delay overheads of our approach (compared to an unprotected circuit) are 23.75% and 4.4% respectively, for delay mapped circuits.

A shorter version of the basic circuit level radiation hardening approach presented in this paper can be found in [23]. This manuscript provides additional details and an improved radiation hardening approach as well.

III. Our Approach

Radiation strikes cause charge to be dumped on a diffusion node, which results in voltage glitches on these nodes. We are concerned with those glitches that cause nodes to change their logical value (i.e. those that cross the switch-point of the gate in question). Our solution to the SEU problem involves a novel circuit design technique which ensures that such a glitch is clamped before it reaches the switch-point.

This section is divided into three subsections. In Section III-A, we discuss two circuit structures (shown in Figures 1 and 2) that we investigated, in order to create a radiation-hardened standard cell. Section III-B discusses the notion of *critical depth* for any protected library cell. A larger critical depth for any cell indicates that we require more logic stages for this cell to erase the effects of a radiation-induced glitch. Based on the notion of critical depth, Section III-C describes our algorithms to selectively protect cells in a standard-cell based circuit, so as to minimize the delay and area overhead.

A. Working of the Clamping Devices

A clamping diode can be used to suppress a glitch. However, this clamping diode should not prevent (or delay) the switching of the logic during its normal functional operation when no radiation strike has occurred. We hence need another similarly sized driver (logic gate) in parallel with the gate we are trying to protect (shown in Figures 1 and 2). When the outputs of these drivers deviate significantly (which would occur when one of the gates undergoes a radiation strike), the clamping circuit turns on, thereby protecting the gate from an SEU event. Note that the supply voltages for the protecting gate are higher (VDD =
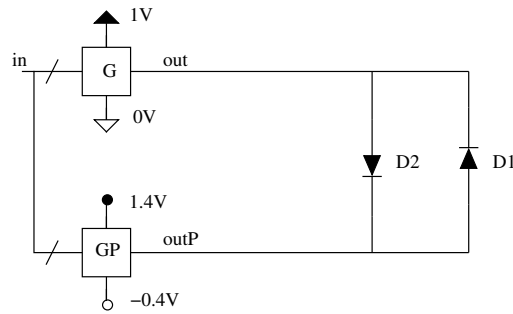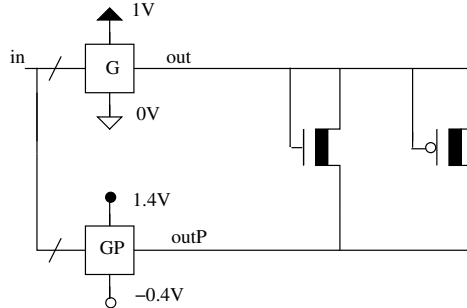
Fig. 1. Diode based SEU Clamping Circuit

Fig. 2. Device based SEU Clamping Circuit

1.4V and VSS = -0.4V). Hence we use thicker oxides for the protecting gates (GP) of Figures 1 and 2 and the diode connected devices of Figure 2, in order to avoid reliability problems. Multiple oxide thicknesses for a 65nm process has been used in past as reported in [24], [25], [26], [27]. The devices used in the protecting gate have a higher V_T (V_T^p = -0.42V and V_T^n = 0.42V) compared to the regular devices in our design (which have $V_{T_n} = 0.22V$ and $V_{T_p} = -0.22V$). This is to minimize the leakage through the protecting gate. The devices used for clamping also have a higher V_T to make sure that they are off during regular operation (in the absence of SEU events). This is important since their inputs are the same as those of the protected gate. In fact the clamping devices are on the verge of conduction (since V_T^p = -0.42V and V_T^n = 0.42V). Ideally we would want the protecting gate to have an even higher V_T (to minimize the leakage through this gate), but we restrict ourselves to two V_T values in this paper. The bulk terminal of the protecting gate (GP) and the diode connected devices of Figure 2 are connected to the protecting gate power supply i.e. VDD = 1.4V and VSS = -0.4. This ensures that the bulk terminals of these devices are not forward biased.

The clamping diodes used can either be regular PN junction type diodes or diode connected devices. We investigated both options.

1) PN Junction Diode

Consider the circuit in Figure 1. Let us first consider an SEU event that causes a rising pulse on the output node of a protected gate which is at logic 0. This means that the steady state output of the protected gate is at 0V and that of the protecting gate is at -0.4V. When the voltage on the protected node starts rising and when the voltage across the diode D2 (in Figure 1) reaches the diode turn-on voltage, it begins to clamp the voltage across it. In this way the glitch due to the SEU event is suppressed.

Now let us consider the case of an SEU event striking at the output (outP) of protecting gate which is at logic 0. In this case the protected node is still protected (remains at logic 0). This is because the protecting node is initially at a much lower voltage (-0.4V) and as the voltage at the protecting node rises, the diode D2 remains turned-off. Diode D1 turns on only when the voltage at the protecting node rises to a value greater than the diode turn-on voltage (i.e. voltage glitch = 0.4 + diode turn-on voltage). However, the cosmic particle which can cause such a glitch would have to have a very high energy.

The working of the clamping structure for falling pulses when the output node is at logic 1 is similar to that discussed above.

2) Diode Connected Device

Consider the circuit in Figure 2. Let us once again, consider a radiation event that causes a rising pulse on a node at logic 0. This means that the steady state output of the protected gate is at 0V and that of the protecting gate is at -0.4V. When the voltage on the protected node starts rising, the clamping NMOS device starts to turn on and turn on more strongly if the voltage on the protecting node continues to rise, thus clamping the protected node. If the radiation event strikes at the protecting nodes, the protected node remains at logic 0. This is because the protecting node is initially at a much lower voltage (-0.4V) and as the voltage at the protecting node rises, the clamping NMOS device turns off more. It is only when the voltage of the protecting node rises above 0.4V that the clamping PMOS device starts turning on. This could cause the voltage of the protected node to rise. As discussed in Section III-A.1 a radiation event to cause such a glitch would have to be very large.

In a similar manner, the clamping PMOS device helps protect a gate from a falling pulse due to a radiation event.

Both the device-based and diode-based clamping structures were implemented, and had very similar protection characteristics, as shown in the sequel. The layout area penalty of the device-based clamping structure was determined to be lower than that for a diode-based clamping structure. As a consequence, the experiments reported in the sequel are all based on the device based clamping structure. The performance of device-based and diode-based clamping structures for an inverter are presented in Tables I, II, III and IV. Rest all experiments are done for device-based clamping structure only as reported in experimental section.

We have verified that a SEU strike at the shadow gate will not cause extra soft errors (for the given value of Q, τ_α and τ_β). In particular, if there is a radiation particle strike at the output of protecting gate then the resulting glitch has to be much larger that the Q value used in our simulation, to turn on the diode connected devices and affect protected node. We have explicitly verified the correct operation of our circuit by striking each node of Figure 2 with both positive and negative glitches, for every gate in our design.

B. Critical Depth for a Gate

For each of the cells in our library, we designed counterpart cells which were radiation hardened, using diode connected devices to achieve radiation hardening. For each such radiation hardened cell, we computed its *critical depth*.

Consider a sequence of n copies of the same library cell C, with the output of the ith cell being one of the inputs of the $(i+1)^{th}$ cell. Let all the other inputs of the $(i+1)^{th}$ cell be assigned to their non-controlling values. Assume that the radiation strike occurs on the output of the cell at the first level, and corresponds to a charge Q being dumped on the output node
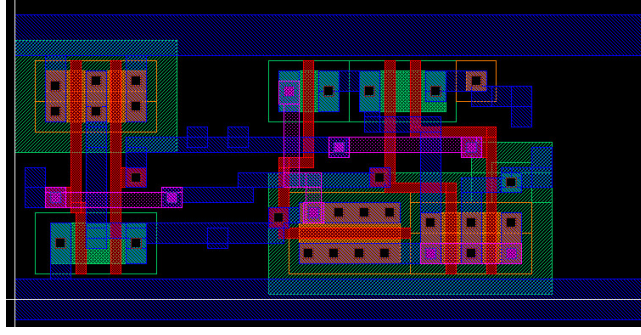
Fig. 3. Layout of SEU-tolerant NAND2 gate (uses Device based Clamping)

at the first level, with a collection time constant τ_α, and a ion track establishment constant of τ_β. Based on Equation 1, we can compute the effective current source that is connected to the corresponding output. Then the critical depth of library cell C, denoted as $\Delta(C)$, is defined as the number of levels of logic that are required for the magnitude of the glitch due to the radiation event to become smaller than $\gamma \times VDD$, where $\gamma < 1$. Note that $\Delta(C)$ is a function of Q, τ_α, and τ_β. The values of as $\Delta(C)$, were estimated using SPICE simulations.

C. Circuit Level Radiation Hardening

A simplistic approach would be to protect each gate in the design using our approach. However, this would result in an exorbitant delay and area overhead for the circuit. Instead, we propose a method where the delay and area overhead is minimized, while guaranteeing radiation hardness for the circuit.

Let $\Delta = max_C(\Delta(C))$. Given any circuit, we can protect all gates that are topologically Δ or less levels away from any primary outputs of the circuit. In this case, if there is a radiation strike on any protected cell, it would be eliminated because the cell is protected. If there is a radiation strike on an unprotected cell, it would be eliminated since it needs to traverse through Δ or more levels of protected gates before it reaches the output. In either case, the circuit is tolerant to the radiation event.

A variant of the above approach, which is slightly more efficient, is based on *variable depth protection*, and is described in Algorithm 1. It is based on a reverse topological traversal of a circuit η from its primary outputs. Let $deptharray()$ be the array of critical depths of all the library cells used in the implementation of the circuit η. The algorithm starts with a requirement to protect gates up to a reverse topological depth $D = \Delta(p)$, where $\Delta(p)$ is the critical depth of the gate at the primary output p. Whenever a gate C with critical depth $\Delta(C)$ is encountered, the algorithm updates the depth to be protected as $D = min(D - l, \Delta(C))$. Here, l is the topological depth of gate C from the primary output p.

Algorithm 1 Variable Depth Radiation Hardening for a Circuit

$variable\_depth\_protect(\eta, deptharray)$
for $each\ p \in PO(\eta)$ **do**
    $D = \Delta(p)$
    for $each\ cell\ C\ such\ that\ p \in fanout(C)$ **do**
        $l =$ topological depth of C from p
        $D = min(D - l, \Delta(C))$
        if $D > 1$ **then**
            $Replace\ C\ by\ C_{hardened}$
        end if
    end for
end for

D. Alternative Circuit Level Radiation Hardening

If a large number of gates with high critical depth are present near the primary outputs of a circuit then we might have to protect a significant portion of the circuit using our variable depth protection approach. This will result in large area and delay overheads. Column 5 of Table V reports the critical depth of all the gates in our library. We can observe from this table that the critical depth of inv2AA gate is much higher than the rest of the gates in our library. Therefore, if a large number of inv2AA gates are present near the primary outputs of a circuit then we will have a large area and delay overhead. Thus, to reduce the area and delay overhead associated with variable depth protection scheme, we present an algorithm which tries to reduce the number of gates with large critical depth (such as inv2AA) near the primary outputs of a circuit.

Our approach to further reduce the area or delay overhead is described in Algorithm 2. Let η be a mapped circuit obtained using library L with either area or delay as a cost function. Also let η^* be the circuit obtained after using variable depth protection algorithm on η. Now, we partition η^* into two parts, the first part is the unprotected portion of η^* represented by ζ and the second part is the protected portion of η^* represented by ϕ. We also modify our library L to obtain another library L^* in which we assign a large area and delay cost to gates with large critical depths (for example inv2AA). Now we re-synthesize ϕ with the new library L^* to obtain ϕ^* which will contain very few gates of high critical depth because of the high cost associated with them. Then, we combine ζ and ϕ^* and apply variable depth protection algorithm on the combined circuit to produce a SEU tolerant circuit η'. We will refer to the resulting circuit η' as the *re-synthesized hardened circuit*.

Algorithm 2 Alternative circuit level radiation hardening

$alternative\_circuit\_protect(\eta, L, deptharray)$
$\eta^* = variable\_depth\_protect(\eta, deptharray)$
$Decompose\ \eta^*\ into\ (\zeta, \phi)$
$L^* = modify(L)$
$\phi^* = re - synthesize(\phi, L^*)$
$\eta^c = combine(\zeta, \phi^*)$
$\eta^{'} = variable\_depth\_protect(\eta^c, deptharray)$

E. Final Circuit Selection

We get two different SEU tolerant versions η^* and η' of a regular circuit η using the approaches described in Sections III-C and III-D. We obtain the delay and area associated with both η^* and η'. Now our final radiation tolerant circuit can be obtained by choosing η^* or η' such that the area or the delay is minimized. We will refer to this approach as *improved circuit protection approach*.

IV. Experimental Results

The SEU tolerance of both our circuit structures was simulated in SPICE [28]. We used a 65nm BPTM [29] model card, with $VDD = 1V$ and $V_{T_N} = |V_{T_P}| = 0.22V$. The radiation strike was modeled as a current source described as $I(t) = \frac{Q}{(\tau_\alpha - \tau_\beta)}(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta})$.

Based on [9], we used a value of $\tau_\beta = 45ps$. We varied the values of τ_α and Q, to test our design against a variety of radiation conditions. Figure 4 describes the current injection waveform for various values of Q and τ_α.

The performance of both our designs is summarized in Tables I, II, III and IV. These tables report the protection results for

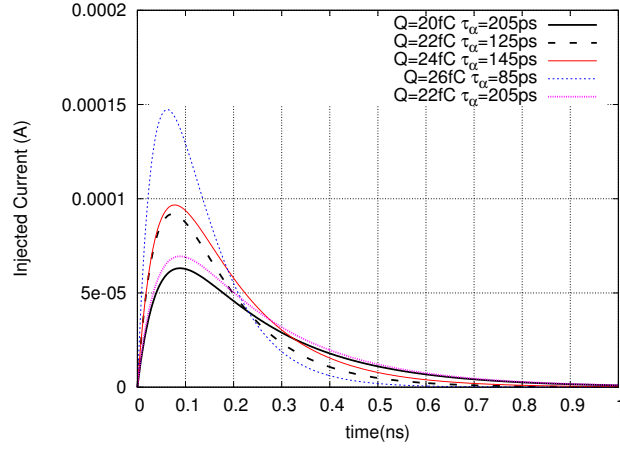Fig. 4. Current Injection Waveform as a Function of Q and τ_α

Q(fC)	Decay time τ_α (ps)									
	105	115	125	135	145	155	165	175	185	195
21	0.3170	0.2989	0.2843	0.2714	0.2603	0.2496	0.2419	0.2355	0.2245	0.2201
22	0.3325	0.3245	0.2985	0.2837	0.2722	0.2614	0.2503	0.2413	0.2331	0.2258
23	0.3475	0.3297	0.3105	0.2959	0.2835	0.2735	0.2608	0.2532	0.2427	0.2347
24	0.3643	0.3431	0.3259	0.3126	0.2970	0.2829	0.2713	0.2626	0.2517	0.2442
25	0.3810	0.3587	0.3393	0.3220	0.3103	0.2953	0.2837	0.2715	0.2621	0.2539
26	0.3998	0.3760	0.3538	0.3362	0.3192	0.3051	0.2933	0.2829	0.2734	0.2630
27	0.4171	0.3964	0.3682	0.3609	0.3320	0.3195	0.3040	0.2926	0.2833	0.2725
28	0.4365	0.4135	0.3854	0.3635	0.3468	0.3309	0.3157	0.3038	0.2921	0.2814
29	0.4579	0.4269	0.3995	0.3781	0.3596	0.3430	0.3267	0.3147	0.3073	0.2913
30	0.4779	0.4472	0.4173	0.3933	0.3744	0.3553	0.3394	0.3256	0.3144	0.3010

TABLE I

PERFORMANCE OF PN JUNCTION CLAMPING DIODE FOR RISING PULSES (OUTPUT AT LOGIC 0)

the INV-2X gate, which is the most radiation sensitive gate in our library. The first two tables report the simulation results for diode based clamping, and the latter two describe the results for device based clamping. For both styles, we report the glitch magnitude for varying values of τ_α and Q. The first and third tables report values of glitch magnitudes when the output is at logic 0, while the second and fourth correspond to an output at logic 1.

Based on these tables, we find that the regular PN junction diode tended to have better protection performance than the diode connected device for the same active area. However, implementing the PN junction diodes require a larger area on account of the spacing requirements of the wells which are at different potentials. The diode connected devices on the other hand share their well with the devices in the protecting gate, and can be implemented efficiently. Figure 3 describes the device-based clamping approach, applied to a nand gate. We created the layouts of the protected versions of all gates in our standard-cell library, which consisted of the cells INV-2X, INV-4X, AND2, AND3, AND4, OR2, OR3, OR4, NAND2, NAND3, NAND4, NOR2, NOR3 and NOR4.

Figure 5 describes the voltage waveform at the output of a gate, when a current corresponding to $Q = 24$ fC and $\tau_\alpha = 145ps$ is injected into this node. The voltage waveform of the unprotected design experiences a large glitch. If it were part of a memory element, the element could have erroneously flipped. Our device based clamping circuit successfully clamps the voltage to a safe level.

Q(fC)	Decay time τ_α (ps)									
	105	115	125	135	145	155	165	175	185	195
21	0.3102	0.2943	0.2822	0.2696	0.2589	0.2479	0.2417	0.2312	0.2233	0.2163
22	0.3246	0.3233	0.2936	0.2832	0.2691	0.2586	0.2496	0.2420	0.2337	0.2258
23	0.3400	0.3213	0.3065	0.2927	0.2801	0.2690	0.2601	0.2517	0.2429	0.2343
24	0.3545	0.3349	0.3204	0.3055	0.2913	0.2803	0.2713	0.2598	0.2532	0.2453
25	0.3683	0.3496	0.3356	0.3166	0.3042	0.2906	0.2818	0.2696	0.2611	0.2525
26	0.3836	0.3638	0.3488	0.3301	0.3155	0.3020	0.2901	0.2801	0.2697	0.2615
27	0.4004	0.3778	0.3576	0.3405	0.3262	0.3131	0.3005	0.2895	0.2818	0.2702
28	0.4156	0.3931	0.3803	0.3543	0.3403	0.3236	0.3116	0.2994	0.2888	0.2803
29	0.4348	0.4080	0.3880	0.3656	0.3504	0.3353	0.3212	0.3091	0.2989	0.2893
30	0.4515	0.4228	0.4014	0.3800	0.3851	0.3466	0.3346	0.3195	0.3089	0.2988

TABLE II

PERFORMANCE OF PN JUNCTION CLAMPING DIODE FOR FALLING PULSES (OUTPUT AT LOGIC 1)

Q(fC)	Decay time τ_α (ps)									
	105	115	125	135	145	155	165	175	185	195
21	0.3396	0.3163	0.2977	0.2790	0.2648	0.2527	0.2393	0.2285	0.2185	0.2097
22	0.3605	0.3354	0.3141	0.2958	0.2788	0.2660	0.2527	0.2416	0.2305	0.2207
23	0.3825	0.3547	0.3324	0.3111	0.2943	0.2811	0.2663	0.2548	0.2430	0.2334
24	0.4055	0.3742	0.3494	0.3301	0.3102	0.2946	0.2803	0.2674	0.2555	0.2437
25	0.4283	0.3963	0.3696	0.3472	0.3279	0.3111	0.2933	0.2780	0.2674	0.2556
26	0.4551	0.4176	0.3899	0.3656	0.3436	0.3237	0.3085	0.2927	0.2796	0.2682
27	0.4802	0.4413	0.4103	0.3874	0.3586	0.3400	0.3228	0.3076	0.2925	0.2805
28	0.5074	0.4664	0.4317	0.4045	0.3785	0.3580	0.3380	0.3203	0.3053	0.2920
29	0.5352	0.4916	0.4549	0.4232	0.3959	0.3730	0.3523	0.3351	0.3198	0.3055
30	0.5662	0.5163	0.4780	0.4435	0.4159	0.3904	0.3696	0.3506	0.3324	0.3176

TABLE III

PERFORMANCE OF DIODE-CONNECTED CLAMPING DEVICE FOR RISING PULSES (OUTPUT AT LOGIC 0)

Q(fC)	Decay time τ_α (ps)									
	105	115	125	135	145	155	165	175	185	195
21	0.3227	0.3024	0.2888	0.2738	0.2634	0.2432	0.2326	0.2233	0.2143	0.2046
22	0.3398	0.3192	0.3018	0.2839	0.2690	0.2576	0.2446	0.2377	0.2245	0.2150
23	0.3596	0.3359	0.3159	0.2978	0.2853	0.2700	0.2572	0.2462	0.2366	0.2274
24	0.3832	0.3539	0.3320	0.3134	0.2973	0.2848	0.2694	0.2596	0.2467	0.2417
25	0.4025	0.3709	0.3498	0.3300	0.3140	0.2961	0.2847	0.2699	0.2582	0.2470
26	0.4196	0.3891	0.3650	0.3479	0.3276	0.3098	0.2975	0.2838	0.2708	0.2608
27	0.4383	0.4149	0.3832	0.3597	0.3409	0.3259	0.3082	0.2931	0.2829	0.2698
28	0.4588	0.4302	0.4085	0.3782	0.3566	0.3386	0.3210	0.3063	0.2931	0.2809
29	0.4873	0.4463	0.4213	0.3944	0.3796	0.3531	0.3466	0.3184	0.3063	0.2964
30	0.5044	0.4681	0.4366	0.4087	0.3871	0.3665	0.3478	0.3327	0.3169	0.3102

TABLE IV

PERFORMANCE OF DIODE-CONNECTED CLAMPING DEVICE FOR FALLING PULSES (OUTPUT AT LOGIC 1)
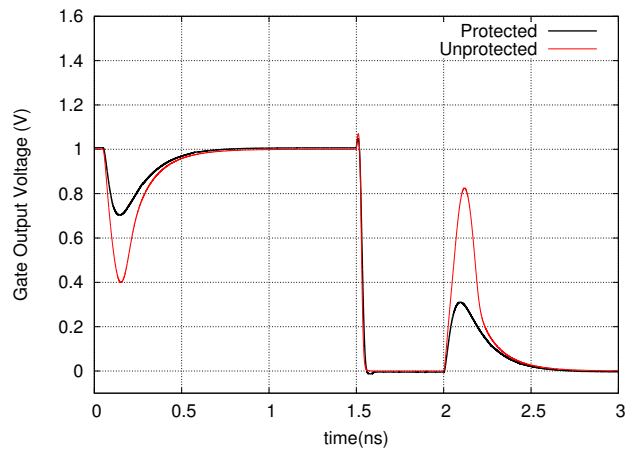
Fig. 5.   Output Waveform during a Radiation Event on Output

Figure 6 shows the voltage waveform at the output of a gate, when a current corresponding to Q = 24 fC and $\tau_\alpha = 145ps$ is injected into *the protecting* node. The voltage waveform of the output node is well within the noise margins of the gate.
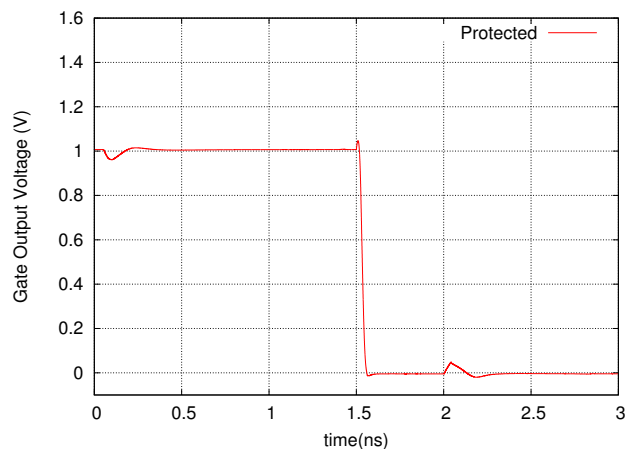

Fig. 6.   Output Waveform during a Radiation Event on Protecting Node

Based on the fact that we utilize the device-based protection scheme due to its better layout characteristics, we find the largest value of Q, for the most aggressive value of $\tau_\alpha = 145ps$ that our INV-2X cell can tolerate (from Tables III and IV). For $\gamma = 0.35$ (i.e. we can tolerate a glitch magnitude of $0.35 \times$VDD), we find that $Q = 24$fC.

Based on the values of $\tau_\alpha = 145ps$ and $\tau_\beta = 45ps$, we computed the critical depth $\Delta(C)$ for each gate C in our standard cell library. We used a value of $Q = 24$fC which results in a glitch magnitude of less than $0.35 \times$VDD. The results of this exercise are presented in Table V in Column 8. In addition to critical depth, Table V also reports the worst-case delay (in picoseconds) and the layout area (in μm^2) of each cell in our library. Columns 2 and 3 report the worst case delay of the unprotected and protected versions of the cell. Column 4 reports the percentage overhead in the worst-case delay of the hardened version of each cell compared to the regular version. Note that the worst-case delay of the protected cell is on average just slightly larger than that of a regular cell. Also note that for some cells (inv4AA, and3AA, etc) the delay overhead is negative. We conjecture that this is because of the fact that the leakage current of the hardened version of those cell is greater than the regular cell, therefore resulting in faster output transitions. Columns 5 and 6 report the layout area of unprotected and protected versions

Cell	Reg. Delay (ps)	Hard. Delay(ps)	Delay % Ovh.	Reg. Area (μm^2)	Hard. Area (μm^2)	Area % Ovh.	Depth
inv2AA	24.04	26.24	9.16	1.53	8.15	433.33	4
inv4AA	23.91	22.75	-4.88	2.04	9.60	370.83	1
nand2AA	31.42	33.01	5.06	2.04	9.17	350.00	1
nand3AA	44.92	46.10	2.63	2.55	10.70	320.00	1
nand4AA	62.44	63.34	1.44	3.06	12.23	300.00	1
nor2AA	45.62	48.46	6.24	2.55	10.19	300.00	2
nor3AA	77.15	81.04	5.04	4.59	14.52	216.67	1
nor4AA	92.80	92.74	-0.07	7.13	18.86	164.29	1
and2AA	57.48	58.52	1.81	2.55	10.19	300.00	1
and3AA	76.90	75.67	-1.60	3.06	11.72	283.33	1
and4AA	98.75	99.60	0.86	3.57	12.74	257.14	1
or2AA	71.16	71.00	-0.23	3.57	12.23	242.86	1
or3AA	112.87	113.37	0.44	5.35	15.29	185.71	1
or4AA	125.17	123.51	-1.32	8.15	20.89	156.25	1
AVG			1.76			277.17	

TABLE V

DELAY, AREA AND CRITICAL DEPTH OF CELLS

of cells. The area overhead of hardened version of each cell compared to the regular version is reported in Column 7. We note that the average area overhead is about 277% which is quite large. Therefore, we use variable depth protection to harden a circuit where only few gates are replaced with the radiation tolerant version. This helps in achieving lower area overhead.

Table VI reports the delay overhead of our SEU tolerant approaches (η^* and η') for both area and delay mapping. The area overhead of the SEU tolerant approaches is reported in Table VII. Tables IX and X report the delay and the area overhead respectively of the best SEU tolerant circuit (between η^* and η') using delay or area based mapping. The circuits were optimized using technology independent optimization in SIS (including redundancy removal), and were then mapped for area and delay using our 65nm standard cell library.

The delay penalty associated with applying our radiation hardening approaches is presented in Table VI. Delays were computed using the *sense* [30] package in SIS [31], which computes the largest sensitizable delay for a mapped circuit. In Table VI, Columns 2 and 3 report the delay (in picoseconds) of a regular design and a radiation-hardened area-mapped design (before re-synthesis). Column 4 reports the percentage delay overhead for the radiation-hardened design. Column 5 reports the delay of re-synthesized radiation-hardened area-mapped design (which are obtained as described in Section III-D) and Column 6 reports the percentage delay overhead for this design. Similarly, Columns 7 and 8 report the delay (in picoseconds) of a regular design and a radiation-hardened delay-mapped design (before re-synthesis). Column 9 reports the percentage delay overhead for the radiation-hardened design. Column 10 reports the delay of re-synthesized radiation-hardened delay-mapped design and Column 11 reports the percentage delay overhead for this design. We note that the circuit-level delay overhead of variable depth protection algorithm is as low as 2.92% on average for delay mapped designs, and about 1.6% for area mapped designs before re-synthesis. Note that our radiation hardened designs are generated by replacing regular gates (which are topologically close to the outputs) by hardened gates. This results in a large increase in the load capacitance of the regular gates that drive the hardened gates. As a consequence, the circuit level delay penalty in Table VI is sometimes larger than the gate-level delay penalty reported in Table V. The circuit-level delay overhead of the re-synthesized hardened circuit is 2.63% on average for delay mapped designs, and about 8.11% for area mapped designs which is higher than the delay associated with hardened circuit before re-synthesis. For area mapped circuits, the delay overhead increases (for η') because for resynthesis of the hardened circuit, we first extract the hardened portion of the circuit obtained from the variable depth protection algorithm.

Then we re-synthesize this sub-circuit with a high cost assigned to gates with a large critical depth, to minimize their utilization. This increases the utilization of gates with a large input load capacitance and hence, the load on the unprotected circuit increases resulting in a delay increase. However, for delay mapped designs, the delay overhead reduces due to the more usage of low overhead (and negative overhead) gates. Also note that sometimes, the delay overhead of the hardened circuit is negative. This is due to the increased usage of the hardened inv4AA gate which has a negative delay overhead over the regular inv4AA gate. We conjecture that this is because of the fact that the leakage current of the hardened inv4AA cell is greater than the regular inv4AA cell, therefore resulting in faster output transitions.

We technology mapped both the regular and the radiation hardened circuits using the library of cells mentioned in the beginning of this section. The resulting designs were placed and routed using SEDSM [32]. Note that we have accounted for routing of the additional power supplies. We have routed additional supply lines as regular signal lines. The area penalty associated with applying our protection algorithms is presented in Table VII. In Table VII, Columns 2 and 3 report the placed-and-routed area (in μm^2) of a regular design and the radiation-hardened area-mapped design (before re-synthesis). Column 4 reports the percentage area overhead for the radiation-hardened design. Column 5 reports the placed-and-routed area of re-synthesized hardened area-mapped design and Column 6 reports the percentage area overhead for this design. Similarly, Columns 7 and 8 report the area (in μm^2) of a regular design and a radiation-hardened delay-mapped design (before re-synthesis). Column 9 reports the percentage area overhead for the radiation-hardened design. Column 10 reports the placed-and-routed area of re-synthesized radiation tolerant delay-mapped design and Column 11 reports the percentage area overhead for this design. We note that the area overheads on average are larger for area-mapped designs, which is reasonable since the designs were mapped with an area-based cost function to start with. The average area penalty was about 45% and 28% for area and delay mapped designs obtained using variable depth protection approach before re-synthesis. However, the area overhead was around 29% and 24% for re-synthesized area and delay mapped hardened designs. The area overhead of re-synthesized designs is lower than that of the original designs since we utilize a small number of gates with high critical depth in the re-synthesized circuit. The area overhead of either of our approaches is significantly lower than the area overheads associated with alternate radiation hardening approaches, which commonly require logic duplication or triplication. Some designs (such as *frg2*) have a low logic depth and large number of inputs, and consequently, their area overheads are higher.

Table VIII reports the total number of gates and the number of hardened gates in a circuit resulted from using our circuit tolerant approaches (η^* and η') for both area and delay mapping. In Table VIII, Columns 2 and 3 report the total number of gates and the number of hardened gates of a radiation-hardened area-mapped design (before re-synthesis). Columns 4 and 5 reports these numbers for for the radiation-hardened design after re-synthesis. Similarly, Columns 5 and 6 report the total number of gates and the number of hardened gates for radiation-hardened delay-mapped design (before re-synthesis) and Columns 7 and 8 report for radiation-hardened delay-mapped design after re-synthesis, respectively.

The delay penalty associated with applying our improved circuit protection approach is presented in Table IX. We have two different radiation hardened versions for each design and we can choose the best among them in terms of area or delay. In Table IX, Column 2 reports the delay (in picoseconds) of a regular area-mapped design. Column 3 reports the delay of radiation-hardened area-mapped design with the best delay. Column 4 reports the percentage delay overhead for this design. Column 5

Ckt	Area Mapping					Delay Mapping				
	Regular	η^*	%Ovh.	η'	%Ovh.	Regular	η^*	%Ovh.	η'	%Ovh.
alu2	1211.680	1165.100	-3.84	1214.939	0.27	1052.595	1066.158	1.29	1073.261	1.96
alu4	1405.975	1435.371	2.09	1533.967	9.10	1319.840	1329.837	0.76	1425.119	7.98
C1355	960.003	990.448	3.17	984.751	2.58	775.568	787.417	1.53	787.417	1.53
C1908	1376.626	1385.880	0.67	1486.142	7.96	1172.012	1184.320	1.05	1215.548	3.71
C3540	1682.691	1728.315	2.71	1772.920	5.36	1560.553	1571.991	0.73	1588.231	1.77
C499	960.003	990.448	3.17	984.751	2.58	775.568	787.417	1.53	787.417	1.53
C880	1606.093	1669.115	3.92	1323.711	-17.58	1544.077	1570.779	1.73	1239.997	-19.69
dalu	1325.516	1363.747	2.88	1415.225	6.77	1221.374	1233.771	1.02	1232.717	0.93
des	2170.999	1721.303	-20.71	2595.902	19.57	2016.371	2053.416	1.84	2272.788	12.72
frg2	910.514	930.828	2.23	991.758	8.92	911.745	957.092	4.97	870.592	-4.51
i2	462.161	477.990	3.42	478.714	3.58	377.435	386.718	2.46	417.151	10.52
i3	172.459	199.782	15.84	233.170	35.20	172.459	199.782	15.84	194.383	12.71
i10	2217.855	2335.109	5.29	2685.245	21.07	2246.170	2318.547	3.22	2315.502	3.09
AVG			1.60		8.11			2.92		2.63

TABLE VI

DELAY OVERHEAD OF OUR RADIATION HARDENED DESIGN APPROACHES

Ckt	Area Mapping					Delay Mapping				
	Regular	η^*	%Ovh.	η'	%Ovh.	Regular	η^*	%Ovh.	η'	%Ovh.
alu2	1045.88	1418.28	35.61	1215.22	16.19	1397.26	1569.74	12.34	1569.74	12.34
alu4	1994.52	2470.09	23.84	2279.11	14.27	2470.09	2756.25	11.59	2756.25	11.59
C1355	1592.01	2121.52	33.26	1994.52	25.28	1728.90	2279.11	31.82	2279.11	31.82
C1908	1569.74	1994.52	27.06	1799.46	14.63	1799.46	2225.95	23.70	2279.11	26.66
C3540	3183.22	3916.26	23.03	3573.65	12.27	4022.10	4572.46	13.68	4515.84	12.28
C499	1569.74	2121.52	35.15	1994.52	27.06	1728.90	2279.11	31.82	2279.11	31.82
C880	1045.88	1752.26	67.54	1418.28	35.61	1397.26	1871.43	33.94	1764.00	26.25
dalu	2470.09	2996.47	21.31	2965.89	20.07	3310.85	4057.69	22.56	3573.65	7.94
des	9964.03	16842.85	69.04	13731.15	37.81	12139.63	17800.90	46.63	15490.29	27.60
frg2	1994.52	4201.63	110.66	3916.26	96.35	2611.21	4147.36	58.83	4238.01	62.30
i2	685.39	730.08	6.52	745.29	8.74	872.61	872.61	0.00	872.61	0.00
i3	495.51	670.81	35.38	600.25	21.14	495.51	656.38	32.47	600.25	21.14
i10	6037.29	12016.54	99.04	9304.53	54.12	7705.33	11231.76	45.77	11054.42	43.46
AVG			45.19		29.50			28.09		24.25

TABLE VII

AREA OVERHEAD OF OUR RADIATION HARDENED DESIGN APPROACHES

reports the delay of the radiation-hardened area-mapped design with the best area and Column 6 reports the percentage delay overhead for this design. Similarly, Column 7 reports the delay (in picoseconds) of a regular delay-mapped design. Column 8 reports the delay of the radiation-hardened delay-mapped design with the best delay. Column 9 reports the percentage delay overhead. Column 10 reports the delay of the radiation-hardened delay-mapped design with the best area and Column 11 reports the percentage delay overhead for this design. We note that the circuit-level delay overhead of our improved circuit protection algorithm is as low as 0.29% on average for delay mapped designs, and about -0.14% for area mapped designs.

The placed-and-routed area penalty associated with applying our improved circuit protection approach is presented in Table X. In Table X, Column 2 reports the placed-and-routed area (in μm^2) of a regular area-mapped design. Column 3 reports the area of the radiation-hardened area-mapped circuits with the best delay. Column 4 reports the percentage area overhead for the corresponding design. Column 5 reports the area of the radiation-hardened area-mapped design with the best area and Column 6 reports the percentage area overhead for this design. Similarly, Column 7 reports the area (in μm^2) of a regular delay-mapped design. Column 8 reports the area of the radiation-hardened delay-mapped circuit with the lowest delay. Column 9 reports the percentage area overhead for the corresponding circuit. Column 10 reports the area of the radiation-hardened delay-mapped designs with the least area and Column 11 reports the percentage area overhead of corresponding design. We note that the circuit-level area overhead of improved circuit protection algorithm is 23.75% on average for delay mapped designs, and about 29.33% for area mapped designs.

Ckt	Area Mapping				Delay Mapping			
	η^*		η'		η^*		η'	
	Total # of Gate	# of Hardened Gates	Total # of Gate	# of Hardened Gates	Total # of Gate	# of Hardened Gates	Total # of Gate	# of Hardened Gates
alu2	273	45	270	7	429	17	474	7
alu4	537	52	531	11	795	27	845	14
C1355	455	51	450	32	582	32	582	32
C1908	406	45	415	25	579	27	597	25
C3540	893	80	904	22	1290	46	1356	24
C499	455	51	450	32	582	32	582	32
C880	308	54	310	26	417	51	445	31
dalu	733	51	747	19	1064	38	1082	16
des	2795	545	2628	245	3812	365	4213	245
frg2	597	221	579	132	846	144	941	137
i2	151	2	151	3	228	3	230	1
i3	110	14	110	6	114	14	118	6
i10	1775	519	1787	233	2507	346	2792	243

TABLE VIII

TOTAL NUMBER OF GATES AND NUMBER OF HARDENED GATE IN DIFFERENT DESIGNS

Ckt	Area Mapping					Delay Mapping				
		Best Delay		Best Area			Best Delay		Best Area	
	Regular	$min(\eta^*,\eta')$	%Ovh.	$min(\eta^*,\eta')$	%Ovh.	Regular	$min(\eta^*,\eta')$	%Ovh.	$min(\eta^*,\eta')$	%Ovh.
alu2	1025.881	1165.1	-3.84	1214.939	0.27	883.78	1066.16	1.29	1073.26	1.96
alu4	1219.078	1435.371	2.09	1533.967	9.1	1126.59	1329.84	0.76	1329.84	0.76
C1355	835.347	984.751	2.58	984.751	2.58	670.35	787.42	1.53	787.42	1.53
C1908	1206.572	1385.88	0.67	1486.142	7.96	1028.11	1184.32	1.05	1184.32	1.05
C3540	1466.264	1728.315	2.71	1772.92	5.36	1343.16	1571.99	0.73	1588.23	1.77
C499	835.347	984.751	2.58	984.751	2.58	670.35	787.42	1.53	787.42	1.53
C880	1402.478	1323.711	-17.58	1323.711	-17.58	1319.60	1240.00	-19.69	1240.00	-19.69
dalu	1041.554	1363.747	2.88	1415.225	6.77	1008.48	1232.72	0.93	1232.72	0.93
des	1476.792	1721.303	-20.71	2595.902	19.57	1459.22	2053.42	1.84	2272.79	12.72
frg2	768.107	930.828	2.23	991.758	8.92	756.23	870.59	-4.51	957.09	4.97
i2	432.983	477.99	3.42	477.99	3.42	346.60	386.72	2.46	417.15	10.52
i3	160.868	199.782	15.84	233.17	35.2	160.87	194.38	12.71	194.38	12.71
i10	1879.402	2335.109	5.29	2685.245	21.07	1882.47	2315.50	3.09	2315.50	3.09
			-0.14		8.09			0.29		2.60

TABLE IX

DELAY OVERHEAD OF OUR IMPROVED CIRCUIT PROTECTION APPROACH

The dynamic power is proportional to the switching capacitance and the square of voltage swing value. Therefore, to estimate the power overhead associated with our improved circuit protection approach we calculate the effective node capacitance (C_{eff}) of a circuit. The voltage swing at the output of protecting gate (GP) of Figure 2 is 1.8V (i.e. from -0.4V to 1.4V) which is $1.8\times$ of the voltage swing at the output of protected gate (G) or any unprotected gate in a circuit. Thus, the node capacitance of the output node of the protecting gate is multiplied by the square of 1.8 before adding it to C_{eff}. In other words, C_{eff} is the total capacitance of the circuit normalized across the voltage swing of the protected and protecting gates. This helps in obtaining a better estimate of the power overhead. The effective node capacitances obtained for different designs are reported in Table XI. We have two different radiation hardened versions for each design and we can choose the best among them in terms of area or delay. In Table XI, Column 2 reports C_{eff} (in fF) of a regular area-mapped design. Column 3 reports C_{eff} of radiation-hardened area-mapped design with the best delay. Column 4 reports the percentage C_{eff} increase (or power overhead) for this design. Column 5 reports C_{eff} of the radiation-hardened area-mapped design with the best area and Column 6 reports the percentage capacitance increase for this design. Similarly, Column 7 reports C_{eff} (in fF) of a regular delay-mapped design. Column 8 reports C_{eff} of the radiation-hardened delay-mapped design with the best delay. Column 9 reports the percentage C_{eff} increase. Column 10 reports C_{eff} of the radiation-hardened delay-mapped design with the best area and Column 11 reports the percentage delay overhead for this design. We note that the circuit-level C_{eff} increase (or power overhead) of

	Area Mapping					Delay Mapping				
		Best Delay		Best Area			Best Delay		Best Area	
Ckt	Regular	$min(\eta^*, \eta')$	%Ovh.	$min(\eta^*, \eta')$	%Ovh.	Regular	$min(\eta^*, \eta')$	%Ovh.	$min(\eta^*, \eta')$	%Ovh.
alu2	1045.88	1418.28	35.61	1215.22	16.19	1397.26	1569.74	12.34	1569.74	12.34
alu4	1994.52	2470.09	23.84	2279.11	14.27	2470.09	2756.25	11.59	2756.25	11.59
C1355	1592.01	1994.52	25.28	1994.52	25.28	1728.9	2279.11	31.82	2279.11	31.82
C1908	1569.74	1994.52	27.06	1799.46	14.63	1799.46	2225.95	23.7	2225.95	23.7
C3540	3183.22	3916.26	23.03	3573.65	12.27	4022.1	4572.46	13.68	4515.84	12.28
C499	1569.74	1994.52	27.06	1994.52	27.06	1728.9	2279.11	31.82	2279.11	31.82
C880	1045.88	1418.28	35.61	1418.28	35.61	1397.26	1764	26.25	1764	26.25
dalu	2470.09	2996.47	21.31	2965.89	20.07	3310.85	3573.65	7.94	3573.65	7.94
des	9964.03	16842.85	69.04	13731.15	37.81	12139.63	17800.9	46.63	15490.29	27.6
frg2	1994.52	4201.63	110.66	3916.26	96.35	2611.21	4238.01	62.3	4147.36	58.83
i2	685.39	730.08	6.52	730.08	6.52	872.61	872.61	0	872.61	0
i3	495.51	670.81	35.38	600.25	21.14	495.51	600.25	21.14	600.25	21.14
i10	6037.29	12016.54	99.04	9304.53	54.12	7705.33	11054.42	43.46	11054.42	43.46
			41.50		29.33			25.59		23.75

TABLE X

AREA OVERHEAD OF OUR IMPROVED CIRCUIT PROTECTION APPROACH

	Area Mapping					Delay Mapping				
		Best Delay		Best Area			Best Delay		Best Area	
Ckt	Regular	$min(\eta^*, \eta')$	%Ovh.	$min(\eta^*, \eta')$	%Ovh.	Regular	$min(\eta^*, \eta')$	%Ovh.	$min(\eta^*, \eta')$	%Ovh.
alu2	1128.33	1438.01	27.45	1394.50	23.59	1451.52	1688.16	16.30	1688.16	16.30
alu4	2173.59	2544.65	17.07	2551.76	17.40	2685.13	3067.76	14.25	3067.76	14.25
C1355	1621.02	1731.34	6.81	1731.34	6.81	1864.59	1922.35	3.10	2370.35	27.12
C1908	1576.09	1873.24	18.85	1772.10	12.44	1865.07	2287.86	22.67	2287.86	22.67
C3540	3589.63	4269.24	18.93	4341.12	20.94	4408.19	5193.34	17.81	4788.92	8.64
C499	1621.02	1731.34	6.81	1731.34	6.81	1864.59	1922.35	3.10	1922.35	3.10
C880	1218.94	1766.32	44.91	1766.32	44.91	1468.59	1823.02	24.13	1823.02	24.13
dalu	2836.04	3149.19	11.04	3220.33	13.55	3645.71	3798.04	4.18	3798.04	4.18
des	10778.04	14816.73	37.47	14205.61	31.80	13276.49	19643.34	47.96	14741.34	11.03
frg2	2175.90	4521.89	107.82	4655.13	113.94	2816.91	4262.64	51.32	5821.60	106.67
i2	780.24	793.24	1.67	793.24	1.67	844.29	895.10	0.71	895.10	6.02
i3	472.52	600.99	27.19	574.13	21.50	479.15	582.68	21.61	582.68	21.61
i10	6674.11	11696.77	75.26	11458.16	71.68	8411.67	11112.62	32.11	11112.62	32.11
AVG			30.87		29.77			19.94		22.91

TABLE XI

ESTIMATED POWER OVERHEAD OF OUR IMPROVED CIRCUIT PROTECTION APPROACH

our improved circuit protection algorithm is as low as 19.94% on average for delay mapped designs, and about 29.77% for area mapped designs. The leakage power overhead of our approach is little higher but it can be reduced by increasing the threshold voltages of devices used in protected gate, protecting gate and the devices used for clamping. As a result of this the performance of our gate hardening approach will degrade slightly. However, the performance can be improved by increasing the devices sizes. Also, the leakage currents are generally higher for the process we used in our experiments. Recently, with the advances in process technology, the leakage currents have reduced [33]. Therefore, for these newer processes, our approach will yield low leakage power overheads.

V. Conclusion

In this paper, we have presented a novel circuit design approach for radiation hardened digital electronics. Our approach uses shadow gates to protect the primary gate in case it is struck by radiation. We locally duplicate the gate to be protected, and connect a pair of diode-connected transistors (or diodes) between the outputs of the original and shadow gates. These transistors turn on when the voltages of the two gates deviate during a radiation strike. The delay overhead of our approach per library gate is about 1.76%. The area overhead of our approach is 277% per library gate.

In addition, we present variable depth protection approach to perform *circuit-level radiation hardening with very low delay and area overheads*. In this approach, we minimize the number of gates that need to be protected in the manner described

above. The resulting circuit is made radiation hard, with a very low area and delay penalty (28% and 3% on average, for delay mapped designs) compared to an unprotected circuit. In practice, however, a very small fraction of gates need to be protected.

We also present another approach which reduces the area and delay penalty based on the desired cost function. With our improved circuit protection algorithm, radiation tolerant circuits are obtained with a very low area penalty as low as 23.75% and a delay penalty as low as -0.14% on average. We anticipate that our approach could be used in memory elements, or even the gates that drive memory elements. In this way, our approach can protect both combinational and sequential circuits from SEU events.

In the future, we plan to incorporate radiation hardening into the technology mapping step.

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