Efficient Analytical Determination of the SEU-induced Pulse Shape

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***Abstract*— Single event upsets (SEUs) have become problematic for both combinational and sequential circuits in the deep sub-micron era due to device scaling, lowered supply voltages and higher operating frequencies. To design radiation tolerant circuits efficiently, techniques are required to analyze the effects of a radiation particle strike on a circuit early in the design flow, and hence evaluate the circuit's resilience to SEU events. For an accurate estimation of the SEU tolerance of a circuit, it is important to consider the effects of electrical masking. This is typically done by performing circuit simulations, which are slow. In this paper, we present an analytical model for the determination of the shape of radiation-induced voltage glitches in combinational circuits. The output of our approach can be propagated to the primary outputs of the circuit using existing tools, thereby modeling the effects of electrical masking. This enables an accurate and quick evaluation of the SEU robustness of a circuit. Experimental results demonstrate that our model is very accurate, with a very low root mean square percentage error in the estimation of the shape of the voltage glitch of (4.5%) compared to SPICE. Our model gains its accuracy by using a non-linear model for the load current of the gate, and by considering the effect of τ_β on the radiation induced voltage glitch. Our analytical model is very fast (275$\times$ faster than SPICE) and accurate, and can therefore be easily incorporated in a design flow to estimate the SEU tolerance of circuits early in the design process.**

I. Introduction

Single event upsets (SEUs) (or single even transients (SETs)) have become increasingly problematic for both combinational and sequential VLSI circuits in the deep sub-micron (DSM) era [1], [2], [3], [4]. This is due to continuously decreasing feature sizes, lower supply voltages and higher operating frequencies which cause a reduction in the noise margins of VLSI designs. Many critical applications such as biomedical, space and military electronics demand reliable circuit functionality. Therefore, the circuits used in these application must be hardened so that they can provide reliable operation in the presence of radiation particles.

Circuit hardening approaches [5], [6] often employ selective gate hardening to reduce the area and delay overhead associated with the hardening approach. This is achieved by only protecting those gates in the circuit which are the significant contributers to the soft error failure rate of the circuit. Such gates in the circuit are identified based on three masking factors: logical, electrical and temporal masking [3], [5]. Out of these masking factors, both logical and temporal masking can be obtained without electrical simulations [3], [5]. However, electrical masking of a gate G in the circuit heavily depends upon the electrical properties of all the gates along any sensitized path from the output of G to a primary output of the circuit. Thus, electrical (SPICE) simulations are required to determine electrical masking effects in the circuit. For efficient circuit hardening, it is important to consider the effects of all these three masking factors and hence circuit simulations are required. Another reason for the need of the circuit simulations is that when a voltage glitch propagates through the circuit, the pulse width of the voltage glitch can increase, resulting in pulse spreading [7]. With circuit simulations, it will be possible to accurately obtain the glitch width at the primary output of the circuit. This is important for system level circuit hardening approaches [8], [9], [10] which use information about the radiation induced voltage glitch at the primary output for soft error detection and tolerance mechanisms. Therefore, techniques are required to analyze and simulate a circuit early in the design flow, and evaluate its resilience to SEU/SET events. Based on the results of this analysis, circuit hardening approaches can be implemented to achieve the level of protection required (while satisfying area, delay and power constraints) while taking masking factors into consideration to reduce overheads. This will help in reducing the number of design iterations. However, this can be practically achieved only if these analysis techniques can quickly and accurately simulate the SETs for different particle energies and for different gates with different input states.

An exhaustive SPICE based simulation of SET events in a circuit would be accurate; however it would require a large number of simulations since the circuit can have a large number of gates and a radiation particle strike can occur at *any* one of these gates (which can have any input state). Also, the transient pulse resulting from an SEU event depends upon the node capacitance and the sizing characteristics of the gate driving that node, the amount of charge dumped by a radiation particle strike and the state of the circuit inputs. Therefore, it is computationally intractable to use SPICE-like simulators to simulate the effect of SET events at early stages in the design flow. Thus, there is a need for efficient and accurate models/simulators for SET events in combinational circuits. These simulators should quickly estimate the shape of the voltage glitch at the node where the radiation particle strikes, and then propagate the effect of voltage glitch to the primary outputs of the circuit.

The current pulse that results from a radiation particle strike is traditionally described as a double exponential function [11], [12]. The expression for the pulse is

$$i_{seu}(t) = \frac{Q}{(\tau_\alpha - \tau_\beta)}(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}) \quad (1)$$

Here Q is the amount of charge deposited as a result of the ion strike, while τ_α is the collection time constant for the junction and τ_β is the ion track establishment time constant. The time constants τ_α and τ_β depend upon several process related parameters, and typically τ_α is of the order of 200ps and τ_β is of the order of tens of picoseconds [5], [4].

In this paper, we present an analytical model for the radiation induced transients in combinational circuits. Our model efficiently estimates the shape of the voltage pulse or glitch that results from a radiation particle strike. The voltage glitch estimated by our analytical model can be propagated to the primary outputs of the circuit using a voltage glitch propagation tool such as [13][1]. Since there exists previous work to address glitch propagation, it is not addressed in the current work. The properties of the voltage glitch (such as the magnitude, glitch shape and pulse width) at the primary output can be used to evaluate the SEU/SET robustness of the circuit. Based on the result of this analysis, circuit hardening approaches can be implemented to achieve the level of SET tolerance required.

The main contributions of this paper are:

- We present a closed-form analytical expression to compute the shape of the voltage glitch induced by a radiation particle strike. Although not addressed in this paper, this voltage glitch can be propagated to the primary outputs of the circuit to measure the SEU robustness of the circuit.
- We use a model for the load current $I^G_{out}(V_{in}, V_{out})$ or the output terminal current) of the gate G to increase the analysis accuracy. In contrast, the existing approaches [14], [13] model

[1]We are currently developing a more accurate voltage glitch propagation tool

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the electrical behavior of the gate using a linear RC circuit. The load current model of the gate is also more accurate than the transistor I_{DS} model used in [15] for the SET analysis.
- Our model can be used for any combinational gate.
- The model can be used for the analysis of SET events on arbitrarily sized gates with different loading, and for arbitrary values of deposited charge.
- In contrast to [14], [13], we consider the effect of the ion track establishment constant (τ_β) of the radiation particle induced current pulse. This improves the accuracy of our method.

It was reported in [15], through SPICE simulations, that ignoring τ_β results in an under-estimation of the pulse width of the voltage glitch by 10%. Therefore, neglecting the contribution of the τ_β term of the current pulse of Equation 1 diminishes the severity of the radiation particle strike, and hence leads to an optimistic estimate for the voltage glitch. In other words, the magnitude and the pulse width of the voltage glitch that is estimated can be lower than the actual values. Therefore, ignoring τ_β (as done by [14], [13]) for SEU/SET tolerance analysis and for circuit hardening, can lead to an optimistic design. Hence, the system can fail in the event of a radiation particle strike. In this paper, we consider the effect of τ_β on the radiation induced current pulse, and also use a non-linear model for the load current of a gate, to increase the analysis accuracy. The root mean square error in the estimation of the shape of the voltage glitch using our approach is 4.5% (compared to SPICE based simulation).

II. Previous Work

The simulation and analysis of SEU-induced transients has been a topic of interest for many years. Much work has been done on this topic for combinational and sequential circuit elements [16], [1], [2], [14], [17], [18], [13]. Most of this work can be classified under three categories: device-level, circuit-level and logic-level.

Device based simulation approaches [19], [20] perform three-dimensional numerical simulation to evaluate the effect of a radiation particle strike by solving device physics equations. Although such approaches result in a very accurate analysis, they are extremely time-consuming in nature. Also, these techniques provide very little direct insight into the problem of circuit hardening.

For circuit-level and logic-level simulation approaches, a double exponential current pulse (Equation 1) is used to model a particle strike [11], [18], [6]. Logic-level based approaches [17], [21] are utilized when the speed of analysis is more critical than the accuracy of the analysis. In these approaches, the electrical nature of transient faults are abstracted into logic-level models, which are then used in gate-level timing simulations to propagate the effects of particle strikes to the memory elements at the outputs of the circuit. The large inaccuracy of these approaches makes them unattractive for robustness evaluation of circuits under SEU transients.

Circuit-level simulation approaches provide accuracy and runtimes which are intermediate between device and logic based methods. As mentioned in Section I, SPICE based circuit simulation provides an accurate analysis, however it is still very time consuming since a large number of simulations are required to be performed due to the reasons mentioned in Section I. In [22], the authors presented a methodology to analyze compound noise effects in circuits by using look-up tables and a database generated using SPICE simulations of all the cells in a library. An iterative approach for soft error rate analysis of combinational circuits (while accounting for electrical masking) is reported in [23]. As the approach of [23] estimates the effects of a radiation particle strike iteratively, the speedup obtained over SPICE simulations is not high. Many approaches [24], [13], [14] attempt to solve a non-linear differential equation (this equation is called Ricatti differential equation) of the transistor to obtain a closed-form expression for SEU-induced transients. However, due to the non-linear nature of the differential equation, it is not possible to obtain a closed-form solution. Thus, many approximations have been proposed to model SEU transients. The authors of [24] presented an exact solution of the Ricatti equation using a computationally expensive infinite power series solution. In [13], a switch-level simulator is presented to simulate faults induced by radiation particle strikes. The simulator uses a linear RC gate model to simplify the analysis. In [14], a closed-form model is reported for SEU induced transient simulation for combinational circuits. Again, a linear RC gate model is used, which is derived using a SPICE-based calibration of logic gates for a range of values of fanout, charge deposited and scale factor. In [14], [13], the circuit simulation approaches *assume a linear RC gate model* which is not a valid assumption as will be explained in Section III. Also, these approaches neglect the contribution of the ion track establishment constant (τ_β) of the SEU-induced current pulse of Equation 1, which further increases the inaccuracy in the analysis. Recently, an analytical model for the estimation of the pulse width of the voltage glitch induced by a radiation particle strike in combinational circuits was reported in [15]. The approach of [15] is only able to predict the pulse width of the voltage glitch induced by a radiation particle. The current model used in [15] is not very accurate due to which the inaccuracy in the pulse width estimation is sometimes high (as high as 10%). Also, this approach *cannot predict the shape of the voltage glitch* which is required for efficient circuit hardening as explained in Section I. In contrast to this, we uses a more accurate current model of a gate and our approach can accurately predict the *shape* of the voltage glitch induced by a radiation particle strike. Our model can also compute the pulse width of the voltage glitch. Also, our model incorporates the contribution of τ_β.

Orthogonal to the analysis of SEU-induced transients, a great deal of research has been conducted on circuit-level modeling and simulation for static timing analysis (STA) [25] and static noise analysis (SNA) [26]. The approaches for STA [25] and SNA [26] are iterative, and hence sometimes require a large number of iterations to converge. Thus, the speedup obtained by such iterative approach is not high (the speedup of [25] is 3-70× and [26] is 20× compared to SPICE), and also varies in a wide range depending upon the simulation scenario. In contrast to these iterative approaches, our analytical approach is *at least* 275× faster compared to SPICE.

III. Our Approach

In Section III-A, we classify the radiation-induced transient into 4 cases based on the magnitude of the voltage glitch induced by a radiation particle strike. Our model for a radiation-induced voltage glitch, based on these cases, is introduced in Section III-B. In Section III-C, we provide details about our method to determine the shape of the radiation-induced voltage glitch.

A. Classification of Radiation Particle Strikes

The analysis presented in this paper is for an inverter with its input at VDD and its output at GND. The radiation particle strike results in a positive voltage glitch at the output of the gate. However, the same analysis and the same analytical model can be used for any type of gate (NAND, NOR, etc), with any logic values applied to its inputs. The handling of NAND, NOR, etc. gates is achieved by constructing an equivalent inverter for the gate. The size of this inverter depends on the given input values of the gate. The applicability of our model to different gates is verified by applying our model to a 2-input NAND gate (for all four input combinations) and 3-input NOR gate (for all eight input combinations). These results are presented in Section IV. Note that for multiple input gates, we do not consider the radiation particle strike at intermediate nodes of the gate, because the worst-case transient occurs when the particle strike occurs at the output node of the gate. Therefore, the estimate of the voltage glitch at the output node of the gate due to a particle strike at any intermediate node will not be useful for circuit hardening. Hence, in our analysis, we do not consider the cases where the radiation particle strike occurs at intermediate nodes of multi-input gates.

Consider four identical inverters as shown in Figure 1 (a). These inverters are implemented using a 65nm PTM [27] model card with VDD=1V. Let node a be at logic value 0 when a radiation particle strikes the diffusion of INV1. This is modeled by the injection of $i_{seu}(t)$ (described by Equation 1) at node a. The voltage glitch that results from the radiation particle strike is shown in Figure 1 (b) for four different inverter sizes (1X, 4X, 5X and 6X) and for Q=100fC, τ_α = 200ps and τ_β = 50ps. From Figure 1 (b), we observe that INV1

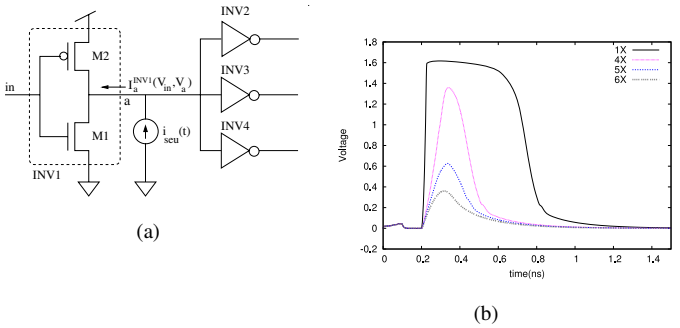


Fig. 1. a) SEU current injected at the output of inverter INV1, b)Voltage glitch at node a

can operate in 4 different *cases* during the radiation event transient, based on the maximum voltage glitch magnitude V_{GM}. Note that the value of V_{GM} depends upon the sizes of the devices M1 and M2, the gate loading at the output node a and the value of Q, τ_α and τ_β. The classification of INV1 operating in different cases is as follows. If an SEU event results in a maximum voltage glitch of magnitude $V_{GM} \geq VDD$ + 0.6V, we refer to this as Case 1. If $VDD + |V_{TP}| \leq V_{GM} < VDD + 0.6V$, then we call this Case 2. If V_{GM} is greater or equal to $VDD/2$ and less than $VDD + |V_{TP}|$, this condition is referred to as Case 3. For $V_{GM} < VDD/2$, we have Case 4. Out of these 4 cases, Case 4 corresponds to a voltage glitch of magnitude less than $VDD/2$ and hence the radiation event does not result in a logic flip at the node. For other regions, the radiation event causes a logic flip, and hence we present our analysis for these cases (i.e. for Cases 1, 2 and 3). The shape of the voltage glitch is computed differently for different cases, due to the different behavior of M1 and M2 (Figure 1 (a)) for these cases. The description of Cases 1, 2 and 3 is summarized below:

- Case 1: In this case, with the increasing voltage of node a (V_a), M1 starts conducting in the linear region and enters the saturation region when the V_a becomes more than V_{dsat}^N. M2 starts conducting in the saturation mode once V_a crosses $VDD + |V_{TP}|$. Eventually when V_a reaches VDD + 0.6V, the voltage between the source diffusion and the bulk terminal of the PMOS transistor M2 becomes $\geq$ 0.6V. Therefore, the diode between these two terminals get forward biased and it starts conducting heavily. Thus V_a gets clamped to a value around VDD + 0.6V.
- Case 2: In this case as well, both M1 and M2 conduct similar to Case 1. However, the diode between the diffusion and the bulk terminals of M2 remains off.
- Case 3: Only M1 conducts in this case. M1 starts conducting in the linear region and when V_a crosses V_{dsat}^N, M1 enters the saturation region. M2 remains off in this case.

Based on the above discussion, we note that inverters of four different sizes operate quite differently during the radiation-induced transient, and the maximum voltage glitch magnitude (V_{GM}) determines their behavior at different times during the transient. Therefore, *it will not be accurate to model INV1 by a linear RC gate model*, as in the case [14], [13]. Also, it will be inaccurate to model the load current of INV1 (during the radiation induced transient) at the transistor current of M1 (as modeled by [15]) since M2 also conducts in Cases 1 and 2.

B. Overview of Our Model for Determining the Pulse Shape of the Voltage Glitch

Figure 2(a) (shown at the top left portion of Figure 2) schematically illustrates a voltage glitch that results from a radiation strike at the output node a of INV1. As shown in Figure 2(a), the node voltage rises and reaches V_{dsat}^N at time T_{sat}^1, $VDD/2$ at time t_1, $VDD + |V_{TP}|$ at time T_P^1 (for Cases 1 and 2), and then after reaching a maximum value of V_{GM}, the node voltage falls to $VDD + |V_{TP}|$ at time T_P^2 (for Cases 1 and 2), $VDD/2$ at time t_2 and finally to V_{dsat}^N at the time T_{sat}^2. Hence the shape of the voltage glitch of Figure 2(a) is defined by the node a voltage equations between the time intervals: (0, T_{sat}^1), {(T_{sat}^1, T_P^1), (T_P^1, T_P^2) and (T_P^2, T_{sat}^2)} for Cases 1 and 2 or (T_{sat}^1, T_{sat}^2) for Case 3, and (T_{sat}^2,∞) for all cases. Our goal is to compute all the variables which define these time intervals, and also the node voltage equations of node a corresponding to these time durations. We can also compute t_1 and t_2 to obtain the width of the voltage glitch of Figure 2(a) (the width of the voltage glitch is $t_2 - t_1$). Before we can use our analytical model, we characterize all the gates in our library using the same approach as reported in [25]. For each gate (for all input combinations), we compute the load current of the gate ($I_{out}(V_{in}, V_{out})$) as a function of its output node voltage, and store this in a look-up table. We also compute the input gate capacitance C_G (the output node diffusion capacitance C_D) as a function of the input (output) node voltage and store them in a look-up table. For these look-up table entries, we discretize the voltages in steps of 0.1V. For example, for INV1 of Figure 1, we compute $I_a(V_{in}, V_a)$ through output terminal a for different V_a voltage values at a, when the input node in is at VDD and GND ($V_{in} = VDD$ and $V_{in} = GND$). Thus, the number of current look-up tables for any gate is equal to 2^n (where n is the number of inputs of a gate). Similarly, C_D is also computed depending upon the input state of the gate. Therefore, for an n-input gate, the total size of the look-up tables for C_G is $23 \cdot n$, C_D is $17 \cdot 2^n$ and load current I_{out} is $17 \cdot 2^n$. This step is performed once for each gate in a library and thus it does not affect the runtime of our model. Also, n is typically ≤ 3, hence these lookup tables are quite tractable in size. The saturation voltage (V_{dsat}) is obtained using SPICE [28].

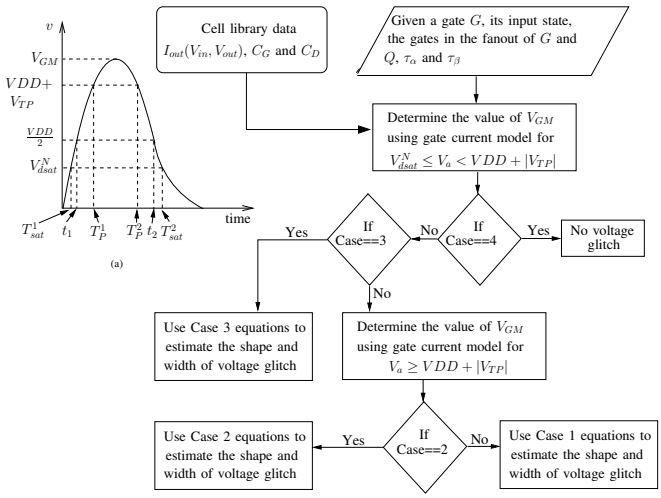


Fig. 2. Flowchart of our model for Pulse Width Calculation

Figure 2(b) shows the flowchart of our algorithm to compute the shape and the width of the voltage glitch. The input to our model is a gate G (the radiation event is to be simulated at the output node of gate G), its input state, the list of gates which are driven by the gate G, and the values of Q, τ_α and τ_β. Our algorithm first computes V_{GM} using the gate current model for $V_{dsat}^N < V_a < VDD + |V_{TP}|$ and then determines the case that is applicable. If $V_{GM} < VDD/2$ (i.e. Case 4 applies), then there is no voltage glitch reported. Otherwise if $V_{GM} < VDD + |V_{TP}|$ then Case 3 applies and we use Case 3 equations to obtain the shape and the width of the voltage glitch else we again compute V_{GM} using gate current model for $V_a > VDD + |V_{TP}|$. Based on this new value of V_{GM}, the operating case of gate G can be found (either Case 1 or Case 2) and then the corresponding case equations are used to compute the shape and the width of the voltage glitch. The steps of our algorithm are explained in the following sub-sections.

C. Derivation of Our Model for Determining the Shape of the Voltage Glitch

As mentioned earlier, the analysis presented in this paper is for INV1 (Figure 1) with its input node in at VDD and the output node a at GND. A radiation particle strike results in a positive voltage glitch at node a. To ensure that the model for radiation events in combinational circuit elements is manageable, we simplify the load current model $I_a^{INV1}(V_{in}, V_a)$ of INV1. Note that in the following

analysis we use $I_a^{INV1}(V_a)$ instead of $I_a^{INV1}(V_{in}, V_a)$ since the analysis is presented for $V_{in} = VDD$. With the input terminal of INV1 at VDD, $I_a^{INV1}(V_a)$ can be written as:

$$I_a^{INV1}(V_a) = \begin{cases} V_a/R_n & V_a < V_{dsat}^N \\ K_3 + K_4 \cdot V_a & V_{dsat}^N \leq V_a < VDD + |V_{TP}| \\ K_5 + K_6 \cdot V_a & VDD + |V_{TP}| \leq V_a < VDD + 0.6V \end{cases}$$

Here, R_n is the linear region resistance of M1 (since M2 is off in this region), which is calculated using the $I_a^{INV1}(V_a)$ versus V_a lookup table for V_a values less than V_{dsat}^N. The constants K_3 and K_4 are obtained by using a linear equation for the points $I_a^{INV1}(V_a)$ versus V_a from the lookup table for V_a values greater than V_{dsat}^N and less than $VDD + |V_{TP}|$. When $V_a > VDD + |V_{TP}|$, $I_a^{INV1}(V_a)$ increases super-linearly with V_a because both M1 and M2 are ON. Thus, the constants K_5 and K_6 are obtained by fitting a least square line to the points (V_a, $I_a^{INV1}(V_a)$) from the lookup table for V_a values greater than $VDD + |V_{TP}|$ and less than $VDD + 0.6V$.

To determine the applicable case, we first need to find V_{GM}. The method of finding V_{GM} is described next.

1) Voltage glitch magnitude V_{GM}: A radiation event can result in a node voltage flip only if $I_{seu}^{max} > I_a^{INV1}(VDD/2)$, where I_{seu}^{max} is the maximum value of SEU-induced current pulse of Equation 1. This is a necessary condition which is used to check whether a radiation event will result in a significant voltage glitch or not. The differential equation for the radiation-induced voltage transient at the output of INV1 of Figure 1 is given by:

$$C\frac{dV_a(t)}{dt} + I_a^{INV1}(V_a) \quad = \quad i_{seu}(t) \tag{2}$$

where, C is the capacitance[2] at node a. The above equation can be integrated with the initial condition $V_a(t) = 0$ at $t = 0$ to obtain $V_a(t)$. For deep sub-micron processes, V_{dsat} is much lower than $V_{GS} - V_T$ due to short channel effects. For the 65nm PTM [27] model card used in this paper, V_{dsat} for both NMOS and PMOS transistors is lower than $VDD/2$. Therefore, to obtain the V_{GM} value, we first integrate Equation 2 from the initial condition and using $I_a^{INV1} = V_a/R_n$ till V_a reaches the V_{dsat}^N value. Then we again integrate Equation 2 using $I_a^{INV1}(V_a) = K_3 + K_4 \cdot V_a$ to obtain the $V_a(t)$ expression. Then, we find the maximum value V_{GM} attained by this $V_a(t)$ expression. If $V_{GM} < VDD + |V_{TP}|$ then INV1 is operating in Case 3. Otherwise, INV1 in operating in either Case 1 or Case 2[3]. The methodology to decide between Cases 1 and 2 is explained later. Now integrating Equation 2 using $I_a^{INV1}(V_a) = V_a/R_n$ and with the initial condition $V_a(t) = 0$ at $t = 0$, we get:

$$V_a(t) = \frac{I_n}{C}\left(\frac{e^{-t/\tau_\alpha}}{X} - \frac{e^{-t/\tau_\beta}}{Y} - Ze^{-t/R_nC}\right) \tag{3}$$
$$where \;\; X = \frac{1}{R_nC} - \frac{1}{\tau_\alpha}, Y = \frac{1}{R_nC} - \frac{1}{\tau_\beta},$$
$$I_n = \frac{Q}{\tau_\alpha - \tau_\beta} \;\&\; Z = \frac{1}{X} - \frac{1}{Y}$$

To obtain the time T_{sat}^1 when $V_a(t)$ reaches the V_{dsat}^N value from Equation 3, we linearly expand Equation 3 around the initial guess T_{sat}^{1a}. The expression for T_{sat}^1 thus obtained is:

$$T_{sat}^1 = T_{sat}^{1a} + \frac{V_{dsat}^N - \frac{I_n}{C}\left(\frac{e^{-T_{sat}^{1a}/\tau_\alpha}}{X} - \frac{e^{-T_{sat}^{1a}/\tau_\beta}}{Y} - Ze^{-T_{sat}^{1a}/R_nC}\right)}{\frac{I_n}{C}\left(-\frac{e^{-T_{sat}^{1a}/\tau_\alpha}}{\tau_\alpha X} + \frac{e^{-T_{sat}^{1a}/\tau_\beta}}{\tau_\beta Y} + \frac{Z}{R_nC}e^{-T_{sat}^{1a}/R_nC}\right)} \tag{4}$$

To obtain the initial guess T_{sat}^{1a}, we approximate the rising part of the SEU-induced current by a line between the origin and the point where $i_{seu}(t)$ of Equation 1 reaches its maximum value I_{seu}^{max}. The SEU-induced current $i_{seu}(t)$ reaches I_{seu}^{max} at T_{seu}^{max}. Then we substitute this approximated SEU current in the RHS of Equation 2 and integrate it from the initial condition $V_a(t) = 0$ at $t = 0$ to $V_a(t) = V_{dsat}^N$ at $t = T_{sat}^{1a}$ using $I_a^{INV1}(V_a) = V_a/R_n$. After this we solve for T_{sat}^{1a} by performing a quadratic expansion of the resulting equation around the origin. The expression we get for T_{sat}^{1a} is not reported for brevity.

So far we know T_{sat}^1, the time when $V_a(t)$ reaches V_{dsat}^N, or the time when M1 enters the saturation mode. Now we again integrate Equation 2 with the initial condition $V_a(t) = V_{dsat}^N$ at $t = T_{sat}^1$, and using $I_a^{INV1}(V_a) = K_3 + K_4 \cdot V_a$. The expression we get for $V_a(t)$ is:

$$V_a(t) = \frac{I_n}{C}\left(\frac{e^{-t/\tau_\alpha}}{X'} - \frac{e^{-t/\tau_\beta}}{Y'}\right) - \frac{K_3}{K_4} + Z'e^{-K_4t/C} \tag{5}$$
$$where \;\; X' = \frac{K_4}{C} - \frac{1}{\tau_\alpha}, Y' = \frac{K_4}{C} - \frac{1}{\tau_\beta}$$
$$Z' = V_{dsat}^N e^{K_4T_{sat}^1/C} - \frac{I_n}{C}e^{K_4T_{sat}^1/C}\left(\frac{e^{-T_{sat}^1/\tau_\alpha}}{X'} - \frac{e^{-T_{sat}^1/\tau_\beta}}{Y'}\right) + \frac{K_3}{K_4}e^{K_4T_{sat}^1/C}$$

To calculate the value of V_{GM}, first we differentiate Equation 5 and equate $dV_a(t)/dt$ to zero and solve for $T_{V_{GM}}$ (the time at which $V_a(t)$ reaches its maximum value). Since the equation $dV_a(t)/dt = 0$ is also transcendental equation, hence we linearly expand $dV_a(t)/dt = 0$ around $T_{V_{GM}}^a$ and solve for $T_{V_{GM}}$. We get:

$$T_{V_{GM}} = T_{V_{GM}}^a + \frac{\frac{e^{-T_{V_{GM}}^a/\tau_\alpha}}{\tau_\alpha X'} - \frac{e^{-T_{V_{GM}}^a/\tau_\beta}}{\tau_\beta Y'} + \frac{K_4Z'}{C}e^{-K_4T_{V_{GM}}^a/C}}{\frac{e^{-T_{V_{GM}}^a/\tau_\alpha}}{\tau_\alpha^2 X'} - \frac{e^{-T_{V_{GM}}^a/\tau_\beta}}{\tau_\beta^2 Y'} + \frac{K_4^2Z'}{C^2}e^{-K_4T_{V_{GM}}^a/C}} \tag{6}$$

Now, we calculate V_{GM} by substituting $T_{V_{GM}}$ obtained from Equation 6, in to Equation 5. If $V_{GM} < VDD/2$ then Case 4 applies and the radiation event does not flip the logic level of the affected node. If $VDD/2 \leq V_{GM} < VDD + |V_{TP}|$, then Case 3 is applicable. Otherwise, either Case 1 or Case 2 is applicable. Before we describe the methodology to decide between Case 1 and Case 2, we will first discuss the method to obtain the value of $T_{V_{GM}}^a$.

Note that the output node voltage of INV1 i.e. $V_a(t)$ of Equation 5 always attains its maximum value after T_{seu}^{max} (the time $i_{seu}(t)$ of Equation 1 reaches its maximum value I_{seu}^{max}). Therefore, we integrate Equation 2 using a linear model ($i_{seu}^m(t)$) for radiation-induced current for time $t > T_{seu}^{max}$ and with the initial condition $V_a(t) = V_a^{sm}$ at $t = T_{seu}^{max}$ obtained from Equation 5. The radiation-induced linear current model $i_{seu}^m(t)$ has one of its end-points I_{seu}^{max} at a time value of T_{seu}^{max}. The other end-point has its current value as 0, and its time value t^* is obtained by equating the charge deposited by the actual SEU current $i_{seu}(t)$ from time T_{seu}^{max} to ∞ and the charge deposited by the linearized radiation-induced current equation. Hence the expression for the radiation-induced linear current model is:

$$i_{seu}^m(t) = I_{seu}^{max}\left(1 - \frac{t - T_{seu}^{max}}{t^* - T_{seu}^{max}}\right) = P + Mt \tag{7}$$

Now we substitute $i_{seu}^m(t)$ for $i_{seu}(t)$ in Equation 2, use $I_a^{INV1}(V_a) = K_3 + K_4 \cdot V_a$ and then integrate. After this we differentiate the resulting equation for $V_a(t)$ and equate $dV_a(t)/dt$ to zero and solve for $T_{V_{GM}}^a$.

Deciding between Case 1 and Case 2: Before we can decide whether INV1 is operating in Case 1 or Case 2, first we need to compute the time t_1 when $V_a(t)$ reaches $VDD/2$ and then we have to compute T_P^1 (the time when $V_a(t)$ reaches $VDD + |V_{TP}|$) using t_1. After this, we will integrate Equation 2 using the initial condition $V_a(t) = VDD + |V_{TP}|$ at $t = T_P^1$ and $I_a^{INV1}(V_a) = K_5 + K_6 \cdot V_a$ to obtain the expression for $V_a(t)$. Then this expression of $V_a(t)$ will be used to decide between Cases 1 and 2 using the V_{GM} value. As shown in the flowchart of our algorithm in Figure 2, the method to compute t_1 is identical for cases 1, 2 or 3. Therefore, the value of t_1 will also be useful for the estimation of the pulse width of the voltage glitch induced. To obtain the expression for t_1, we substitute $t = t_1$ and $V_a(t_1) = VDD/2$ in Equation 5 and then solve for t_1 after expanding it linearly around the point t_1^a (which is an initial guess for t_1). Here $t_1^a = T_{sat}^1 VDD/(2V_{dsat}^N)$. The expression for t_1 is therefore:

[2]The value of C is obtained by the addition of the average value of $n \cdot C_G$ and C_D over the operating voltage range. The factor of n occurs due to the fact that we assume a fanout of n.

[3]In Cases 1 and 2, both M1 and M2 conduct and hence INV1 load current model $K_5 + K_6 \cdot V_a$ is used to accurate value of V_{GM}. This new value of V_{GM} is used to decide between Cases 1 and 2.

$$t_1 = t_1^a + \frac{\frac{e^{-t_1^a/\tau_\alpha}}{X'} - \frac{e^{-t_1^a/\tau_\beta}}{Y'} + \frac{C}{I_n}(Z'e^{-K_4 t_1^a/C} - \frac{K_3}{K_4} - \frac{VDD}{2})}{\frac{e^{-t_1^a/\tau_\alpha}}{X'\tau_\alpha} - \frac{e^{-t_1^a/\tau_\beta}}{Y'\tau_\beta} + \frac{K_4 Z'}{I_n}e^{-K_4 t_1^a/C}} \quad (8)$$

Then we compute the time $t = T_P^1$ when $V_a(t)$ reaches $VDD + |V_{TP}|$ since the load current model of INV1 changes at this time instant. To obtain T_P^1, we repeat the same steps as we followed for the derivation of the t_1 expression with the condition $V_a(t) = VDD + |V_{TP}|$ at $t = T_P^1$ in Equation 5 and with the initial guess $T_P^{1a} = t_1 + (VDD + |V_{TP}| - V_{dsat}^N)/(VDD/2 - V_{dsat}^N)$. The expression for T_P^1 is therefore similar to Equation 8 with t_1^a replaced by T_P^{1a}, t_1 by T_P^1 and $VDD/2$ by $VDD + |V_{TP}|$.

Now we integrate Equation 2 with the initial condition $V_a(t) = VDD + |V_{TP}|$ at $t = T_{sat}^1$, and using $I_a^{INV1}(V_a) = K_5 + K_6 \cdot V_a$. The expression we get for $V_a(t)$ is:

$$V_a(t) = \frac{I_n}{C}(\frac{e^{-t/\tau_\alpha}}{X''} - \frac{e^{-t/\tau_\beta}}{Y''}) - \frac{K_5}{K_6} + Z''e^{-K_6 t/C} \quad (9)$$

$$where \;\; X'' = \frac{K_6}{C} - \frac{1}{\tau_\alpha}, Y'' = \frac{K_6}{C} - \frac{1}{\tau_\beta}$$

$$Z'' = V_{dsat}^N e^{K_6 T_P^1/C} - \frac{I_n}{C}e^{K_6 T_P^1/C}(\frac{e^{-T_P^1/\tau_\alpha}}{X''} - \frac{e^{-T_P^1/\tau_\beta}}{Y''}) + \frac{K_5}{K_6}e^{K_6 T_P^1/C}$$

To calculate the value of the maximum value of $V_a(t)$ of Equation 9 i.e. V_{GM} (maximum glitch magnitude for Case 1 or Case 2), we have to repeat the same steps as we followed while calculating the maximum value of $V_a(t)$ of Equation 5. After we obtain the value of V_{GM}, we can decide whether the INV1 is operating in Case 1 or Case 2. Note that by using this method, V_{GM} can be evaluated to be greater than $VDD + 0.6V$, because the diode is not modeled in Equation 2. Therefore, if $V_{GM} > VDD + 0.6V$ then we set $V_{GM} = VDD + 0.6V$.

So far, we have obtained the expression for V_{GM} which can be used to determine the operating case of INV1. We also derived expressions for T_{sat}^1, t_1, T_P^1 and the INV1 output node voltage equations for different time durations (Equations 3, 5, 9).

2) Derivation of the expressions for Case 3: The derivation of the expressions for the shape and the pulse width of the voltage glitch is as follows. First, we derive the expression for t_2 i.e. the time when $V_a(t)$ falls to $VDD/2$ value. Note that in this case, only M1 of Figure 1 (a) conducts because the magnitude of the glitch voltage is less than $VDD + |V_{TP}|$. Therefore, Equation 5 describes the voltage of node a for all times t such that $T_{sat}^1 \leq t \leq T_{sat}^2$. The expression for t_2 can be obtained in similar manner as t_1 with the substitution t = t_2 and $V_a(t_2) = VDD/2$ in Equation 5 and with the initial guess point t_2^a. Based on our observation, we find that t_2^a (the time when $i_{seu}(t)$ falls to $I_{DS}^{VDD/2}$ after reaching I_{seu}^{max}) can be used as an initial guess for t_2 since the node voltage at that time will be close to $VDD/2$. We ignore the contribution of the e^{-t/τ_β} term of $i_{seu}(t)$ when calculating t_2^a. This is reasonable since τ_α is usually 3-4 times of τ_β and therefore e^{-t/τ_β} approaches 0 much faster than the e^{-t/τ_α} term. Thus the value of e^{-t/τ_β} around t_2^a (which is greater than T_{seu}^{max}) will be approximately equal to 0. The expression for t_2^a is $-\tau_\alpha \log I_{DS}^{VDD/2}/I_n$.

Now, we again substitute $t = T_{sat}^2$ and $V_a(T_{sat}^2) = V_{dsat}^N$ in Equation 5 and solve for T_{sat}^2 in a similar manner as solved for t_1 (Equation 8) using the initial guess T_{sat}^{2a}. The expression for T_{sat}^{2a} is $t_2 + V_{dsat}^N - 0.5 \cdot VDD/(dV_a(t)/dt|_{t=t_2})$.

To obtain the node a voltage equation for $t > T_{sat}^2$, we integrate Equation 2 with the initial condition $V_a(T_{sat}^2) = V_{dsat}^N$ and using $I_a^{INV1}(V_a) = V_a/R_n$. The expression we get is:

$$V_a(t) = \frac{I_n}{C}(\frac{e^{-t/\tau_\alpha}}{X} - \frac{e^{-t/\tau_\beta}}{Y} - A_p e^{(T_{sat}-t)/R_n C}) \quad (10)$$
$$where \;\; A_p = V_{dsat}^N - \frac{I_n}{C}(\frac{e^{-T_{sat}^2/\tau_\alpha}}{X} - \frac{e^{-T_{sat}^2/\tau_\beta}}{Y})$$

Now we can write the analytical expression of the voltage glitch induced by a radiation particle strike. The voltage glitch is described by a set of 3 equations (Equations 3, 5 and 10) as summarized below:

$$V_a(t) = \begin{cases} Eqn.\ 3 & t < T_{sat}^1 \\ Eqn.\ 5 & T_{sat}^1 \leq t \leq T_{sat}^2 \\ Eqn.\ 10 & t > T_{sat}^2 \end{cases}$$

3) Derivation of the expressions for Case 2: In this case, the magnitude of the voltage glitch V_{GM} is between $VDD + |V_{TP}|$ and $VDD + 0.6V$. Therefore, both M1 and M2 of INV1 conducts for the time t such that $T_P^1 \leq t \leq T_P^2$ and hence the node a voltage is described by Equation 9 (this equation was used to calculate V_{GM} value for cases 1 and 2). To obtain the value of T_P^2, substitute $V_a(T_P^2) = VDD + |V_{TP}|$ for $t = T_P^2$ in Equation 9 and then solve for T_P^2 by using T_P^{2a} as the initial guess. The expression for T_P^2 that we get is:

$$T_P^2 = T_P^{2a} + \frac{\frac{e^{-T_P^{2a}/\tau_\alpha}}{X''} - \frac{e^{-T_P^{2a}/\tau_\beta}}{Y''} + \frac{C}{I_n}B}{\frac{e^{-T_P^{2a}/\tau_\alpha}}{X''\tau_\alpha} - \frac{e^{-T_P^{2a}/\tau_\beta}}{Y''\tau_\beta} + \frac{K_6 Z''}{I_n}e^{-K_6 T_P^{2a}/C}} \quad (11)$$
$$where \quad B = Z''e^{-K_6 T_P^{2a}/C} - \frac{K_5}{K_6} - (VDD + |V_{TP}|)$$

The value of T_P^{2a} is obtained using the following observation. We observed that when $i_{seu}(t)$ becomes equal to the drain to source current (I_{DS}) of M1 of Figure 1 (a), then at that instant, the I_{DS} of M2 is approximately equal to 0 and the voltage at node a is $VDD + |V_{TP}|$. Thus, the value of T_P^{2a} is obtained by solving $I_a^{INV1}(VDD + |V_{TP}|) = i_{seu}(T_P^{2a})$ (since at this instant I_{DS} of M2 is zero therefore I_{DS} of M1 is equal to $I_a^{INV1}(VDD + |V_{TP}|)$). In this derivation, we ignore the contribution of the e^{-t/τ_β} term of $i_{seu}(t)$. The expression for T_P^{2a} is $-\tau_\alpha \log(I_a^{INV1}(VDD + |V_{TP}|)/I_n)$.

Now we calculate the node a voltage equation for time duration $T_P^2 \leq t \leq T_{sat}^2$. For this, we integrate Equation 2 with the initial condition $V_a(t) = VDD + |V_{TP}|$ at $t = T_P^2$, and using $I_a^{INV1}(V_a) = K_3 + K_4 \cdot V_a$. The resulting expression for $V_a(t)$ that we get is:

$$V_a(t) = \frac{I_n}{C}(\frac{e^{-t/\tau_\alpha}}{X'} - \frac{e^{-t/\tau_\beta}}{Y'}) - \frac{K_3}{K_4} + Z^* e^{-K_4 t/C} \quad (12)$$

$$where Z^* = (VDD + |V_{TP}|)e^{K_4 T_{sat}^1/C} - \frac{I_n}{C}e^{K_4 T_P^2/C}(\frac{e^{-T_P^2/\tau_\alpha}}{X'} - \frac{e^{-T_P^2/\tau_\beta}}{Y'}) + \frac{K_3}{K_4}e^{K_4 T_P^2/C}$$

Using Equation 12, we can obtain the values of t_2 and T_{sat}^2 for Case 2 in the same manner as t_2 and T_{sat}^2 were derived for Case3. After we obtained the values for t_2 and T_{sat}^2, the node a voltage equation for $t > T_{sat}^2$ is same as Equation 10 (with the values of t_2 and T_{sat}^2 calculated for this case). Now that we have derived all variables for this case, we can write the equation for the radiation induced voltage glitch at node a as shown below:

$$V_a(t) = \begin{cases} Eqn.\ 3 & t < T_{sat}^1 \\ Eqn.\ 5 & T_{sat}^1 \leq t < T_P^1 \\ Eqn.\ 9 & T_P^1 \leq t < T_P^2 \\ Eqn.\ 12 & T_P^2 \leq t \leq T_{sat}^2 \\ Eqn.\ 10 & t > T_{sat}^2 \end{cases}$$

4) Derivation of the expressions for Case 1: In this case, both M1 and M2 of Figure 1 (a) conduct similar to Case 2. However, when the voltage at node a reaches $VDD + 0.6V$ value, the diffusion diode between the node a and the bulk terminal of M2 gets forward biased and start conducting heavily. Thus $V_a(t)$ get clamped to a value around $VDD + 0.6V$. Therefore, all expressions derived for Case 2 are also applicable to this case with a slight modification to incorporate the effect of this clamping action. In this case, when Equation 9 computes a value greater than $VDD + 0.6V$ for any time t then we set the node a voltage value to $VDD + 0.6V$. Thus, the

resulting equations for the voltage glitch for this case are:

$$V_a(t) = \begin{cases} Eqn.\ 3 & t < T^1_{sat} \\ Eqn.\ 5 & T^1_{sat} \leq t < T^1_P \\ min(Eqn.\ 9, VDD + 0.6V) & T^1_P \leq t < T^2_P \\ Eqn.\ 12 & T^2_P \leq t \leq T^2_{sat} \\ Eqn.\ 10 & t > T^2_{sat} \end{cases}$$

Using the equations for the radiation-induced voltage glitch obtained in this Section (for Cases 1, 2 and 3), we can determine the shape of the glitch. For all three cases, we can also find the pulse width of the voltage glitch at node a using the values of t_1 and t_2. Note that we *do not ignore* τ_β in the derivation of the voltage glitch equations and in the calculation of all time variables of our model such as T^1_{sat}, t_1, T^1_P, etc. Sometimes, we ignored the contribution of the e^{-t/τ_β} term of $i_{seu}(t)$ only during the *calculation of the initial guess* for these time variables.

IV. Experimental Results

We compared the accuracy of our model for determining the shape of the voltage glitch induced by a radiation particle strike with SPICE [28]. Our method is implemented in *perl* and is 275× faster than SPICE simulation for the estimation of the radiation-induced voltage glitch at the output of an inverter. For other gates such as NAND, NOR, etc, SPICE takes more time to simulate a radiation particle strike due to more number of transistors in these gates than inverter. However, the runtime of our approach does not change significantly with different gate types due to the usage of a model for the load current of the gate. Therefore, the speedup of our approach compared to SPICE simulation will be higher for NAND, NOR and any complex gates [4]. We implemented a cell library using a 65nm PTM [27] model card with $VDD = 1V$. Our cell library contains INV, NAND and NOR gates of 5 different sizes (1× to 5×) and different numbers of inputs. As mentioned in Section III-B, before we can use our model to compute the shape and the pulse width, we need to obtain look-up tables for the load current model of the gate, the input gate capacitance C_G and the output node diffusion capacitance C_D (for all input combinations) for all the gates in our library. The method to obtain the load current, C_G and C_D look-up tables was explained in Section III-B.

To validate the applicability of our model to different types of gates, we simulated radiation particle strikes at the output of INVs, 2-input NANDs and 3-input NORs using our model. For each gate type we considered 5 different sizes (1× to 5×) with all possible input states. We also validated the applicability of our model to different scenarios by loading the gates with different loads and by varying the values Q, τ_α and τ_β. All gates were loaded with 1 and 3 inverters of the same size as the equivalent inverter of G. We simulated radiation particle strikes corresponding to $Q = 150fC$, $\tau_\alpha = 150ps$ and $\tau_\beta = 50ps$ and $Q = 100fC$, $\tau_\alpha = 200ps$ and $\tau_\beta = 50ps$.

The radiation-induced voltage glitches obtained using our model and SPICE are shown in Figure 3 for INV, NAND2 and NOR3 gates with different scenarios (as mentioned in the figure). Figure 3 also reports the operating case of the gate with the gate size and the input state. From Figure 3, we observe that the voltage glitch waveforms obtained using our model *match very closely* with the voltage glitch obtained from SPICE. Note that we simulated these gates of different sizes with all possible input states and with different radiation induced current pulses. However, due to the lack of space, we are showing only a few waveforms. The voltage glitches shown in Figure 3 were chosen to demonstrate applicability of our model to different scenarios. Figure 3(b) corresponds to Case 3 in which a 4× INV has its input at GND value and is driving 3-4× INVs. In this case, the voltage glitch predicted by our model deviates from SPICE when the affected node voltage drops to 0.2V. This is due to the Miller-feedback from the switching of the output of the loading inverters (3-4× INVs) to the node affected by radiation strike. The effect of the Miller-feedback is more dominant for the gates operating in Case 3 than in Case 1 and 2. This is because in Case 3, the effect of a radiation particle strike is lower than in Case 1 or 2 and hence the Miller-feedback has a significant impact on the voltage glitch. We also observe slight mis-matches in some of the voltage glitch waveforms of Figure 3. We conjecture that this is due to the modeling error which is introduced by the gate characterization at a coarser voltage step of 0.1V.

[4]For 2-input NAND gate, our approach is 330× faster than SPICE simulations

		Input State								Avg.
Load	Gate	0	1	2	3	4	5	6	7	RMSP Err.
1	INV	2.86	2.62							2.74
1	NAND2	3.75	3.05	3.3	4.0					3.52
1	NOR3	3.45	2.43	7.06	3.65	10.85	5.38	7.40	8.76	6.12
3	INV	3.46	4.94							4.2
3	NAND2	3.72	3.36	3.57	5.89					4.13
3	NOR3	3.29	4.24	5.13	4.51	9.40	5.72	5.64	10.41	6.04
Avg.										5.06

TABLE I
RMSP ERROR OF OUR MODEL FOR 3× GATES AND $Q = 150fC$, $\tau_\alpha = 150ps$ AND $\tau_\beta = 50ps$

		Gate Size					
Load	Gate	1×	2×	3×	4×	5×	Avg. RMSP Err.
1	INV	2.72	2.66	2.74	3.08	3.49	2.94
1	NAND2	3.45	3.27	3.52	3.93	3.80	3.6
1	NOR3	4.43	4.76	6.04	6.96	6.02	5.64
3	INV	3.66	3.95	4.20	4.61	5.15	4.3
3	NAND2	3.81	3.83	4.14	4.69	4.53	4.2
3	NOR3	4.77	4.99	6.12	6.98	7.12	6.00
Avg.							4.45

TABLE II
RMSP ERROR OF OUR MODEL FOR DIFFERENT GATES SIZES AND $Q = 150fC$, $\tau_\alpha = 150ps$ AND $\tau_\beta = 50ps$

We evaluate the performance of our model by calculating the root-mean-square percentage ($rmsp$) error of the voltage glitches obtained using our model compared to the glitch waveforms obtained using SPICE. We computed the $rmsp$ error over a time period for which the affected node voltage value is greater (lesser) than V_{TN} ($VDD - |V_{TP}|$) for a positive (negative) glitch. Table I reports the $rmsp$ error of our model for 3× gates and with a radiation particle strike corresponding to $Q = 150fC$, $\tau_\alpha = 150ps$ and $\tau_\beta = 50ps$ for all possible input states. Column 1 reports the number of inverters driven by the gate reported in Column 2. Note that the loading inverters are of the same size as the equivalent inverter of the corresponding gate. Columns 3 through 10 reports the $rmsp$ error of the voltage glitch estimated by our model compared to SPICE for all possible input states. Column 11 reports the average $rmsp$ error for a 3× gate averaged over its all possible states. A blank entry in Table I implies that the input state of the corresponding column is not applicable to the corresponding gate. From Table I, we conclude that our model is able to predict the radiation-induced voltage glitch for 3× gates with a very small $rmsp$ error of 5.06% (as reported by the last row of Table I) averaged over all gates for all input states. We obtained similar results for $Q = 100fC$, $\tau_\alpha = 200ps$ and $\tau_\beta = 50ps$ (which are omitted for brevity).

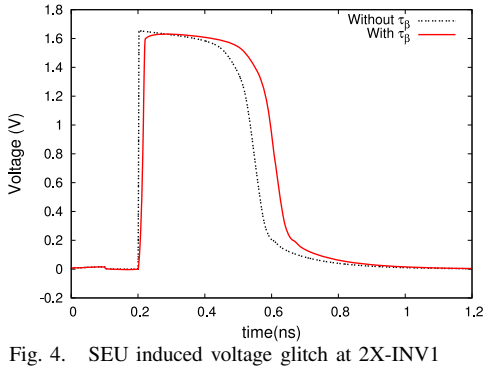
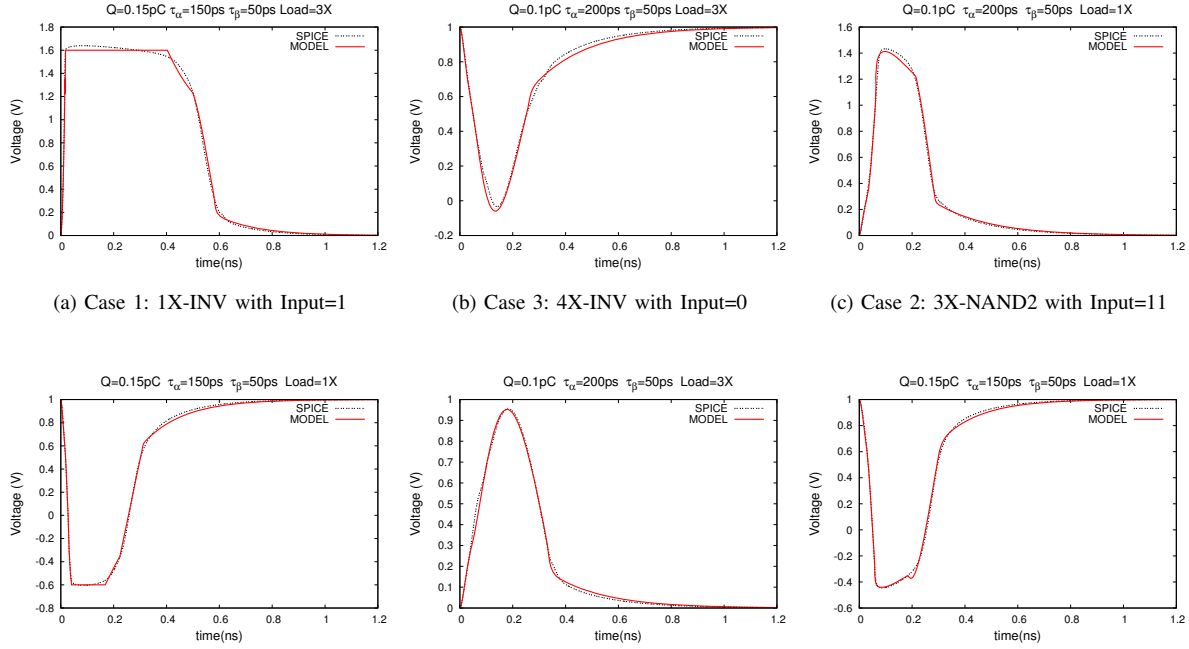


Fig. 4. SEU induced voltage glitch at 2X-INV1

Tables II reports the $rmsp$ error of our model for different gate sizes from 1× to 5× with $Q = 150fC$, $\tau_\alpha = 150ps$ and $\tau_\beta = 50ps$ and averaged over all possible input states for a gate. From Tables II, we observe that our model to estimate radiation induced voltage glitch is very accurate and the average $rmsp$ error is 4.45% averaged over all simulated scenarios (different gate types, gate loading and gate sizes). Also, our approach is *at least* 275× faster than SPICE



(a) Case 1: 1X-INV with Input=1 (b) Case 3: 4X-INV with Input=0 (c) Case 2: 3X-NAND2 with Input=11

(d) Case 1: 2X-NAND2 with Input=00 (e) Case 3: 4X-NOR3 with Input=010 (f) Case 2: 5X-NOR3 with Input=000

Fig. 3. Radiation-induced voltage glitches obtained using our model and SPICE for different gates

simulations. Note that the best known previous analytical approach to predict the radiation-induced voltage glitch is reported in [14] which is just $100\times$ faster than SPICE. Also in [14], the authors report that their approach sometimes yields 15% error in the SEU induced glitch, compared to SPICE. Moreover, the authors ignore the effect of the ion track establishment constant (τ_β) by setting it to zero for both their model as well as SPICE simulations. To evaluate the impact of ignoring τ_β on the radiation-induced voltage glitch, we simulated radiation particle strikes (with and without the inclusion of τ_β) at the output of inverters of different sizes ($1\times$ - $5\times$) in SPICE. We performed these simulations for two different radiation strike parameter values ($Q = 150fC$, $\tau_\alpha = 150ps$, and $\tau_\beta = 50ps$) and ($Q = 100fC$, $\tau_\alpha = 200ps$ and $\tau_\beta = 50ps$) and for different loads on the inverters. For $Q = 150fC$, $\tau_\alpha = 150ps$, and $\tau_\beta = 50ps$ ($Q = 100fC$, $\tau_\alpha = 200ps$ and $\tau_\beta = 50ps$), we found that ignoring τ_β results in an *underestimation of the pulse width of the voltage glitch by 10% (8%)*. The voltage waveforms at the output of a 2X inverter under a radiation particle strike with and without the inclusion of the τ_β term (for $Q = 150fC$, $\tau_\alpha = 150ps$, and $\tau_\beta = 50ps$) are shown in Figure 4. The $rmsp$ error of the voltage glitch without τ_β shown in Figure 4 is 40% which is much higher than the error of our approach. Thus, for an accurate analysis, it is crucial to include the contribution of τ_β. As mentioned earlier, the authors of [14] ignore τ_β and therefore, the error of their approach can be much higher than reported in [14] when compared with the shape of the radiation-induced voltage glitch obtained by considering the contributions of τ_β. To the best of our knowledge, our paper is the first to model the effect of both τ_α and τ_β for the estimation of the shape of the radiation-induced voltage glitch. Thus, our approach is more accurate than the best known previous approach [14].

V. Conclusions

In this paper, we present an analytical model for the determination of the shape of radiation-induced voltage glitches in combinational circuits. The radiation-induced voltage glitch at an internal node of a circuit can be propagated to the primary outputs of the circuit (using existing tools) to account for the effects of electrical masking. This enables an accurate and quick evaluation of the SEU robustness of a circuit. Experimental results demonstrate that our model is very accurate, with a very low root mean square percentage error in the estimation of the shape of the voltage glitch (of 4.5%) compared to SPICE. Our model gains its accuracy by using a non-linear model for the load current of the gate, and by considering the effect of τ_β of the radiation induced current pulse. Our analytical model is very fast ($275\times$ faster than SPICE) and accurate, and can therefore be easily incorporated in a design flow to implement SEU tolerant circuits.

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