SEU Hardened Clock Regeneration Circuits

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***Abstract*— Single event upsets (SEUs) are becoming increasingly problematic for VLSI circuits due to device scaling, decreasing supply voltages and increasing operating frequencies. To deal with SEUs, radiation hardening is often employed to increase the reliability of VLSI systems. Most existing radiation hardening approaches focus on the combinational or sequential part of the design. Little or no attention has been paid to the impact of radiation particle strikes on the clock network of an IC. Recently, it has been shown that in the deep submicron regime, radiation particle strikes on clock networks can prove to be catastrophic. As a result, the clock network contributes significantly to the chip level Soft Error Rate (SER). In this paper, we present two SEU hardened clock regenerator designs which are immune to radiation particle strikes. The new designs result in a significant reduction in SEU induced clock jitter. Experimental results demonstrate that our clock regenerator hardening approaches reduce the radiation induced jitter to around 30ps and completely eliminates radiation induced voltage glitches, for radiation strikes with a deposited charge of up to 150fC.**

Keywords: Soft Errors, Single Event Upset (SEU), Clock Regeneration

I. Introduction

Deep sub-micron CMOS VLSI designs are characterized by successively diminishing feature sizes, lower supply voltages and higher operating system frequencies. These technology trends are adversely affecting noise margins of VLSI circuits, making them more susceptible to noise effects such as crosstalk, power supply variations and single event effects (SEE) (or soft errors). SEUs are caused when radiation particles like protons, neutrons, alpha particles, or heavy ions strike sensitive regions in VLSI circuits. These particle strikes usually deposit sufficient charge on circuit nodes to cause a voltage pulse or glitch on that node. A charge deposition from these radiation particles in semiconductor memories may cause bit-flips and hence alter the stored state of a memory element. This is generally referred as Single Event Upset(SEU) [1], [2]. In addition to the SEU effects on sequential elements, soft errors in combinational circuits are contributing increasingly to chip-level soft error rate (SER) in deep-submicron technologies [3], [4], [5]. In combinational logic, the charge deposition due to radiation particles causes a voltage glitch which may propagate to the primary output(s). This may result in the sampling of incorrect data by subsequent flip-flops, leading to system failure. Although the SER of sequentials and combinational circuits has been studied extensively in the past, the SER due to upsets in the clock nodes can result in several errors simultaneously, and has not been extensively studied. The clock distribution network in a chip consists of a global clock distribution network followed by regional clock regeneration buffers. The global clock signal is relatively immune to radiation strikes due to the large node capacitances [6] of this signal. However, a particle strike on a regional regenerator may result in a significant voltage glitch. This may result in incorrectly sampled data by all the sequentials connected to the regional clock node. In other words, multiple upsets can occur due to a simple strike on a regional clock regenerator. Therefore, the focus of this paper is to present design approaches to harden the regional clock regeneration buffers. We present two radiation hardened regional clock regenerator designs which minimize radiation induced jitter and eliminate voltage glitches for radiation strikes up to 150 fC.

The amount of charge deposited per unit time is therefore quantified as the Linear Energy Transfer (LET). As the amount of charge deposited by a radiation strike is directly proportional to the LET (L) and charge collection depth (t) which is seen in the following equation [7]:

$$Q = 0.01036 \cdot L \cdot t$$

Here L is expressed in MeV-cm^2/mg, t in microns, and Q in pC. For example, an alpha particle with 5 MeV-cm^2/mg LET deposits around 50fC/μm. The minimum amount of deposited charge that is required to cause an SEU is defined as critical charge (Q_{crit}) [2]. Additionally, the probability distribution of energetic particles drops off rapidly with increasing LETs [8]. The largest population of particles have an LET of 20 MeV-cm^2/mg or less, and particles with an LET greater than 30 MeV-cm^2/mg are exceedingly rare [8], [9]. The current pulse that results from a particle strike is traditionally described as a double exponential function [10], [11]. The expression for the pulse is :

$$i_{seu}(t) = \frac{Q}{(\tau_\alpha - \tau_\beta)}(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}) \quad (1)$$

Here Q is the amount of charge collected as a result of the ion strike, while τ_α is the collection time constant for the junction and τ_β is the ion track establishment time constant. Time constants τ_α and τ_β depend upon several process related parameters, and typically τ_α is on the order of 100ps and τ_β is on the order of tens of picoseconds [4], [12]. In our experiments, we have used $Q = 150fC$, $\tau_\alpha = 150ps$ and $\tau_\beta = 38ps$ [12], [13].

The importance of reliability in digital circuits, especially in highly critical applications such as biomedical, space and

military electronics is the major motivation for circuit hardening against radiation strikes. There has been a great deal of work on radiation hardened circuit design approaches, with a focusing on combinational and sequential designs [14], [15], [12], [16], [5], [17], [18]. Very little attention has been paid to SER due to radiation particle strikes on clock nodes despite their significant contribution to the chip level SER. Clock node upsets account for nearly 20% of the overall sequential SER [6]. The global distribution clock network is relatively immune to upsets [6] due to the following reasons:

- The global clock net has large buffers and large node capacitances.
- It has a smaller active area (which can collect charge) compared to the cumulative active area occupied by the regional regenerators.
- The global clock grid has a large RC time constant and thus acts as a low pass filter.

The authors in [6] also report that the contribution to the SER of the global clock grid is negligible (0.1%) compared to that of the regional regenerator circuit. The clock nodes of the regional regenerator circuits are very susceptible to radiation strikes. The regional regenerator drives a relatively small load at its output (depending on the number of sequential elements connected to it). In order to drive this load at a reasonable slew rate, progressively sized inverters are used in the regenerator circuit as shown in Figure 1. The PMOS and NMOS transistors of these inverters are prone to radiation strikes, resulting in *radiation-induced clock jitter* and voltage glitches (also referred to as *radiation-induced race*) in the clock nodes. These effects can cause incorrect data to be latched by the sequential elements that are connected to these clock regenerators. Radiation-induced race and radiation-induced jitter are described further in Section III-A.

In this paper, we present two radiation hardened designs for the regional clock regenerators, using a triple modulo redundancy (TMR) approach as well as a split-output SEU tolerant inverter approach. Our hardened regenerator circuits suppress glitches due to SEU strikes, and also significantly improve the clock jitter as compared to regular clock regenerator. We compare our solutions with each other, and show that the split-output inverter based design achieves smaller area overhead, better jitter and improved glitch suppression compared to the TMR approach. Our designs can be used with any global clock distribution network, to provide a reliable clock signal to the sequential elements in the design. Hence, our approach reduces the SER impact of radiation particle strikes on clock nodes.

The main contributions of this paper are:

- We study the vulnerability of the unhardened regional regenerator to radiation particle strikes.
- We implement a TMR based hardening approach for the regional regenerators and study the performance metrics (i.e. area, dynamic power, glitch suppression and jitter reduction) for this method.
- We present another radiation hardened regional regenerator using split-output inverter stages. This circuit is compared with the unhardened case as well as the TMR based hardening approach.

The rest of the paper is organized as follows. Section II briefly discusses previous work in this area. In Section III we describe our circuit design approaches to harden the regional clock regenerator. We first study the vulnerability of clock nodes in an unhardened regenerator. Then, we report results for a TMR based hardening technique for the clock regenerator. We also present our split-output inverter based solution. In Section IV we present experimental results for both the hardened approaches, along with the unhardened regenerator circuit. Section V concludes the paper.

II. Previous Work

There has been a great deal of work on radiation hardened circuit design approaches. Several papers report on experimental studies in the area of hardened logic circuits [7], [2], [19], [5], [12], [15], while others have focused on radiation hardened memories [1], [2], [20], [21], [22], [23], [24], [25]. Since memories are particularly susceptible to SEU/SET events, these efforts were crucial to space and military applications. Other approaches address the modeling and simulation of radiation events [11], [8], [26].

Circuit hardening approaches can be classified as device level [14], circuit level [15], [12], [16], [5], [24], [25] and system level [20]. The device and circuit level approaches are typically fault *avoidance* approaches, while system level approaches typically involve the use of fault *detection and tolerance* mechanisms. Device level approaches require changes to the fabrication process to improve the radiation immunity of a design [14], whereas circuit level hardening approaches use special circuit design techniques that reduce the vulnerability of a circuit to radiation strikes. System level approaches typically involve the use of fault *detection and tolerance* mechanisms. For example, triple modular redundancy (TMR) is a classical example of a system level design approach.

Although much work has been published in the literature with respect to hardening techniques for combinational and sequential circuits, very few research efforts have addressed the problem of clock node upsets and their effect on the chip level sequential SER. Recently, the authors of [6] studied the effect of radiation particle strikes on clock nodes. They partitioned the radiation induced transients on the clock into two categories: *radiation-induced clock jitter* and *radiation-induced race*. They report that 20% of total sequential SER is due to clock node upsets. The contribution of radiation-induced jitter is less than 2% of the total sequential SER. This means that most of the upsets occur due to radiation-induced race. Another important conclusion of their experiments was that the contribution of the global clock network is 0.1% of the overall SER due to clock node upsets. Hence, we can conclude that clock node upsets contribute significantly to the SER of the design. Moreover, radiation particle strikes on the regional clock regenerator are primarily responsible for the SER due to radiation strikes on the clock network. The authors of [27] performed an experimental analysis to

calculate the contribution of clock node upset to SER on the "RH1020" chip in high energy radiation environments. They suggest that the clock upset rate has a strong and linear dependence on clock frequency. They suggest ad-hoc methods to reduce clock node upsets, such as reducing clock frequency and using redundancy in the clock network. However, no experimental results or design approaches were presented.

In this paper, we present two hardening techniques for regional clock regenerators. Our experimental results indicate a significant improvement in SEU tolerance over a regular clock regenerator. One approach uses TMR for radiation hardening, while the other approach uses radiation hardened split-output inverters from [13] to construct a SEU tolerant regional clock regenerator. The TMR approach eliminates the risk of radiation-induced clock races by suppressing glitches in the clock nodes (up to Q=150fC). However, it does not reduce the radiation-induced jitter as effectively as the split-output inverter based approach. Additionally, it has an area overhead (282%) and increased dynamic power consumption by (116%) as compared to regular clock regenerator. In our second approach, we present a novel design which completely eliminates radiation-induced races and reduces radiation-induced jitter to within tolerable limits ($\sim$ 30ps) for up to $Q = 150fC$. It has less dynamic power consumption (18% lower) and less area (25% lower) as compared to the TMR based approach of clock-hardening.

III. Our Approach

In Section III-A, we discuss the effects of radiation particle strike on a regular regional clock regenerator circuit. Section III-B explains the TMR based hardening method for the clock regenerator. and Section III-C presents our split-output inverter based clock regenerator hardening technique.

A. Regular Unhardened Regional Clock Regenerator

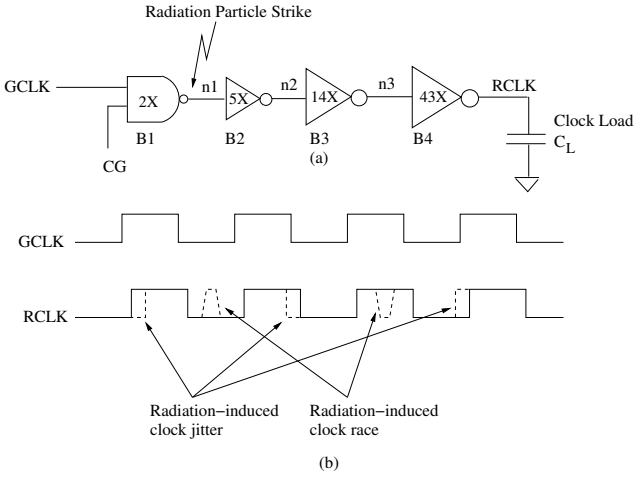

Fig. 1. a) Regular regional clock regenerator under consideration, b) Voltage waveform at $GCLK$ and $RCLK$.

A regular regional clock regenerator is shown in Figure 1 (a). Regenerators are generally used to locally buffer the clock signal before driving the sequential elements connected to this regional clock node $RCLK$. The regenerator consists of a NAND gate which has two inputs. One input is the clock signal ($GCLK$) from the global clock distribution network, and the other input is the clock gating signal (CG). In current digital VLSI systems, each regional clock regenerator circuit typically drive the clock signal of around 20 to 64 sequentials in flip-flop based design. Therefore, the clock regenerator circuit drives a load of around 64 flip-flops in the maximal case. In each flip-flop (not shown), the clock input drives a load of a 2X inverter, assuming typical master-slave D flip-flops. Hence, for our simulations we use a 128X ($64 \times 2X$) inverter as the capacitive load driven by the clock regenerator. In order to drive this load with minimum delay and reasonable slew rates, a chain of progressively sized inverters is used. Figure 1 shows three progressively sized inverters (5X, 14X, 43X) with sizing ratios nearly equal to the optimal sizing ratio ($\sim$ 3) required for minimum delay [28].

To study the effect (on the timing of the output $RCLK$) of radiation particle strikes, we simulated radiation particle strikes on each node ($n1$, $n2$, $n3$, and $RCLK$) of the regular clock regenerator circuit of Figure 1 (a). We used the current pulse equation given in Equation 1 (with Q=150fC, τ_α=150ps and τ_β=38ps [12], [13]). These radiation particle strikes were modeled at different times during the clock period (for $n1$, $n2$, $n3$ and $RCLK$ nodes). The clock regenerator shown in Figure 1 was implemented using a 65nm PTM model card [29] with VDD=1.0V. Figure 1 (b) shows the voltage waveforms at $GCLK$ and $RCLK$ when there is no radiation strike (solid line) and during a radiation strike at $n1$ (dotted line). In general, radiation strikes can occur at any node of the clock regenerator. Our experiments show that radiation particle strikes at the times when the clock signal is changing generally result in a radiation-induced jitter due to shifting of the clock edge of $RCLK$ (as shown in Figure 1 (b)). On the contrary, radiation strikes at the static portions of the clock signal result in voltage glitches which may break a clock pulse into two smaller clock pulses also shown in Figure 1 (b). In this case, new clock edges are formed before the completion of the actual clock cycle. This causes a radiation-induced race condition. These two phenomena are defined as follows [6]:

- **Radiation-induced clock jitter:** During the transition of the clock pulse, any charge injected into the nodes of a clock regenerator by a radiation particle strike can cause the clock edge to move. The difference in the clock arrival time at $RCLK$ due to radiation particle strikes on the clock regenerator is called radiation-induced clock jitter.
- **Radiation-induced race:** Voltage glitches due to radiation particle strikes at the nodes of clock regenerator can create a new clock edge at $RCLK$ which can result in incorrect data being latched. This phenomenon of data racing through two sequentials in one clock cycle due to a radiation particle strike is called radiation-induced race.

The worst voltage glitch (in terms of pulse width) at

$RCLK$ occurs due to a radiation particle strike at the node $n1$. Through SPICE [30] simulations we found that a particle strike at $n1$ can result in a voltage glitch at $RCLK$ with the pulse width as high as 442.3ps. The maximum radiation induced clock jitter is around 833.5ps. Note that a radiation particle strike at the succeeding nodes $n2$ and $n3$ also results in a voltage glitch with significant pulse width and clock jitter. However, the effect of particle strikes at $n2$ and $n3$ at $RCLK$ is less severe than that of a particle strike at $n1$. These results clearly demonstrate the need for hardening clock regenerator circuit. At node $RCLK$, the driving inverter is very large (i.e. 43X), therefore, a radiation particle strike (corresponding to Q=150fC, τ_α=150ps and τ_β=38ps) at this node does not affect the clock signal at $RCLK$ significantly.

B. TMR based Regional Clock Regenerator

In this approach, we implemented a triple modulo redundancy based design for hardening the regional clock regenerator. We used TMR to regenerate the clock signal using three parallel regenerator circuits as shown in Figure 2. The three parallel signals are used as inputs of a majority function gate. The output of the majority function gate is then used to drive the 43X inverter (B4) which is immune to radiation particle strikes (up to 150fC). The majority function gate implements voting logic to compute the correct output. The voting logic function with three inputs a, b and c is $\overline{ab + bc + ca}$. In this case, a radiation strike at a node (say $n1\_1$) will result in an incorrect value at one of the inputs of the majority function gate (at $n2\_1$). However, the other two inputs of the majority function gate ($n2\_2$ and $n2\_3$) will be at their correct value. Thus, the majority function gate can compute the correct input value for B4. To protect $RCLK$ from a radiation particle strike at the output of majority function gate ($n3$), we size up the majority function gate [12]. In this way, the clock regenerator shown in Figure 2 is tolerant to a radiation particle strike.

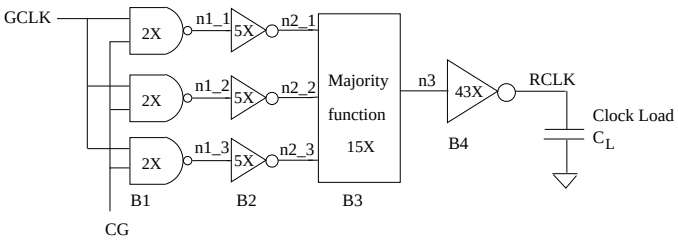

Fig. 2. TMR Based Regional Clock Regenerator Circuit

C. Split-output Inverter Based Clock Regenerator

Before we describe our split-output based regional clock regenerator hardening approach, we explain why the split-output inverter [13] is tolerant to radiation particle strikes.

1) Radiation Tolerant Split-output Inverter: A radiation particle strike induces a current which always flows from the n-type diffusion to the p-type diffusion through a pn junction [13], [24]. This implies that a radiation particle strike at a PMOS (NMOS) transistor can only lead to a 0 to 1 (1 to 0) node voltage change. This fact is utilized in [13] to design highly SEU tolerant standard cell gates. Consider two regular (unhardened) inverters as shown in Figure 3 (a). To harden INV1 of Figure 3 (a) such that a particle strike at the output of INV1 does not affect the voltage at the output of INV2, INV1 is modified as shown in Figure 3 (b). INV1 shown in Figure 3 (b) has 2 inputs (inp and inn) and 2 outputs ($out1p$ and $out1n$). Both inputs of INV1 are of the same polarity. Similarly, both outputs of INV1 are also of same polarity. Also, note that the inverter INV2 is also modified such that two different input signals (of the same polarity) drive the transistors M3 and M4. This is required since the hardened INV1 has dual outputs. In the sequel, we refer to a gate (such as inverter INV2 of Figure 3 (b)) whose inputs to PMOS and NMOS transistors are separated, as a *modified* gate. Note that in general such a gate has $2n$ inputs (compared to n inputs for an unmodified gate).

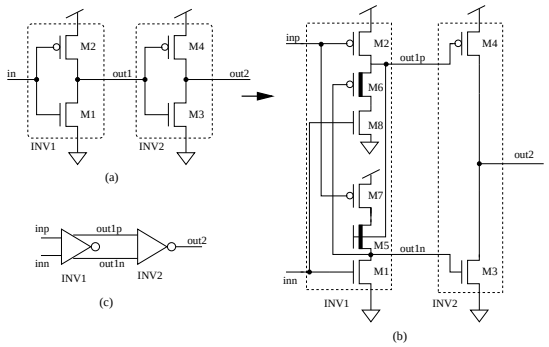

Fig. 3. Split-output SEU tolerant inverter of [13]

The inverter INV1 of Figure 3 (b) works as follows. Assume that both inn and inp are at a logic 0 value. Therefore, $out1p$ and $out1n$ are at logic 1. Now assume that both inn and inp transition to logic 1, due to which transistor M1 turns on and M2 turn off. The turning on of M1 pulls the node $out1n$ down to logic 0 which then turns on M6. Since M6 is ON and M8 is also ON, $out1p$ is driven to a weak logic 0 (i.e. to $|V_T^{M6}|$ volts). Note that V_T^{M6} is the threshold voltage of PMOS transistor M6. Both $out1p$ and $out1n$ are now at logic 0, due to which the output of INV2 ($out2$) goes to logic 1. Now when both inputs of INV1 (inn and inp) change to logic 0, then transistor M1 turns off and M2 turns on. As M2 is on, $out1p$ charges to logic 1, which turns M5 on and hence, node $out1n$ is pulled to a weak logic 1 (VDD- V_T^{M5} volts) since M7 is also ON. Since $out1n$ and $out1p$ are both at logic 1, the node $out2$ is driven to logic 0. Thus, INV1 of Figure 3 (b) behaves like an inverter, with the output node $out1p$ ($out1n$) switching between VDD and $|V_T^{M6}|$ (VDD - V_T^{M5} and GND). Also, note that the transistors M5 and M6 of INV1 of Figure3 (b) are selected to be low threshold voltage transistors (indicated by a thicker line in the figure). This is done so as to increase the voltage swing at nodes $out1p$ and $out1n$, and bring them closer to the rail voltages.

The inverter INV1 of Figure 3 (b) is tolerant to a radiation strike at $out1p$ and $out1n$. Consider the case when the nodes inp and inn are at VDD, which implies that $out1p$ and $out1n$ are at $|V_T^{M6}|$ and GND respectively, and $out2$ is at

the VDD value. Now suppose a radiation particle strikes at node $out1p$ (the radiation particle strikes either M2 or M6) which increases the voltage at node $out1p$ to VDD (due to the positive charge collection at $out1p$). Due to this, M4 of INV2 turns off and M5 turns on. However, the node $out1n$ remains at GND value because M7 is in cutoff. Therefore M3 also remains off. Thus, the node $out2$ remains at the VDD value, in a high impedance state. Eventually, the charge collected at $out1p$ dissipates through M6 and M8 (since inp and inn are at VDD) which brings the voltage at $out1p$ node back to $|V_T^{M6}|$. At this point, M4 turns on again. In this way, the radiation strike at $out1p$ does not affect the voltage value of the $out2$ node. Similarly, a particle strike at $out1n$ does not affect the node $out2$ when inn and inp are at the GND value. A radiation particle strike at M8 can be of any significance only when $out1p$ is at the VDD value (since a radiation particle strike at the NMOS transistor can only result in a negative glitch). However, when $out1p$ is at VDD, M6 is turned off and hence a particle strike at M8 does not affect the node voltage of $out1p$. Similarly, a radiation particle strike at M7 does not affect the voltage of the $out1n$ node. Hence, INV1 of Figure 3 (b) is tolerant to radiation particle strikes.

D. Our Split-output Inverter based Clock Regenerator Hardening

As mentioned earlier, a radiation particle strike at $RCLK$ of the clock regenerator shown in Figure 1 does not significantly affect the clock signal at $RCLK$. However, a particle strike at either of $n1$, $n2$ and $n3$ nodes may result in a significant clock jitter or a voltage glitch at $RCLK$. Therefore, we need to harden the gates driving the $n1$, $n2$ and $n3$ nodes (i.e. gates B1, B2 and B3, respectively) in the regional clock regenerator of Figure 1.

We cannot directly replace B1, B2 and B3 in Figure 1 by their hardened counterparts obtained using the hardening approach of [13], in order to obtain radiation tolerant clock regenerator. This is because when a radiation particle strike induces a voltage glitch at either $out1p$ or $out1n$ of INV1 of Figure 3 (b), then both the PMOS and the NMOS transistors of INV2 turn off. Hence, during this time, the output of INV2 remains in high-impedance state. Now suppose that a radiation particle strike occurs at $out1p$ of INV1 of Figure 3 (b), just after both $out1p$ and $out1n$ had fallen to GND and before $out2$ has risen to VDD. Then, $out2$ will enter high impedance state with GND or some intermediate voltage value, which would be incorrect. If these inverters were a part of the clock regenerator of Figure 1 (with INV1 corresponding to B3 and INV2 to B4) then this phenomenon may delay the clock edge at $RCLK$ and hence, result in a large clock jitter.

To deal with this problem, we duplicate the buffer chain in the clock regenerator of Figure 1. The resulting chains are B1-B2-B3-B4 and B1d-B2d-B3d-B4d (Figure 5. In these two buffer chains, we replace regular NAND2's and inverters by their hardened counterparts obtained using the hardening approach of [13]. Now, there are two outputs of B4: op and on corresponding to the top and the bottom outputs of the hardened inverter, respectively. Similarly, there are two output of B4d: opd and ond. Out of these 4 outputs, op and opd (on and ond) are driven by only PMOS (NMOS) transistors. Therefore, op and opd (on and ond) can experience only 0 to 1 (1 to 0) flips due to a radiation particle strike. Using these 4 outputs, we want to generate the correct clock signal $RCLK$ even during a radiation particle strike at any node of these two chains. The function of op, opd, on and ond which generates the correct $RCLK$ signal is obtained using the Karnaugh map shown in Figure 4. If there is no radiation particle strike, at all op, opd, on and ond will be either at 0 or 1. Due to a radiation strike, only one of op, opd, on and ond will be at the incorrect value. All other possible values of op, opd, on and ond (with two or more errors) are don't cares. If there is an error in one of op, opd, on and ond value, we still want to obtain the correct signal at $RCLK$. Based on this, we construct the Karnaugh map shown in Figure 4. From the Karnaugh map, we obtain that the $RCLK$ signal is $op \cdot opd$. The resulting clock regenerator circuit that we obtain after this approach is shown in Figure 5 (a). To protect the clock signal $RCLK$ of the clock regenerator shown in Figure 5 (a) from the radiation strikes at $n5$ (the output of B6), we used gate sizing approach of [12]. We have to size up B6 to 28X to reduce the effects on $RCLK$ of radiation particle strikes at $n5$.

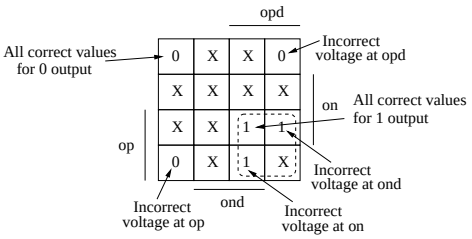

Fig. 4. Karnaugh map for correct $RCLK$ clock signal

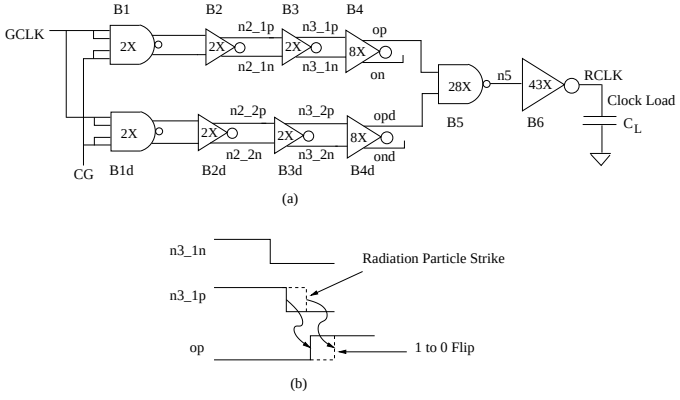

Fig. 5. Clock regenerator circuit using split-output gates (initial incorrect design for illustration purposes)

Now we would expect that the clock regenerator shown in Figure 5 (a) is tolerant to radiation particle strikes at any node in the regenerator. However, this is not the case – the clock

regenerator is tolerant to strikes at only op, opd, on, ond, $n5$ and $RCLK$ nodes. This is because a particle strike at any other node may translate into 1 to 0 (0 to 1) upset at op or opd (on or ond) nodes. This is explained through the waveforms shown in Figure 5 (b). In Figure 5 (b), the waveforms during no radiation strike are shown by solid lines. Waveforms under radiation strike are shown by a dashed line. When there is no radiation strike, a falling transition at $n3\_1p$ results in a rising transition at the op node. Now assume that a radiation particle strike occurs at $n3\_1p$ just at the time when it is supposed to fall. Due to this, the falling transition at $n3\_1p$ gets delayed. Hence, the rising transistor at op gets delayed as well. This delay in the rising transition at op appears like a 1 to 0 flip which we considered as a don't care in the Karnaugh map shown in Figure 4 (since op is driven by only PMOS transistors). Similarly, a 1 to 0 flip can occur on the opd node, as well due to a radiation particle strike at $n3\_2p$. To fix this problem, we need to ensure that only 1 to 0 flips occur at the op and opd nodes. Hence, we have to modify the input connections of the inverters B4 and B4d of Figure 5. Specifically, we have to connect both inputs of B4 (B4d) to $n3\_1n$ ($n3\_2n$). Now we recall that radiation particle strike at $n3\_1n$ ($n3\_2n$) can only result in a 1 to 0 flip. This can only lead to a 0 to 1 flip at op (opd). Therefore, a particle strike at the inputs of B4 (B4d) can only lead to a 0 to 1 flip at op (opd), which is protected due to the way we constructed the Karnaugh map shown in Figure 4. However, we now have to make sure that a radiation particle strike at any node of the clock generator of Figure 5 can only lead to a 1 to 0 flip at $n3\_1n$ ($n3\_2n$). To ensure that, we have to repeat the same procedure and connect both inputs of B3 (B3d) to $n2\_1p$ ($n2\_2p$). We can carry out this process until we reach the output of the NAND2 gates (i.e. B1 and B1d). The final radiation tolerant clock regenerator circuit that we obtain is shown in Figure 6. The regenerator gate were sized to drive a load of a 128X inverter, which is same as the load driven by the regular clock regenerator shown in Figure 1 and the TMR based clock regenerator of Figure 2.

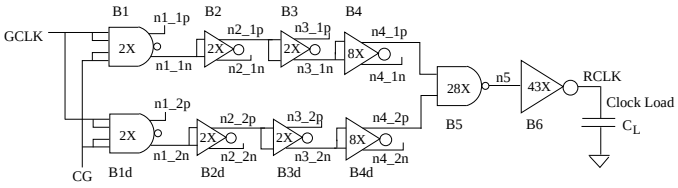

Fig. 6. Final Split-output Inverter Based Clock Regenerator Circuit

Note that the final split-output inverter based regenerator is as shown in Figure 6. The version shown in Figure 5 was meant to describe the approach, but it had a deficiency which was fixed by the final design of Figure 6.

We verified our analysis, and validated that the clock regenerator circuit shown in Figure 6 is tolerant to radiation particle strikes at any node and at any time, through SPICE [30] simulations. We simulated radiation particle strikes at each node and at different times during a clock period. The results are presented in Section IV. Note that in practice, B1 (B1d) can directly drive B4 (B4d) if the clock load is not very high. We validated that the clock regenerator circuit shown in Figure 6 is tolerant to radiation particle strikes for both cases: when B2 (B2d) and B3 (B3d) are included in the clock regenerator, and when B2 (B2d) and B3 (B3d) are not included in the clock regenerator (i.e. when B1 (B1d) directly drives B4 (B4d)). In Section IV, we present the results for the case when B1 (B1d) directly drives B4 (B4d).

IV. Experimental Results

We implemented both the TMR based hardened clock regenerator and the split-output inverter based radiation tolerant regional clock regenerator (shown in Figures 2 and 6, respectively) using a 65nm PTM [29] model card with VDD=1.0V. We simulated radiation particle strikes at *all* nodes of the two clock regenerator circuits, and also at different times during the clock period. To simulate a radiation particle strike at a node, we injected a current pulse (given in Equation 1 with $Q = 150fC$, $\tau_\alpha = 150ps$ and $\tau_\beta = 38ps$ [12], [13]) at that node. We assumed a clock frequency of 2GHz. We also created layouts for the regular clock regenerator, TMR and split-output inverter based hardened clock regenerators using the Cadence SEDSM [31] tools. Note that these layouts of the regenerators are not shown due to space constraints. The majority function gate in Figure 2 and the NAND gate driving $n5$ in Figure 6 are sized such that a radiation particle strike at their output results in voltage glitches of identical magnitude. This was done to ensure a fair comparison of both the hardening schemes.

Table I shows our experimental results for the three regenerator circuits under consideration. All measurements are made at the output node of these regenerator circuits ($RCLK$). Column 1 lists the regenerator circuit under consideration. Columns 2 and 3 report the maximum jitter for the rising and falling clock edges at $RCLK$, respectively. The minimum and maximum rise (fall) times are reported in Columns 3 and 4 (5 and 6), respectively. Columns 7 and 8 report the minimum and the maximum pulse width of the clock signal at $RCLK$, respectively. We observe from Table I that the split-output inverter based regenerator circuit exhibits lesser jitter compared to both the TMR based and the regular clock regenerator circuit. The jitter in the rising (falling) clock edge at $RCLK$ for the split-output inverter based regenerator is 65% (52%) of the jitter for the TMR based approach. Hence, we conclude that the split-output inverter based approach is more effective in reducing radiation-induced clock jitter. The rise time and fall time of the clock signal at $RCLK$ for the split-output inverter and TMR based approaches are comparable. Note that both hardening approaches are able to eliminate radiation-induced voltage glitches on $RCLK$ for $Q = 150fC$ with $\tau_\alpha = 150ps$ and $\tau_\alpha = 38ps$. Also note that the minimum pulse width for the regular clock regenerator is 0 since the pulse width of the voltage glitch induced by a radiation particle strike is 442.3ps. This width of the voltage glitch is greater than half of the clock period (the clock period is 500ps with 50%

Circuit	Jitter(ps)		Rise Time(ps)		Fall Time(ps)		Pulse Width(ps)	
	Rise	Fall	Min	Max	Min	Max	Min	Max
Regular	833.5	833.5	36.3	36.3	32.3	32.3	0	253.5
TMR	38.8	58.2	27.2	60.3	23.7	49.6	220.9	307.4
Split-output	25.0	30.1	24.6	47.3	23.6	45.2	273.9	318.3

TABLE I

COMPARISON OF REGULAR, TMR BASED AND SPLIT-OUTPUT INVERTER BASED CLOCK REGENERATOR

	Leakage (nA)	Dynamic Power (μW)	Area (μm^2)
Regular	236	190.5	13.62
TMR	291	412.0	52.1
Split-output	523	338.3	39.1

TABLE II

LEAKAGE, DYNAMIC POWER AND AREA COMPARISON OF REGULAR, TMR BASED AND OUR SPLIT-OUTPUT BASED REGENERATOR

duty cycle) hence, a radiation particle at the regular clock regenerator may completely suppress the clock pulse. Due to this the minimum clock pulse width is 0. Large pulse width of the voltage glitch induced by a radiation particle strike is also responsible for very high radiation-induced clock jitter (833.5ps) in the regular regenerator circuit.

Table II compares the leakage currents, the dynamic power and the layout area of regular regional regenerator, with the TMR based and split-output based hardened regenerators. Column 1 lists the regenerator circuit under consideration. Column 2 reports the leakage power when the $RCLK$ is low. Note that when $CG = 0$, $RCLK = 0$. Hence the leakage numbers reported in Table II correspond to the case when $RCLK = 0$, which is the situation when the regenerator is gated off. The dynamic power consumption is listed in Column 4. Column 5 reports the layout area of the regenerators. From Table II we observe that both the dynamic power consumption and the layout area of TMR based approach is higher than the split-output based regenerator. For the split-output based approach, the leakage current is slightly more than the regular regenerator as well as the TMR based regenerator due to the presence of non-rail voltages.

From Tables I and II we conclude that the performance of the split-output inverter based regenerator hardening approach is better than the TMR approach (except for an increase in standby leakage). Therefore, we present detailed results for the split-output inverter based approach in Table III. The results are presented when B1 (B1d) directly drives B4 (B4d) (i.e. B2, B3, B2d and B3d are not used) in the split-output inverter based radiation hardened regenerator shown in Figure 6. In other words, the node $n1\_1n$ ($n1\_2n$) of the NAND gate B1 (B1d) drives both the inputs of the inverter B4 (B4d). Table III reports (on $RCLK$) the effect (on $RCLK$) of radiation strikes at different nodes in the split-output inverter based regenerator circuit. Again, all measurements are taken at $RCLK$. Column 1 lists the nodes where a radiation particle strike occurs. Row 1 reports the results obtained under normal operation (when no radiation particle strike occurs). Rows 2 through 11 report the results for radiation strikes at the different nodes of the regenerator circuit. The last row of the table shows the worst case results over the strikes at all nodes. It can be seen that the worst case jitter occurs when a radiation particle strikes node $n5$ in the regenerator.

We observe from Tables I and III that the split-output inverter based clock regenerator circuit is tolerant to radiation particle strike up to $Q = 150fC$ with $\tau_\alpha = 150ps$ and $\tau_\alpha = 38ps$. This approach is more effective than the TMR approach in reducing the radiation-induced clock jitter. Note that both the split-output inverter and the TMR approach are able to completely eliminate radiation-induced race conditions.

V. CONCLUSIONS

Single event upsets (SEUs) are becoming increasingly problematic for both combinational and sequential circuits with device scaling, lower supply voltages and higher operating frequencies. Recently, it has been reported that radiation strikes on the clock nodes in regional clock regenerators contribute heavily (∼20%) to the overall sequential SER. In this paper, we present two radiation hardened designs for the regional clock regenerators, – the first uses a triple modulo redundancy (TMR) approach, and the second is a split-output SEU tolerant inverter approach. Experimental results demonstrate that both our clock regenerator hardening approaches eliminate radiation-induced race conditions for Q up to 150fC. The TMR and the split-output inverter based approaches reduce the radiation-induced clock jitter to 58.2ps and 30.1ps, respectively. The split-output inverter based approach has a slight advantage over the TMR based approach with respect to layout area and dynamic power consumption. Hence, we conclude that the split-output inverter based clock regenerator hardening approach is better than the TMR approach.

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Circuit	Jitter(ps)		Rise Time(ps)		Fall Time(ps)		Pulse Width(ps)	
	Rise	Fall	Min	Max	Min	Max	Min	Max
No Strike	3.7	0.0	31.3	31.4	29.3	29.3	288.3	292.0
n1_1p	8.3	7.3	31.0	31.7	28.6	29.4	281.3	292.0
n1_2p	7.9	6.2	30.8	31.5	28.6	29.3	282.1	292.0
n4_1p	11.2	22.8	30.5	31.5	28.8	37.4	288.3	318.3
n4_2p	9.4	16.5	30.7	31.5	28.8	35.3	288.3	312.5
n1_1n	5.3	20.9	30.4	31.4	28.7	37.0	291.9	318.1
n1_2n	5.1	16.5	30.9	31.6	28.7	35.8	291.9	313.5
n4_1n	6.4	5.4	31.0	31.9	28.2	29.4	285.9	294.9
n4_2n	6.2	4.7	30.7	31.6	28.2	29.4	285.9	294.3
n5	25.0	30.1	28.2	36.6	25.5	36.3	273.9	309.0
n6	14.1	15.6	24.6	47.3	23.6	45.2	281.4	300.7
Worst Case	25.0	30.1	24.6	47.3	23.6	45.2	273.9	318.3

TABLE III

SPLIT-OUTPUT INVERTER BASED SOLUTION

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