A Novel, Highly SEU Tolerant Digital Circuit Design Approach

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***Abstract*— In this paper, we present a new radiation tolerant CMOS standard cell library, and demonstrate its effectiveness in implementing radiation hardened digital circuits. We exploit the fact that if a gate is implemented using only PMOS (NMOS) transistors then a radiation particle strike can result only in logic a 0 to 1 (1 to 0) flip. Based on this observation, we derive our radiation hardened gates from regular static CMOS gates. In particular, we separate the PMOS and NMOS devices, and split the gate output into two signals. One of these outputs of our radiation tolerant gate is generated using PMOS transistors, and it drives other PMOS transistors (only) in its fanout. Similarly, the other output (generated from NMOS transistors) drives only other NMOS transistors in its fanout. Now, if a radiation particle strikes one of the outputs of the radiation tolerant gate, then the gates in the fanout enter a high-impedance state, and hence preserve their output values. Our radiation hardened gates exhibit an extremely high degree of SEU tolerance, which is validated at the circuit level. Using these gates, we also implement circuit level hardening based on logical masking, to selectively harden those gates in a circuit which contribute most to the soft error failure of the circuit. The gates with a low probability of logical masking are replaced by SEU tolerant gates from our new library, such that the digital design achieves a 90% soft error rate reduction. Experimental results demonstrate that this reduction is achieved with a modest layout area and delay penalty of 62% and 29% respectively, for area mapped designs. In contrast with existing approaches, our approach results in SEU immunity for extremely large critical charge values (>650fC).**

I. Introduction

Single event upsets (SEUs) (or single even transients (SETs)) have become increasingly problematic for both combinational and sequential VLSI circuits in the deep submicron (DSM) era [1], [2], [3], [4], [5]. This is due to continuously decreasing feature sizes, lower supply voltages and higher operating frequencies which cause a reduction in the noise margins of VLSI designs. Many critical applications such as biomedical, space and military electronics as well as several mainstream computing applications demand reliable circuit functionality. Therefore, the circuits used in these application must be tolerant to SEU/SET events and therefore, these circuits are designed using circuit hardening approaches.

The current pulse that results from a particle strike is traditionally described as a double exponential function [8]. The expression for the pulse is

$$i_{seu}(t) = \frac{Q}{(\tau_\alpha - \tau_\beta)}(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}) \quad (1)$$

Here Q is the amount of charge deposited as a result of the ion strike, while τ_α is the collection time constant for the junction and τ_β is the ion track establishment time constant. Time constants τ_α and τ_β depend upon several process related parameters, and typically τ_α is on the order of 200ps and τ_β is on the order of tens of picoseconds [4], [6].

There has been a great deal of work on radiation hardened circuit design approaches [6], [5], [9], [7], [10], [13]. Although these approaches increase the circuit reliability to SEU/SET events, the cost (in terms of area, delay and power) associated with these approaches is high, which is unacceptable for high-volume mainstream applications. Also these approaches provide SEU tolerance to strikes by radiation particles with moderate energy levels. In other words, the increase in critical charge Q_{cri} (the minimum amount of charge required to cause an SEU event [2]) achieved by traditional approaches are not very high. Therefore, there is a need for a radiation hardening approach which can provide radiation tolerance against a very large values of Q_{cri}, with comparable or smaller overheads.

In this paper, we present novel circuit design approach for radiation tolerant standard cells. We exploit the fact that if a gate is implemented using only PMOS (NMOS) transistors then a radiation particle strike can result only in logic 0 to 1 (1 to 0) flip [9], [10] and use this idea to derive our radiation hardened gates from regular static CMOS gates. At the circuit level, to keep the area and delay overheads low, we selectively replace unhardened gates with our hardened gates using a logical masking based analysis [6], [3]. We describe a methodology to protect only those gates in the circuit which are the significant contributers to the soft error failure rate of the circuit. Our radiation hardening approach replaces the gates in a circuit to achieve a soft error failure rate reduction by an order of magnitude, with moderate a delay overhead of 29% and area overhead of 62% on average (compared to regular circuits).

The main contributions of this paper are:

- We present a novel circuit design approach for radiation tolerant standard cells.
- We selectively protect gates in a circuit to achieve soft error failure rate reduction by an order of magnitude. We only protect those gates in a circuit which contribute most to the soft error failure rate of the circuit.
- The critical charge for the radiation tolerant circuits implemented using our approach is dramatically higher (greater than 650fC) compared to the past approaches [5], [6], [7].

The rest of the paper is organized as follows. Section II

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briefly discusses some previous work in this area. In Section III we describe our radiation hardening design approach for combinational circuits. In Section IV we present experimental results, followed by conclusions in Section V.

II. Previous Work

There has been a great deal of work on radiation hardened circuit design approaches. Several papers report on experimental studies in the area of logic circuits [11], [2], [5], [6], while others have focused on memory design [1], [2], [12], [10], [13]. Since memories are particularly susceptible to SEU/SET events, these efforts were crucial to space and military applications. Some other approaches perform modeling and simulation of radiation events [14], [15].

Circuit level hardening approaches use special circuit design techniques that reduce the vulnerability of a circuit to radiation strikes [6], [5], [9], [10], [13]. In [6], the authors selectively size up the gates in a digital design to increase the radiation tolerance of the design. A larger gate has higher drive capability and also a higher node capacitance, which increases its radiation immunity compared to a smaller gate. The authors protect gates in a circuit which contribute most to the soft error failure rate of the logic circuit. These sensitive gates in a circuit are identified by using a logical masking [6] analysis. In this paper, we also use logical masking to identify and harden these sensitive gates (using *our* gate hardening technique) in a circuit.

In [10], the authors proposed an SEU immune flip-flop design and also made the following observation: a particle hit induces a current which always flows from the n-type diffusion to the p-type diffusion through a pn junction. This means that if a flip-flop is made up of only PMOS (NMOS) transistors, then a radiation particle strike cannot flip the node voltage from 1 to 0 (0 to 1). The authors of [10] use this observation to design a SEU hardened flip-flop (with two inputs and two outputs) by separating the NMOS and the PMOS transistors in the flip-flop. However, their flip-flop design has significantly higher leakage currents due to non-rail voltages at some nodes. The authors of [13] alleviates this problem by adding few more transistors to the SEU tolerant flip-flip design of [10]. In [9], the author borrows the idea of [10] to design a SEU tolerant standard cell library. However, these hardened cells have significantly larger leakage currents due to non-rail voltage levels at the output nodes of the gates. This is a significant problem because leakage power in today's technologies is comparable to or greater than switching power. In contrast to this, our SEU tolerant standard cell design does not have high leakage currents. Through SPICE simulations we found that our SEU tolerant standard cells have 2 order of magnitude lower leakage compared to the SEU tolerant gates of [9]. The author of [9] also did not describe a methodology to implement a radiation tolerant circuit using the SEU tolerant standard cell library, and hence did not report the area and delay overhead of the resulting radiation tolerant circuit. In this paper, we provide a methodology to selectively harden gates (based on their logical masking probability) in a circuit using our SEU tolerant gates, and also present the delay and the area results for the radiation tolerant circuits.

III. Our Approach

In Section III-A, we discuss our radiation-tolerant standard cell design approach. We discuss our circuit level hardening approach in Section III-B.1. For circuit hardening, we selectively replace those gates in a circuit which contribute most towards the soft error failure rate of the circuit. Our circuit level hardening approach achieves a soft error failure rate reduction by an order of magnitude (90% reduction in soft error rate). In Section III-C, we present an analysis to estimate the critical charge for the hardened circuit obtained by using our approach.

A. Radiation Tolerant Standard Cell Design

As mentioned in Section II, a radiation particle strike induces a current which always flows from the n-type diffusion to the p-type diffusion through a pn junction [10]. This implies that if a gate is made up of only PMOS (NMOS) transistors then a radiation particle strike cannot flip the node voltage from 1 to 0 (0 to 1). In other words, if a particle strikes the diffusion of a PMOS transistor of an inverter whose output is at logic 1, then this particle strike will not cause the output node voltage to flip. Similarly, a particle strike at the diffusion of a NMOS transistor of the inverter (with an output node at logic 0) will not result in SET. This is a key idea since tells us that if a logic circuit is made up only PMOS (NMOS) transistors, then that logic circuit will be tolerant to node flips from 1 to 0 (0 to 1). We use this concept to design highly SEU tolerant standard cell gates.

Consider two regular inverters as shown in Figure 1 (a). Radiation particle strikes at M1 and M2 of INV1 can result in both positive or negative glitches[1] at $out1$ node (since the PMOS and NMOS transistors are both connected to the $out1$ node). The voltage glitch at the $out1$ node can affect the voltage of node $out2$, which can lead to an SEU. To avoid an SEU due to radiation particle strikes at the diffusions of M1 or M2, we need to harden INV1. Figure 1 (b) shows our radiation tolerant inverter circuit. First, we will describe how INV1 of Figure 1 (b) behaves as an inverter and then we will explain why it is tolerant to a radiation particle strike.

Our hardened inverter INV1 shown in Figure 1 (b) has 2 inputs (inp and inn) and 2 outputs ($out1p$ and $out1n$). Both inputs and both outputs of INV1 are of the same polarity. Note that the output nodes $out1p$ and $out1n$ of INV1 respectively drive only PMOS or NMOS transistors of the gates in their fanout ($out1p$ drives M4 of INV2 and $out1n$ drive M3 of INV2 in Figure 1 (b)). Also, note that the inverter INV2 is also modified such that two different input signals (of the same polarity) drive the transistors M3 and M4. In the sequel, we refer to a gate (such as inverter INV2 of Figure 1 (b)) whose inputs to PMOS and NMOS transistors are separated, as a *modified* gate. Note that such a

[1] A positive glitch is defined as the condition in which the node voltage switches from 0 to 1 and then back to 0. Similarly, a negative glitch is defined as a node voltage transition from 1 to 0 to 1.

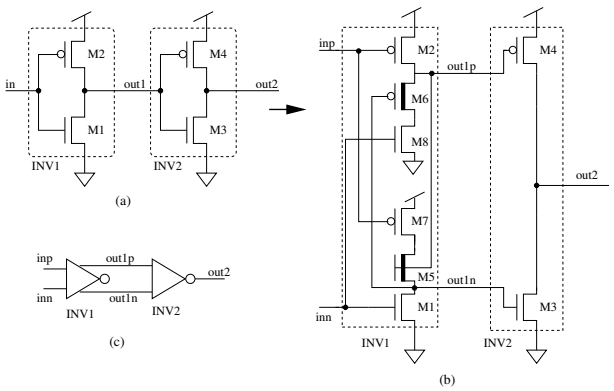

Fig. 1. Design of an SEU tolerant inverter

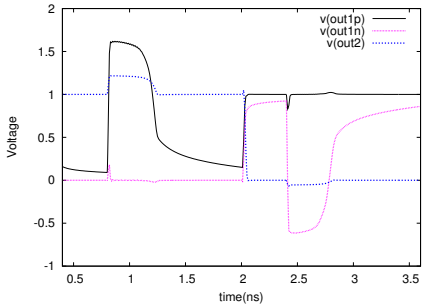

Fig. 2. Radiation particle strike at $out1p$ and $out1n$ of INV1 of Figure 1d

gate has $2n$ inputs (compared to n inputs for any unmodified gate).

Our hardened inverter INV1 of Figure 1 (b) works as follows. Assume that both inn and inp are at a logic 0 value. Therefore, $out1p$ and $out1n$ are at logic 1. Now assume that both inn and inp transition to logic 1 due to which transistor M1 turns on and M2 turn off. The turning on of M1 pulls the node $out1n$ down to logic 0 which then turns on M6. Since M6 is ON and M8 is also ON, $out1p$ is driven to a weak logic 0[2]. Both $out1p$ and $out1n$ are now at logic 0, due to which the output of INV2 ($out2$) goes to logic 1. Now when both inputs of INV1 (inn and inp) change to logic 0, then transistor M1 turns off and M2 turns on. As M2 is on, $out1p$ charges to logic 1, which turns M5 on and hence, node $out1n$ is pulled to a weak logic 1 (VDD- V_T^{M5} volts) since M7 is also ON. Since $out1n$ and $out1p$ are both at logic 1, the node $out2$ is driven to logic 0. Thus, INV1 of Figure 1 (b) behaves like an inverter, with the output node $out1p$ ($out1n$) switching between VDD and $|V_T^{M6}|$ (VDD - V_T^{M5} and GND). Note that the transistors M5 and M6 of INV1 of Figure1 (b) are selected to be low threshold voltage transistors (indicated by a thicker line in the figure). This is done so as to increase the voltage swing at nodes $out1p$ and $out1n$, and bring them closer to the rail voltages. Also, note that the reduced voltage swings at $out1p$ and $out1n$ do not increase the leakage currents in INV2 of Figure 1 (b). This is because, when the node $out1p$ is at $|V_T^{M6}|$ then $out1n$ is at GND due to which M3 is completely turned off while M4 is turned on. Similarly, when the $out1p$ is at VDD then $out1n$ is at VDD-V_T^{M5} and hence M3 is turned on while M4 is completely turned off. Therefore, the leakage currents in INV2 do not increase due to non-rail voltage swing at its inputs.

The inverter INV1 of Figure 1 (b) is tolerant to a radiation strike at $out1p$ and $out1n$. Consider the case when the nodes inp and inn are at VDD, which implies that $out1p$ and $out1n$ are at $|V_T^{M6}|$ and GND respectively, and $out2$ is at the VDD value. Now suppose a radiation particle strikes at node $out1p$ (the radiation particle strikes either M2 or M6) which increases the voltage at node $out1p$ to VDD (due to the positive charge collection at $out1p$). Due to this, M4 of INV2 turns off and M5 turn on. However, the node $out1n$ remains at GND value because M7 is in cutoff. Therefore M3 also remains off. Thus, the node $out2$ remains at the VDD value in a high impedance state. Eventually, the charge collected at $out1p$ dissipates through M6 and M8 (since inp and inn are at VDD) which brings the voltage at $out1p$ node back to $|V_T^{M6}|$. At this point, M4 turns on again. In this way, the radiation strike at $out1p$ does not affect the $out2$ node voltage value. Similarly, a particle strike at $out1n$ does not affect the node $out2$ when inn and inp are at the GND value. A radiation particle at $out1p$ ($out1n$) node can only result in a positive (negative) glitch since only PMOS (NMOS) transistors are connected to it. Also this positive (negative) glitch at $out1p$ ($out1n$) does not propagate to $out2$. This is because the $out1p$ ($out1n$) node drives only the PMOS (NMOS) transistor of INV2 which goes into cutoff mode when a positive (negative) glitch appears at $out1p$ ($out1n$) node. A radiation particle strike at M8 can be of any significance only when $out1p$ is at the VDD value (since a radiation particle strike at the NMOS transistor can only result in a negative glitch). However, when $out1p$ is at VDD, M6 is turned off and hence a particle strike at M8 does not affect $out1p$ node voltage. Similarly, a radiation particle strike at M7 does not affect the voltage of the $out1n$ node. In this way, INV1 of Figure 1 (b) is tolerant to radiation particle strikes since a particle strike at either of its output nodes does not affect the output of its fanout gates (like $out2$ of INV2 of Figure 1 (b)). To validate this, we implemented inverters INV1 and INV2 of Figure 1 (b) using a 65nm PTM [16] model card with VDD = 1.0V. We simulated radiation particle strikes at the $out1p$ (at time = 0.8ns) and $out1n$ (at time = 2.4ns) nodes, with $Q = 150fC$, $\tau_\alpha = 150ps$ and $\tau_\beta = 38ps$. These values of Q, τ_α and τ_β were obtained from [6]. The voltage waveforms at $out1p$, $out1n$ and $out2$ are shown in Figure 2. We observe from Figure 2 that radiation particle strikes at the $out1p$ (at time = 0.8ns) and $out1n$ (at time = 2.4ns) nodes do not affect the logic level at the $out2$ node. Therefore, our radiation hardened inverter INV1 of Figure 1 (b) is tolerant to a radiation strike at $out1p$ and $out1n$.

Our radiation hardening approach can be applied to any static CMOS gate, including complex gates. Figure 3 (a) shows a radiation tolerant 2-input NAND gate designed using our approach. As shown in Figure 3 (a), the radiation tolerant 2-input NAND gate has a total of 4 inputs and 2 outputs. The

[2]The node $out1p$ falls to $|V_T^{M6}|$ volts. Note that V_T^{M6} is the threshold voltage of PMOS transistor M6.

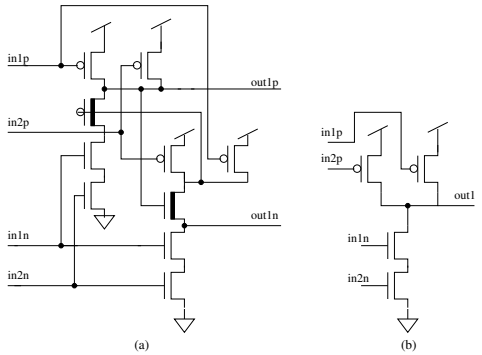

Fig. 3. a) Radiation tolerant 2-input NAND gate, b) *modified* regular 2-input NAND gate

inputs $in1p$ and $in1n$ ($in2p$ and $in2n$) correspond to the first input $in1$ (second input $in2$) of a regular 2-input NAND gate. The two outputs $out1p$ and $out1n$ of the radiation tolerant 2-input NAND gate of Figure 3 drive the PMOS and the NMOS transistors of the gates in its fanout. In general, an n-input static CMOS gate requires $4n + 2$ transistors when implemented in our radiation hardening approach, in contrast to $2n$ transistors for its regular static CMOS counterpart. Figure 3 (b) shows the *modified* regular 2-input NAND gate circuit.

B. Circuit Level Radiation Hardening

A simple way to harden a circuit would be to replace all gates in the circuit with their hardened counterparts. Although this approach provides 100% SEU/SET tolerance however, it can result in a large delay and area overhead for the circuit. Alternatively, we can selectively protect only those gates in a circuit which have a significant contribution to the soft error failure rate of the circuit. Using this approach, we can achieve a reduction in soft errors, with smaller area and delay overheads. Whether a voltage glitch induced by a radiation particle strike at any gate in a circuit propagates to the primary outputs and results in a failure depends upon three masking factors. These masking factors are electrical, logical and temporal masking [3], [6]. Electrical masking occurs when a voltage glitch induced by a radiation particle attenuates as it propagates through the circuit to the primary outputs. Electrical masking can reduce the voltage glitch magnitude to a value which cannot cause any soft errors. Note that with device scaling, the glitch attenuation due to electrical masking has diminished significantly, and hence electrical masking has a small effect on the overall circuit failure rate [17], [6]. Temporal masking occurs if a voltage glitch due to a radiation particle strike reaches the primary outputs of a circuit at an instant other than the latching window of the sequential elements of the circuit. Temporal masking inherently provides some radiation tolerance to a logic circuit against SEUs, and hence cannot be used to identify sensitive gates in a circuit. Logical masking occurs when there is no functionally sensitizeable path from the node in a circuit where the radiation particle strikes to any primary output of the circuit. Hence, the logical masking of a gate can be estimated using logic information. We use the logical masking to identify the sensitive gates in a circuit.

The sensitive gates in a circuit are those gates which have small values for these masking factors, and hence these gates contribute significantly to the soft error failure of the circuit. These are the gates in a circuit which we need to protect by replacing them with our hardened gates, to significantly improve the radiation tolerance of the circuit. As mentioned above, we use logical masking to identify such sensitive gates in a circuit. The approach we use identify these gates is described next.

1) Identifying and protecting sensitive gates in a circuit: To identify the sensitive gates in a circuit we need to compute a measure of the logical masking at all gates in the circuit. The logical masking at a gate is computed as the probability of the absence of a functionally sensitizable path from the gate to any primary output of the circuit. We computed the probability of logical masking at a gate in the same manner as proposed in [6]. As mentioned in [6], the probability of logical masking (P_{LM}) at a gate G is $1 - P^G_{Sen}$ where P^G_{Sen} is the probability of sensitization of gate G. The probability of sensitization is defined as the probability of the existence of at least one functionally sensitizable path from the gate G to any primary output of the circuit.

To calculate the probability of sensitization P_{Sen}, we apply N random vectors to primary inputs of a circuit. For each vector, we perform fault simulation on all gates in the circuit to determine if the fault is sensitized and observable at one or more primary output. For a gate G we count the number of vector (S_G) out of the N applied random vectors which were able to sensitize any fault (both G-stuck-at-1 and G-stuck-at-0) at G to the primary output(s). Note that S_G is the summation of the number of vectors which simulate the fault at G (when the output of G is at logic 0 or logic 1). Now we define the sensitization probability for the gate G (P^G_{Sen}) as S_G/N. A gate which has high probability of sensitization is a sensitive gate which we need to protect.

After we compute the sensitization probabilities (or logical masking probabilities) for all the gates in the circuit (η), we identify and protect the sensitive gates using Algorithm 1. For a given circuit η, first we sort all gates $G \in \eta$ in a decreasing order of their sensitization probabilities, and store them in a list L. Then we protect the top K gates (by replacing them with our hardened gates) in the list L that achieve the required tolerance against radiation particle strikes. The resulting hardened circuit is referred as η^*.

Algorithm 1 Radiation Hardening for a Circuit η

```
Harden_circuit(η)
L = sort(G ∈ η, P^G_Sen)
i = 0
while required tolerance to SEU is not achieved do
  G = L(i)
  Replace G by G_hardened
  i = i + 1
end while
return η*
```

In this paper, we call a circuit protected when the soft error rate reduces by an order of magnitude. To achieve that, we

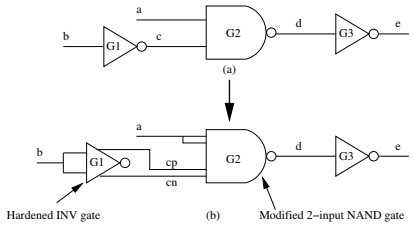

Fig. 4. Part of a circuit

protect gates in the list L (in decreasing order of sensitization probability) until 90% $coverage$ is achieved. The $coverage$ is defined as [6]

$$coverage = \frac{\sum_{\forall\ hardened\ gate\ G \in \eta^*} P^G_{Sen}}{\sum_{\forall\ gate\ G \in \eta} P^G_{Sen}} \cdot 100 \quad (2)$$

It was demonstrated in [6] that $coverage$ is a good estimate for soft error failure rate reduction. 90% coverage corresponds to an order of magnitude reduction in soft error rate. To achieve 90% coverage, we need to protect K gates using Algorithm 1. Note that we protect a gate G by replacing it with its hardened version which is obtained by our gate hardening technique as described in Section III-A. For example, consider a circuit fragment shown in Figure 4 (a). Note that all the gates in Figure 4 (a) are regular gates. Suppose that the gate $G1$ has a very high sensitization probability and it needs to be protected such that *a radiation particle strike at its output should not affect the gates in its fanout ($G2$)*. Now we replace the gate $G1$ of Figure 4 (a) with our hardened inverter gate of Figure 1 (b). The resulting circuit is shown in Figure 4 (b). While replacing the gate $G1$ with its hardened version, we also need to replace all the regular gates in its fanout ($G2$) with their *modified* regular gates[3] because the hardened gate has two outputs (one output drives only the PMOS transistors of the gates in its fanout and second drives the NMOS transistors only). Therefore, we replace $G2$ in Figure 4 (a) with its *modified* regular version in Figure 4 (b).

The gates at the primary output of a circuit are always sensitive and have a sensitization probability equal to 1. Therefore, we always need to replace these gates with their hardened counterparts. However, the replacement of a regular gate (which has one output) with its hardened counterpart results in two outputs. Therefore, the two outputs of each hardened gates that drives the primary outputs of the circuit now need to drive the flip-flop (which samples the primary output values). To achieve that, we can use the SEU tolerant flip-flop design proposed in [13], which is widely used for implementing radiation tolerant VLSI circuits. The radiation tolerant flip-flop of [13] has dual inputs which correspond to the input D of the regular flip-flop. One of the 2 inputs of the radiation tolerant flip-flop only drives PMOS transistors and the other input drives only NMOS transistors. Therefore, our hardened gates are compatible with radiation tolerant flip-flop of [13].

[3]As mentioned earlier, a $modified$ regular n-input gate is same as the regular n-input gate with its inputs to the PMOS and the NMOS transistor disconnected from each other resulting in total of $2n$-inputs. For example, INV2 of Figure 1 (b) is a $modified$ regular inverter. The gate of Figure 3 (b) is a $modified$ regular NAND2 gate.

C. Critical charge for radiation hardened circuits

From the waveforms shown in Figure 2 we can observe that even a large amount of charge dumped by a radiation strike at the output of our hardened gate does not affect the fanout gates' output. Therefore, our approach provides 90% tolerance (90% coverage) to the radiation particle strikes from very high energy radiation particles. However, the frequency of circuit operation imposes a limit on the magnitude of the charge dump that can be tolerated by a hardened circuit implemented using our approach. This is explained next.

Consider a part of the hardened circuit shown in Figure 5 (a). The waveform of the various nodes, along with CLK, are shown in Figure 5 (b). In Figure 5 (b), dark lines correspond to the normal operation (no radiation particle strike). The clock period of the hardened circuit is T and the propagation delay of INV2 is d. Let us assume that a high energy radiation particle strikes the $out1p$ node sometime before $t1$. The particle induces a voltage glitch with the pulse width greater than T and the voltage glitch rises before $t1$ and falls after $T + t1$. As the node $out1p$ switches to logic 1 before $t1$ when $out1n$ is at logic 0, therefore, the node $out2$ enters the high impedance state. At time $t1$, $out1n$ also switches high (due to switching of in to low), and then $out2$ comes out of the high impedance state and switches to logic 0 at the same time as in the normal operation. Now at time $T + t1$, $out1n$ switches to logic 0, and hence the $out2$ node again enters a high impedance state (since $out1p$ is still at logic 1 due to the radiation strike). When $out1p$ fall to logic 0 then $out2$ switches to logic 1 as shown in Figure 5. However, note that the rising $out2$ transition is delayed compared to the normal operation. Due to this, the primary output computation may get delayed, potentially resulting in a circuit failure. If the voltage glitch at $out1p$ had fallen on or before time $T + t1$, then the $out2$ node would have switched at the same time as the normal operation, and hence no circuit failure would have been encountered. Thus, the pulse width of the voltage glitch induced by a radiation particle strike at $out1p$ should be less than the clock period T. Hence the critical charge (Q_{cri}) for the circuit is the maximum amount of charge dumped by a radiation particle such that a voltage glitch of pulse width T is encountered in the circuit. We have experimentally determined that a very large amount of charge should be dumped by a radiation particle, in order to generate a voltage glitch with the pulse width equal to the clock period of a design. This experiment was conducted for the smallest (most sensitive to radiation) gate in our library. This is quantified in the sequel. Hence our approach is extremely robust to radiation strikes.

Now consider a radiation particle strike just after $t1 + d$, at node $out1n$. Due to the particle strike, $out1n$ switches to logic 0 at $t1 + d$, $out2$ enters the high impedance state with the correct logic value of 0. Even if the pulse width of the negative voltage glitch at $out1n$ is greater than T, it is of

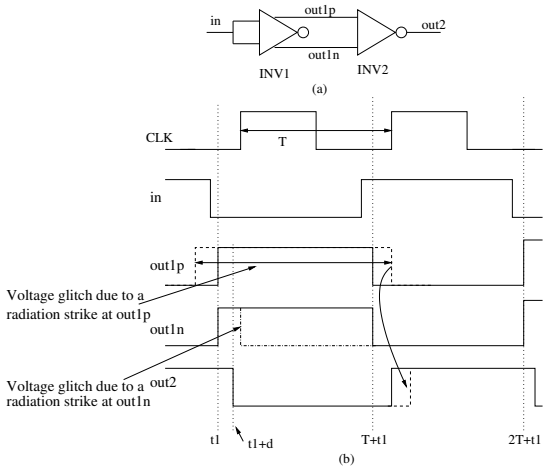

Fig. 5. a) Circuit under consideration b) Waveform at different nodes

no consequence to the $out2$ node voltage. This is because at time $T + t1$ $out1p$ switches to logic 0, hence $out2$ switches to logic 1 at the same time as in normal operation. However, if a radiation particle strikes the $out1n$ node between $t1$ and $t1 + d$ then $out2$ enters the high impedance state with the wrong logic value of 1 (since $out1n$ switched to logic 0 before the $out2$ node switches to logic 1).

To summarize, the maximum tolerable radiation induced glitch width for our approach is T. Also, our hardened gates are vulnerable to radiation particle strikes during the time when their fanouts are computing their outputs. For the circuit shown in Figure 5 (a), INV1 is vulnerable to radiation particle strikes only between $t1$ and $t1 + d$. However, the probability of a particle to strike the $out1n$ node during this time interval is very low[4] and hence, it does not have any impact on the overall soft error rate reduction obtained by our approach.

Our approach can tolerate radiation induced glitch with a maximum width of T, the clock period of the design. Hence, our circuit hardening approach provides tolerance against radiation particles of very high energy. In the experimental section, we have quantified the critical charge (Q_{cri}) values of various benchmark circuits which are hardened using our approach.

IV. Experimental Results

To evaluate the performance of our circuit hardening approach, we applied our technique to several ISCAS and MCNC benchmark circuits. We implemented a standard cell library (L) using 65nm PTM [16] model cards, with VDD = 1.0V. Our standard cell library consists of regular INV2X, INV4X, NAND2, NAND3, NOR2 and NOR3 gates. We also designed *modified* versions as well as the hardened versions of all the gates in the library L. We generated the layouts for all these gates using CADENCE SEDSM [20] tools. We mapped several ISCAS and MCNC benchmark circuits using the library L, for both area and delay optimality. From a mapped design, we first computed the sensitization probability of all the gates in the design. Then we selectively harden (to achieve 90% soft error rate reduction) the sensitive gates in the design based on their sensitization probability, using Algorithm 1. The area and the delay results of the regular (unhardened) and the hardened circuits are reported in Table I.

Table I reports the layout area results for several benchmark circuits which are mapped for both area and delay optimality. Note that the layout area for a design was computed by adding the layout area of all the gates in the circuit. Column 1 reports the circuit under consideration. Column 2 (3) reports the area (in μm^2) for area mapped designs using the traditional (our) approach. Columns 9 (10) report the areas for delay mapped designs using traditional (our) approach. Column 4 reports the percentage area overhead for our radiation-hardened design. Column 7 reports the percentage area overhead for our radiation-hardening approach for delay mapped designs. We observe from Table I that the average area overhead for our hardening approach is 62.4% and 58.15%, for area and delay mapped designs respectively.

The delay penalty associated with applying our radiation hardening approaches is also presented in Table I. Note that the delay for a design reported in Table I is the summation of the combination circuit delay (D), the setup time (T_{su}) of the flip-flop and the clock to output (T_{cq}) delay of the flip-flop. Therefore, Table I reports the clock period ($T = D+T_{su}+T_{cq}$) of a design. The delay of a design is obtained using a static timing analysis tool for regular designs. We modified the static timing analysis tool to compute the delay of our radiation hardened designs. First, we characterized all hardened gates to compute 2-dimensional pin-to-output delay lookup tables for different load values on the two outputs ($outp$ and $outn$). Note that for any hardened gate, the output $outp$ falls after the falling of $outn$, and $outn$ rises after the rising of $outp$. Therefore, the rising (falling) delay of a hardened gate is obtained from the rising (falling) delay of the $outn$ ($outp$) node. After the characterization of all hardened gates, we use the modified static timing analysis tool to compute the delay of radiation hardened circuits using these 2-dimensional delay lookup tables. T_{su} and T_{cq} are obtained using a unhardened D flip-flop for a regular design and a SEU tolerant flip-flop [13] for the hardened design. Table I also reports the critical charge value for the radiation hardened design. Columns 5 and 6 report the clock period (in ps) for a regular area mapped design and the hardened area mapped design. Column 7 reports the percentage delay overhead (or clock period overhead) for the radiation-hardened design. Column 8 report the critical charge (in fC) for the hardened design, as described in Section III-C. Note that the Q_{cri} value is obtained for $\tau_\alpha = 150ps$ and $\tau_\beta = 38ps$ as reported in [6]. We use the smallest gate in our library to find this value. Columns 12 to 15 report the same results as Columns 5 to 8 but for delay

[4]As per [18], [19], the maximum solar proton fluence for particles of energy $>$ 1MeV based on the JPL- 1991 model is $2.91 \times 10^{11}/cm^2/year$ with 99% confidence. The maximum area of a hardened gate in our library is $7.69 \times 10^{-8} cm^2$ and the maximum delay of any gate is 70ps. Using these values, it can be shown that the probability of a radiation particle to strike $out1n$ between $t1$ and $t1 + d$ is 4.96×10^{-14}.

Ckt	Area Map							Delay Map						
	Area (μm^2)			Delay (ps)			Q_{cri}	Area (μm^2)			Delay (ps)			Q_{cri}
	Regular	Hardened	% Ovh.	Regular	Hardened	% Ovh.	(fC)	Regular	Hardened	% Ovh.	Regular	Hardened	% Ovh.	(fC)
alu2	667.89	1080.92	61.84	1068.28	1309.45	22.58	>650	740.39	1160.24	56.71	893.62	1129.06	26.35	>650
apex7	417.43	699.96	67.68	495.00	636.84	28.65	520	465.76	748.96	60.80	451.95	565.13	25.04	330
C1355	949.54	1627.32	71.38	636.95	830.21	30.34	>650	1015.89	1699.16	67.26	639.86	799.49	24.95	>650
C1908	908.68	1486.05	63.54	924.56	1206.91	30.54	>650	1020.73	1624.68	59.17	926.47	1205.01	30.06	>650
C3540	2177.23	3312.64	52.15	1217.71	1582.78	29.98	>650	2401.32	3571.66	48.74	1139.45	1530.20	34.29	>650
C432	348.88	609.23	74.62	856.80	1120.31	30.76	>650	402.93	684.80	69.96	839.02	1094.36	30.43	>650
C499	974.59	1634.13	67.67	670.97	868.22	29.40	>650	1069.50	1756.28	64.22	655.22	784.30	19.70	>650
C880	772.90	1293.15	67.31	923.22	1157.03	25.32	>650	828.71	1361.26	64.26	879.10	1069.67	21.68	>650
dalu	1569.98	2458.44	56.59	909.35	1241.81	36.56	>650	1799.78	2822.27	56.81	821.68	1157.31	40.85	>650
alu4	4093.89	5945.08	45.22	679.15	818.10	20.46	>650	4543.40	6221.46	36.93	625.48	751.79	20.20	>650
frg2	1453.54	2302.90	58.43	679.32	905.38	33.28	>650	1768.15	2736.36	54.76	818.30	1098.05	34.19	>650
Average			62.40			28.90				58.15			27.98	

TABLE I

OVERHEADS AND Q_{cri} OF OUR RADIATION HARDENED DESIGN APPROACH

mapped designs. From Table I, we observe that the average delay overhead of our radiation hardening approach is 28.9% and 28% for area and delay mapped designs respectively. We also observe that the critical charge for the radiation hardened design is a very large value. Traditional radiation hardening approaches such as [6], [7] protect against radiation strikes of at most ∼150fC. For all but one design, the critical charge is greater 650fC[5] for $\tau_\alpha = 150ps$ and $\tau_\beta = 38ps$. Therefore, for all practical purposes, our radiation hardening approach provides 90% coverage (soft error rate reduction by an order magnitude) against very high energy radiation particle strikes.

From Figure 2 we conclude that our radiation tolerant standard cells are very effective and they can tolerate high energy radiation particle strikes without affecting the state of gates in their fanout. We also conclude from Table I that our circuit radiation hardening technique provides good soft error rate reduction (by an order of magnitude) with a modest area overhead of 60% and delay overhead of 29% on average. The critical charge of the hardened circuit obtained using our approach is also a very large value (> 650fC in all but one example), which ensures correct circuit functionality in a heavily radiation prone environment.

V. CONCLUSIONS

In this paper, we present a new SEU tolerant CMOS standard cell library, and demonstrate its effectiveness in implementing digital circuits. It is known that if a gate is implemented using only PMOS (NMOS) transistors then a radiation particle strike can result only in a logic 0 to 1 (1 to 0) flip. We apply this concept to derive our radiation hardened standard cells. Our radiation hardened gates exhibit an extremely high degree of SEU tolerance compared to competing approaches. This is validated at the circuit level. We also implement circuit level hardening using logical masking, to selectively harden those gates in a circuit which contribute most to the soft error failure rate of the circuit. The gates with a low probability of logical masking are replaced by SEU tolerant gates from our new library, such that the digital design achieves 90% soft error rate reduction. Experimental results validate the claims of high radiation tolerance, which is achieved with a modest area and delay penalty of 62% and 29% for area mapped designs.

[5]The pulse width of the voltage glitch induced by a radiation particle strike with $Q >$ 650fC saturates to a value of 660ps.

REFERENCES

[1] T. May and M. Woods, "Alpha-particle-induced soft errors in dynamic memories," *IEEE Trans. on Electron Devices*, vol. ED-26, pp. 2–9, jan 1979.

[2] J. Pickle and J. Blandford, "CMOS RAM cosmic-ray-induced error rate analysis," *IEEE Trans. on Nuclear Science*, vol. NS-29, pp. 3962–3967, 1981.

[3] P. Shivakumar et al., "Modeling the effect of technology trends on the soft error rate of combinational logic," in *DSN '02: Proceedings of the 2002 International Conference on Dependable Systems and Networks*, 2002, pp. 389–398.

[4] P. Dodd and L. Massengill, "Basic mechanisms and modeling of single-event upset in digital microelectronics," *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 583– 602, 2003.

[5] R. Garg et al., "A design approach for radiation-hard digital electronics," in *Proceedings, IEEE/ACM DAC*, July 2006, pp. 773–778.

[6] Q. Zhou and K. Mohanram, "Gate sizing to radiation harden combinational logic," in *Proceedings, Computer-Aided Design of Integrated Circuits and Systems*, Jan 2006, pp. 155–166.

[7] C. Nagpal, R. Garg, and S. P. Khatri, "A delay-efficient radiation-hard digital design approach using CWSP elements," in *DATE*, 2008.

[8] G. Messenger, "Collection of charge on junction nodes from ion tracks," *IEEE Trans. Nuclear Science*, vol. 29, no. 6, pp. 2024–2031, 1982.

[9] J. Canaris, "An SEU immune logic family," in *Proceedings, 3th NASA Symposium on VLSI Design*, Oct 1991.

[10] S. Whitaker et al., "SEU hardened memory cells for a CCSDIS reed solomon encoder," *IEEE Trans. Nuclear Science*, vol. 38, no. 6, pp. 1471–1477, 1991.

[11] W. Massengill, M. Alles, and S. Kerns, "SEU error rates in advanced digital CMOS," in *Proc. Second European Conference on Radiation and its Effects on Components and Systems*, sep 1993, pp. 546 – 553.

[12] B. Gill et al., "An efficient BICS design for SEUs detection and correction in semiconductor memories," in *Proc. of DATE*, march 2005, pp. 592–597.

[13] M. N. Liu and S. Whitaker, "Low power SEU immune CMOS memory circuits," *IEEE Transactions on Nuclear Science*, vol. 36, no. 6, pp. 1679–1684, 1992.

[14] K. Hass and J. Gambles, "Single event transients in deep submicron CMOS," in *Proc. IEEE 42nd Midwest Symposium on Circuits and System*.

[15] A. Johnston, "Scaling and technology issues for soft error rate," in *Proc. Annual Research Conference on Reliability*, oct 2000.

[16] PTM, http://www.eas.asu.edu/ ptm.

[17] M. P. Baze et al., "Attenuation of single event induced pulses in CMOS combinational logic," *IEEE Trans. Nuclear Science*, vol. 44, pp. 2217–2223, Dec 1997.

[18] E. E. C. for Space Standardization, "Energetic particle radiation, http://www.spenvis.oma.be/spenvis/ecss/ecss09/ecss09.html."

[19] J. Feynman et al., *Interplanetary Proton Fluence Model: JPL 1991*. J. Geophys. Res. 98, A8, 1993.

[20] *Envisia Silicon Ensemble Place-and-route Reference*, Cadence Design Systems, Inc., 555 River Oaks Parkway, San Jose, CA 95134, USA, Nov 1999.