Clock Distribution Scheme using Coplanar Transmission Lines

Victor H. Cordero and Sunil P Khatri
Department of ECE, Texas A&M University

Abstract

The current work describes a new standing wave oscillator scheme aimed for clock propagation on coplanar transmission lines on a silicon die. The design is aimed for clock signaling in the Gigahertz range (we are able to achieve clock rates of 8GHz and above). The clock is transported as an oscillatory wave on a pair of conductors. An oscillatory standing wave is formed across a transmission line loop, which is connected beginning-to-end through a Mobius configuration. A single cross coupled inverter pair is required to maintain oscillation across the ring. The design is aimed to achieve low skew, low power and extreme high frequency global clock situations. The energy recycling nature of a standing wave along a transmission line allows us to keep very high frequencies oscillations along a conductor with almost no power consumption at all. A special wide input range driver was designed to convert the differential signals on the coplanar transmission lines into a square clock pulse for standard clock sinks. The design uses CMOS 90nm BSim3v model cards for all simulations, with the transmission lines implemented on Metal8.

1 Introduction

In current digital Integrated Circuit (IC) design, there is an increasing concern about the chip power budget. Metrics such performance per Watt have begun to be used by major processors companies such as Intel, AMD, etc. Low-cost embedded designs can only spare a limited amount of volume /cost/noise/power for heat dissipation systems for a particular chip. Further, high power consumption results in higher chip temperatures, which can have a detrimental effect on chip lifetimes and reliability. Traditionally, the highest power consumption in the chip is attributed to the global clock distribution network. The high-speed global clock signal must reach all the clocked elements within a chip with a low skew. At high frequencies, the RC delays of a wire (and its driver capacitance) produce a considerably skew between the clock generator and the clock receivers.

Conventional clock distribution topologies can be classified as: 1) Grids, 2) H-Trees, 3) Spices and 4) Hybrid topologies. All of them try to equalize the time of flight from generator to receiver. These schemes use a large number of repeaters to reduce the systematic skew and attempt to achieve a balanced clock load distribution to minimize the random skew.

1. Grids use a horizontal and vertical mesh of metal across the chip, with the clock injected from the middle or the edges. The random skew is reduced in this way, since all the clock lines are short circuited. However, their systematic skew is high. The total capacitance of a grid is quite high and hence, so is the power consumed in charging and discharging the grid.

2. H-Trees create a fractal ‘‘recursive-H’’ structure of wires for clock distribution. In this approach, all the end points receive the clock after it has traveled the same wire length, and after it has passed through the same number of drivers. Skew arises due to non-uniform clock loads along the tree, with opposite leaves exhibiting the highest skew. Repeaters are often used along the tree to propagate the clock to the end points with low systematic skew.

3. Spines use a couple of very wide metal tracks for clock propagation. They are routed on a few rows across the whole chip. A thin serpentine wire is laid out to each of the clock receivers, so that all the delays to different receivers are matched. A large capacitance, and high metal area usage, may arise if the total number of receivers is large.

4. Hybrid topologies combine the H-tree and the Grid schemes, and offers lower skew than any of these methods by themselves. The first clock level propagates as an H-tree toward multiple points on the die. Then the second level shorts these points together which lower systematic and uneven load based skew.

All of these schemes focus mostly on the primary goal of skew reduction, and offer little to mitigate power consumption. They all use buffers to charge/discharge the large total clock interconnect capacitance, with no effort towards energy recycling. With dies and frequencies of operation getting larger, the power dissipation due to clock interconnect, described by the equation $P=CV^2f$ (where C is the switched capacitance, V is the supply voltage and f is the clock frequency) grows quickly on the clock paths. For this reason, it is common for the clock network on a large die to consume close to 50% of the total power consumption.

An alternative way to propagate high frequency clock signals along metal strips has long been used by RF engineers. At very high frequencies (gigahertz and above) the signals wavelengths dimensions generate a varying voltage in the conductor, in the direction of wave propagation. At low frequencies, the wavelength of a signal is several orders of magnitudes longer the dimension of the conductor.

Waves can reflect back from the ends of open/shorted conductors if no proper impedance matching is performed. RF engineers use simple metal strips to emulate inductive and capacitive loads along a matching network.

This wave reflection behavior at the end of a conductor can also be exploited to generate oscillators. Such oscillators are categorized into 1) traveling wave and 2) standing wave oscillators.

Examples of *traveling wave oscillators* include the Rotary Clock [6, 7, 8, 9, 10] scheme, which was the original starting point for this project. The Rotary Traveling Wave Oscillator (RTWO) [6] creates a traveling wave within a closed-loop differential transmission line. Distributed CMOS inverters are placed along the ring to regenerate the wave, serving as transmission line amplifiers and to ensure rotational lock. This type of oscillator forms results in multiphase (360 degrees), evenly distributed square waves traveling along the transmission line ring. The energy is recirculated within the transmission line and very little energy goes into sustaining the wave. The energy consumption of this structure is I^2R, where this R is the resistance of the conductor. The power savings of the rotary clock are negated by the fact that along the ring, clock edges are out of phase, with phase changing from 0 to 180 degrees and then back to 0 degrees. This generates the additional undesirable design complication of having to adjust the phase of the clock edge for each clock receiver.

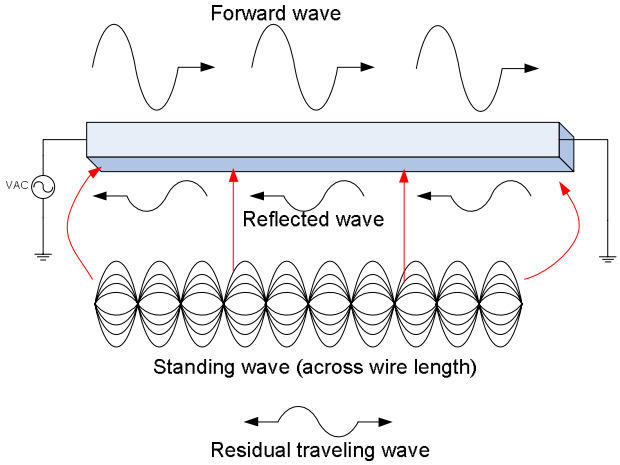

Figure 1. Standing wave and the reflection.

A theoretical *standing wave* (Figure 1) has the property of having position-dependant voltage amplitudes. A standing wave can be easily formed by the juxtaposition of two waves traveling in the opposite direction, such that their amplitudes are the same. We could form a perfect standing wave by sending a sinusoidal wave across an ideal wire that is terminated by a short circuit. In a real world situation, the ideal standing wave is not possible [2, 3] because the amplitude mismatches (and phase mismatches) on the incident and the reflected wave. Such mismatches are caused by the energy losses in the wires. One simple way to compensate for this effect is to generate the standing wave on a short (relative to the signal wavelength) wire. A basic example of an oscillator in this mode is the $\lambda/4$ standing wave oscillator. Figure 2 shows a cross coupled inverter pair placed and the crest of the first wave, which happens at $\lambda/4$ (any odd multiple of this condition will also generate a standing wave). Note that the right hand side of the ring is shorted. Reference [1] uses this configuration to create high Q oscillators for RF applications

978-3-9810801-3-1/DATE08 © 2008 EDAA

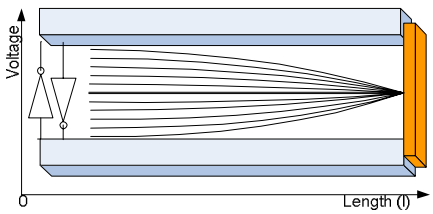

Figure 2. Lambda/4 Standing Wave Oscillator.

The benefit of using a standing wave based oscillator for clocking digital ICs lies in the fact that the voltage across any location along the transmission line will flip polarity at the same time. This allows us to retrieve a square wave clock with constant phase at different points along the transmission line, by using a differential amplifier. Thus the problem due to the variable phase, encountered by the rotary clock, is eliminated. This is of key importance for digital design. The Mobius strip connection presented in this paper allows the recycling the forward and reversing waves traveling along the conductor, saving energy, but at the same time, allows a low-skew square wave clock to be extracted at any point along the transmission line, by using differential amplifiers.

2 Simulation of the Oscillator Architectures

We began by simulating the basic rotary clock [6] and configuring our metal widths and inverter sizes. All oscillator architectures reported in this paper were implemented with conductors on Metal8. The rotary clock is not hard to configure to generate a traveling square pulse. We use an internal element in HSPICE [4] to simulate the transmission line named *U-element*. Our chosen device technology was a 90nm process using BSim3v model cards. We used 24 cross coupled inverter pairs along the rotary ring, all of them equally sized and equidistant from their preceding and succeeding neighbors. We were able to verify that in fact the U-element of HSPICE, in conjunction with the Mobius flip and the cross coupled inverters were able to replicate the inductances and electromagnetic coupling effects required for the rotary clock operation. In Figure 3, we show the superposition of multiple waveforms coming from different cross coupled outputs along the Rotary ring from 0 to 45 degrees along the rotary clock ring. The overshoot of each clock signal along the rotary clock ring is due to the model inductive effects. The main complication of the rotary clock approach arises when these rings are interlocked to form a clocking structure that attempts to cover a larger area of the IC die [11]. In this situation, the clock phase becomes different across the die, complicating synchronous design due to the different phase of clock signals at different parts of the die.

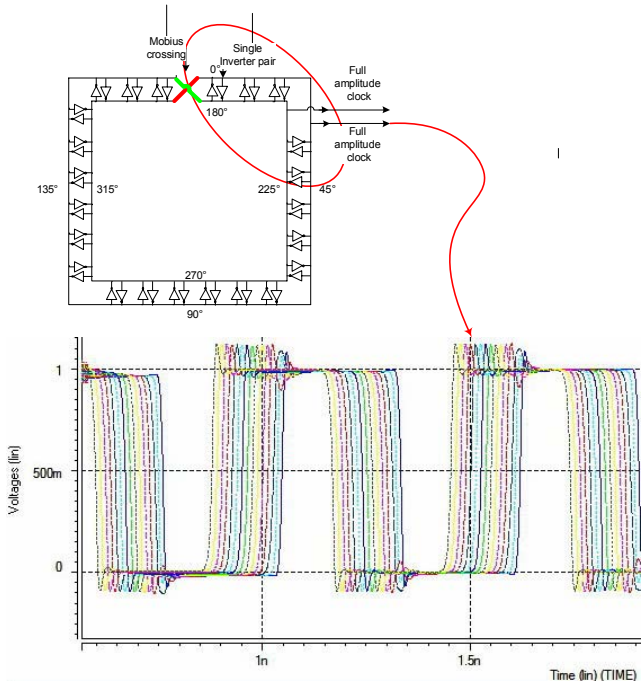

Figure 3: Superposition of waves from our own Rotary clock version in Hspice

We also simulated the standing wave architecture [1] as shown in Figure 4. A single inverter pair was placed at the beginning of the transmission line pair. The transmission line was broken into 24 U-Elements (or transmission line sections) for HSPICE simulation. These segments are labeled 1, 2, 3, etc in Figure 4. Each U-Element was chosen to be 65.3um long, which made the complete ring length 1567.2um. The 90 degree turns are assumed to have a negligible effect on the simulated ring behavior. In between each transmission line segment, our custom designed clock recovery circuit was connected. This clock recovery circuit is explained in the next section.

The output waveforms we obtained along 20 different probing points on the ring. The resulting waveforms are rendered in the plot shown in Figure 5. A qualitative observation on the waveform below shows us clearly that the displayed waveform has a dual nature. First observe the envelope of the wave. This envelope describes the steady standing wave shape. Next observe the modulation that the wave seems to carry (a high frequency "ripple"). This indicates the effect of the traveling wave going upstream along the transmission line, back to the source. This indicates that the amplitude of the traveling wave is quite high compared to the steady wave. This traveling wave will ultimately result in a higher skew in the clock output of the recovery circuit. Notice that the "zero" crossing points of the each waveform (in time scale) occur roughly at the same time. In other words, roughly zero phase is encountered across several probing points on the ring.

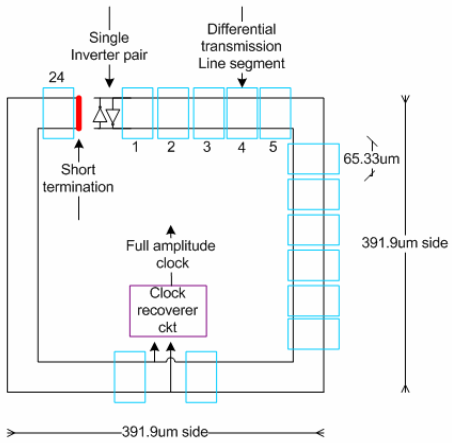

Figure 4: Diagram of out standing wave simulation setup

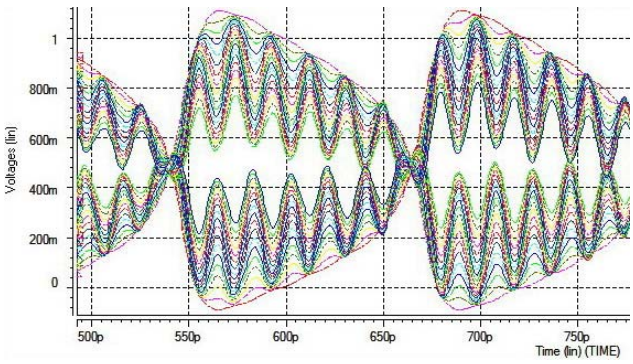

Figure 5: Waveforms at selected ring locations.

Figure 6 shows the recovered clock signals at the 20 probing points. These signals are the output of our recovery circuits. The maximum skew of the recovered clock signals was found to be 6ps, with an average power consumption of 7.57mW (this includes the power due to the cross coupled standing wave generator and the 20 recovery circuits). The frequency of oscillation was found to be 4GHz (with a 250ps period). Note that this frequency is higher than that of the rotary clock descried earlier in this section. We note also that the farther we get from the cross coupled inverters (source) along the ring, the narrower will be the magnitude of the differential signal voltage. If the voltage difference is too low, our differential clock recovery circuit will not be able to correctly recover the clock signal information. This is why we have 20 probing points, even though there are 24 U-elements in the simulation. The last 4 U-elements do not have clock recovery circuits, since the differential voltage magnitude is too small to reliably recover using our clock recovery circuit.

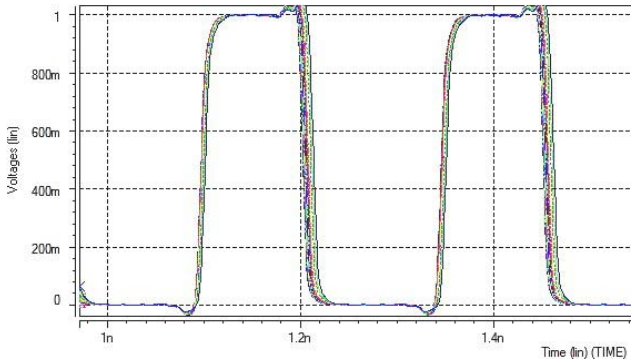

Figure 6: Recovered clock from standing wave ring

For the short-circuit terminated transmission line, the last 4 probing points (closest to the short-circuit location) were considered as unrecoverable clock points, which leave us with a ''null'' part of the ring that doesn't carry proper differential clock information for us to recover.

Now we try out our design (Figure 7), which is the contribution of this paper. Our clocking topology is motivated by the goal of combining the energy recycling feature of the rotary clock scheme with the constant phase (across all points in the ring) of the standing wave oscillator. We next describe our experiments which demonstrate that this is possible. We will use the Mobius termination back to the source (cross coupled wiring pair) which will make our ring look like a single cross coupled rotary wave oscillator. The schematic is shown below in Figure 7. The implications of having this Mobius connection at the cross coupled inverters location is that the ring's clock information will be dual phased. The clock recovery circuits at the right side of the ring will keep the same differential polarity as the non Mobius type of design. On the other hand the recovery circuits on the left side of the ring will now need to have their polarity inverted in order to keep the same phase as the clock signals on the right side of the ring. The second implication of this new arrangement is that a larger part of the total transmission line will be within the vicinity of the cross coupled source, leading to higher voltage amplitudes, and therefore resulting in more usable probing points for clock recovery. The third implication of our approach is that the spurious traveling wave due the amplitude mismatch on the short termination reflection and due to wire losses (studied in [2]) is greatly reduced. Equal and opposite phased waves will meet at the middle of this differential loop. A traveling wave originated due to wire losses will find its opposite wave at this middle and cancel the opposite wave (to a large degree). This comment is better explained with the waveform Figure 8.

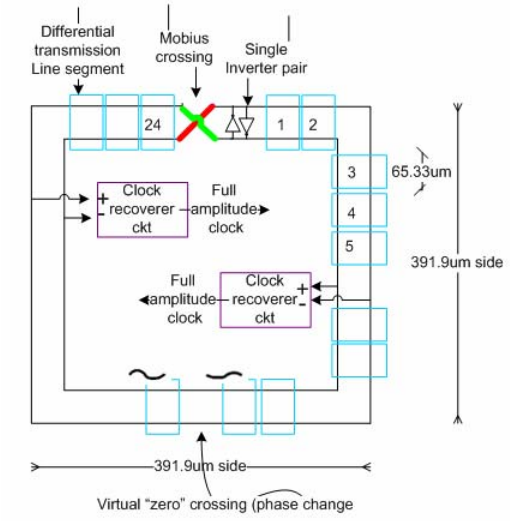

Figure 7: Differential Mobius Transmission Line.

For the simulation of Figure 8, the exact same physical parameters are used as in the non-Mobius case described in Figures 4 and 5. The only change was to make the short-circuited end termination of Figure 4 into a Mobius connection (as shown in Figure 7). In Figure 8, we show the overlap of 20 waveforms coming from different probing points along the transmission line ring, as a function of time. The higher amplitude waves correspond to nodes closer to the source (the cross coupled inverters) while the lower amplitude waves are closer to the virtual short (the point of no oscillation which theoretically has a DC voltage).

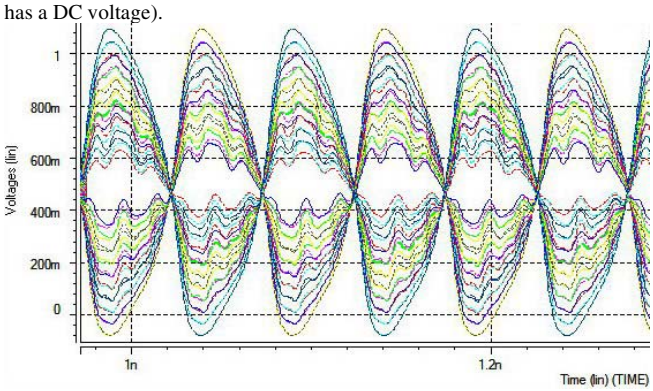

Figure 8: Standing waves from several probing points along the transmission line ring.

The resultant standing wave in Figure 8 shows that the envelope wave (or standing wave) has much higher amplitude than the traveling wave (which is seen as ripples along each pseudo-sinusoidal shape). This allows us to have a bigger differential pair voltage opening resulting in better recovered clock signals at the output of our differential recovery circuit. The recovered clock signals at different points along the ring are overlaid and shown in Figure 9.

The simulated results of our Mobius termination based clock oscillator showed that the maximum global skew was 3.1ps, with an average power consumption of 8.2mW (which includes the power due to all circuits), and a frequency of oscillation of 9.8 GHz (a clock period of 101.9ps). Note that this shows that *our new scheme is able to generate more than double the frequency (145% more frequency) as compared to the short-circuited standing wave oscillator of [1], with the exact same wiring dimensions and with a small increase of power consumption (<8.5%) while improving the skew.*

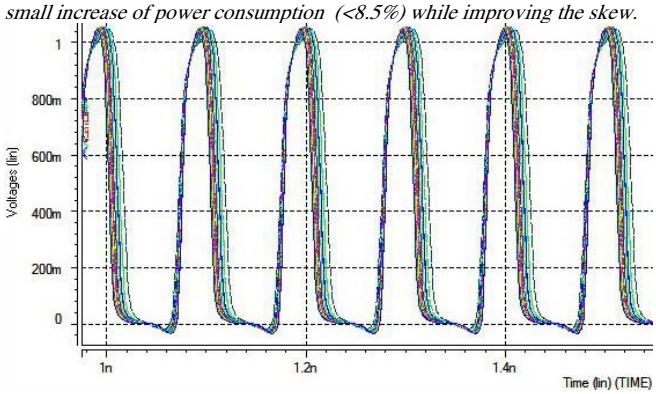

Figure 9: Recovered Clock for Mobius Transmission line scheme

We can therefore claim that our scheme is an improvement over any of the other two oscillator modes simulated in this paper (the rotary clock oscillator and the short-circuit terminated standing wave oscillator), which to the best of out knowledge has not been demonstrated to date.

Please note the small plateau in the recovered clock output is due the fact that our clock recovery circuits (shown in Figure 10), which were designed to operate under a wide range of frequencies (4 to 10GHz), are being used unmodified for all of our simulations of skew at any probing point along the ring. This guarantees that all the configurations are being tested under the same experimental conditions.

2.1 Clock Recovery Circuit.

The clock recovery circuit was designed in a CMOS 90nm Bsim3v process, using the Agilent ADS. The design was then ported to HSPICE, to tune it to operate over a large range of input frequencies, and to tolerate some variations of the DC voltage from the incoming differential signals. Also the design was tuned to tolerate a large range of differential inputs amplitudes. The reason is that we would like to use the same clock recovery circuit to probe the differential signals anywhere along the transmission line pair and get a proper clock recovery. The clock recovery circuits were designed in Agilent ADS using the following design specifications: a VDC on the differential inputs of 0.5V, a VAC of 0.6V to 40mV, and a range of operating frequency from 4 GHz to 10 GHz. Then the model was exported to HSPICE and simulated in HSPICE in conjunction with the Mobius loop based standing wave oscillator. The clock recovery circuit is shown in Figure 10.

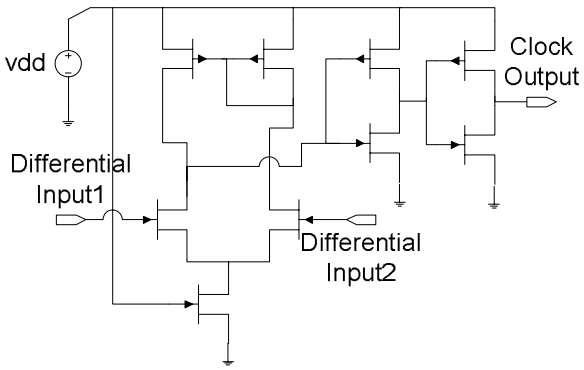

Figure 10: clock recovery circuit schematic

This circuit is composed in three stages, the differential amplifier with bias generator, and two sharp edges generator in cascade (minimum sized). No special voltage supply is required and only one VDC supply is used. Hence this circuit is ideal for a digital IC application.

3 Design Cookbook.

In this section, we explore the effects of designer modifiable parameters on our clock distribution scheme. For this we performed a large batch of Hspice simulations, varying one design parameter at a time and recording the effects of parameter variation on the oscillating frequency, power and skew. Our nominal ring configuration is a setup composed of: PMOS transistors (for the cross-coupled inverter pair) having a width of 300um, and a Wp/Wn ratio of 2.4, The transmission line width was selected to be 20um, the thickness of the transmission line was 2um, and the elevation of the metal tracks from the substrate was 20um. The transmission line segment length was 65.3um. We performed a sweep of only one design variable at the time and analyzed the effect of this change on the operation of the oscillator.

3.1 Variable Number of Clock Recovery Circuits.

The first variable we analyzed is how the loading of the ring due to the clock recovery circuits affects the overall oscillation frequency. For this test we gradually add recovery points along the Mobius connected transmission line. The first recovery circuit is placed on the segment closest to cross coupled pair, and then we added additional recovery circuits which were equidistant from each other. In other word, we added recovery circuits at each of the ports of our transmission line segments. The last (25^{th}) recovery clock probe is placed back toward the source, just before the Mobius wire connection is performed. Figure 11 illustrates the results of this exercise. This figure allows us to make two observations. The first observation is that the loading of the differential transmission line ring that occurs closest to the cross coupled pair affects the oscillating frequency maximally. There was a maximum total clock drift of 11 MHz (when the ring was maximally loaded) compared to the case where the ring was unloaded. Second, we can observe that the power consumed by the clock recovery circuits is minimal compared to the power used to sustain the oscillation. Twenty five recovery circuits used only 0.4mW versus 7.8mW required to sustain the wave.

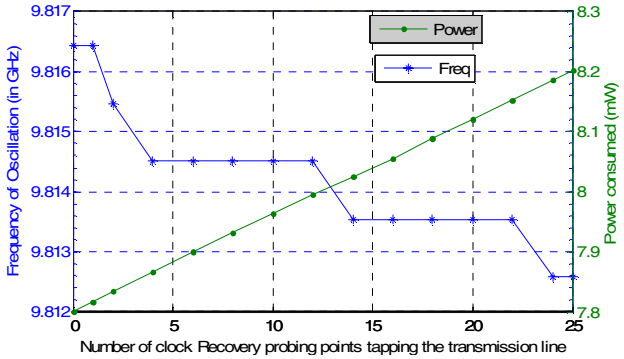

Figure 11: Frequency of oscillation and Power consumption simulations versus a variable amount of clock recovery points.

3.2 Variable Transmission Line Width.

We next conduct experiments to study the effect of a variation in the transmission line width. The first simulation set is shown in Figure 12. We performed a batch of simulations for widths under 20um. 20um is considered our nominal case for the 9.8 GHz oscillator. As we can see in this figure, our power consumption decreases as the transmission line widens. This is because of the reduction in resistive power losses on the clock conductors (which we explained earlier). As the transmission line widens, the frequency of oscillation increases steadily except at 6GHz.

We performed a second batch of experiments where the transmission line width is swept, this time for widths above 20um (results are shown in Figure 13). From Figures 12 and 13, we note that the increase of the frequency of oscillation versus the transmission line width increase continues for wider strips. However, the power consumption as a function of transmission line width does not show a definite trend, for wider transmission lines.

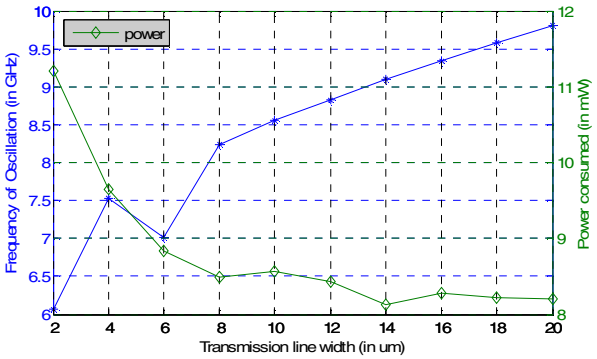

Figure 12: Transmission line width sweep (below 20um)

We also evaluate the effect of the width sweep on the average maximum skew in Figure 14. The average is computed by averaging the maximum skew of the recovered clock from the cross coupled pair to the virtual short on the right side of the transmission line ring, as well as from the cross coupled inverter pair to the virtual short on the left side of the ring.

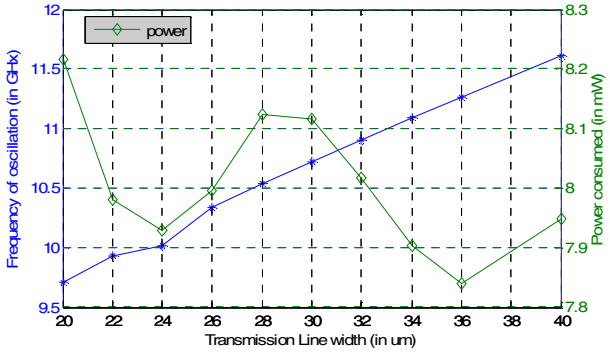

Figure 13: Transmission line width sweep (above 20um)

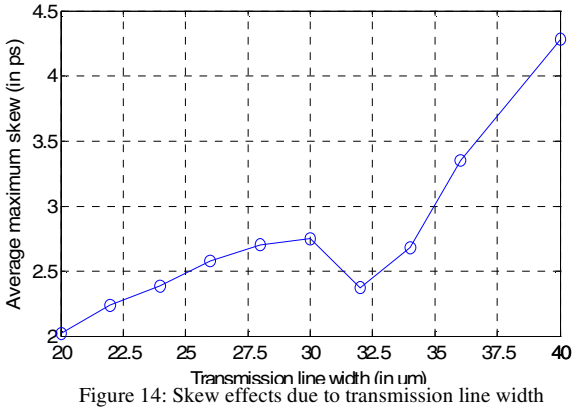

Figure 14: Skew effects due to transmission line width

The global maximum skew increases as the transmission line width increases. Doubling the transmission line width more than doubles the maximum clock skew.

3.3 Variable Ring Length Effects.

We now simulate the effects of extending the length of each individual transmission line segment (the U-element in HSPICE) equally. We first evaluate the effects for the case where the ring is not loaded with the clock recovery circuits. We show this in Figure 15

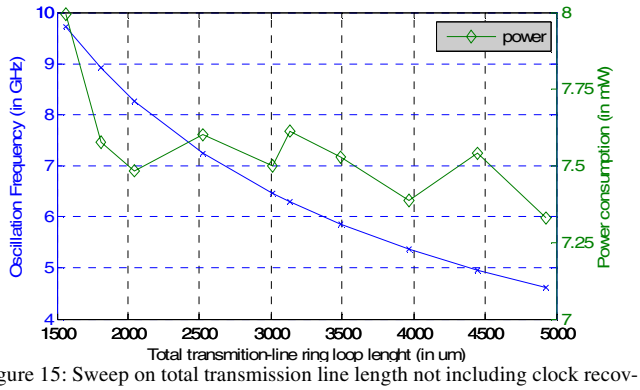

Figure 15: Sweep on total transmission line length not including clock recovery circuits load

This shows us a very clean trend on from the total length to oscillation frequency. The longer the total ring the lower the oscillation frequency. This is expected as the frequency of oscillation described in [6] for a free running standing wave (where no wire losses are present) is modeled by the following equation:

$$Fosc = \frac{1}{2 \cdot \left(\sqrt{L_T \cdot C_T}\right)}$$

In this equation, L_T is the total inductance and C_T is the total capacitances along the transmission line ring. As the total ring length increases both terms increase, yielding a lower frequency of oscillation.

Power consumption follows a harmonic behavior, where for certain oscillation frequencies (or equivalently, total ring length) the energy recycling is less efficient thereby generating power consumption peaks. These peaks however have a small amplitude compared to the total power utilized (note that all of the sample power points above 7mW).

Now we perform the same sweep of the length of the U-elements, but with the clock recovery elements loading the ring. These results are shown in Figure 16. The oscillation frequency gets slightly affected by the recovery circuits (which push all the frequencies slightly lower). Power consumption goes up, and produces the same spikes as the unloaded ring, for the same length values.

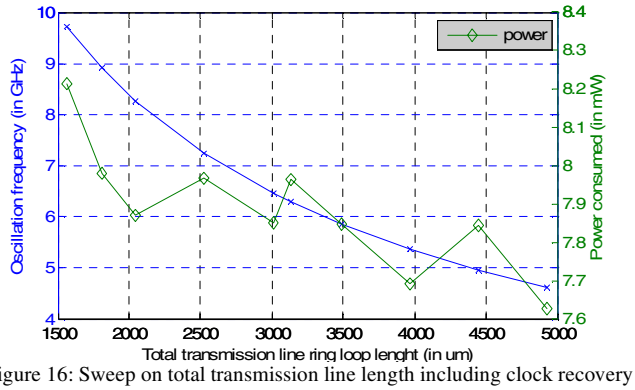

Figure 16: Sweep on total transmission line length including clock recovery circuit's load.

In Fig 17 the skew is obtained for this loaded configuration. Skews were measured on the recovered clock rising edge. The overall trend that we observe is that the skew grows as the transmission line length grows.

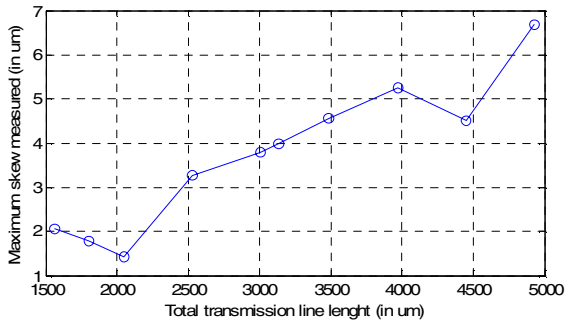

Figure 17: Maximum skew for loaded ring sweep on total length

3.4 Driver Size Wp Variation Effects.

For this experiment we vary the width of the PMOS and NMOS devices of our cross coupled inverters. We keep the ratio of Wp/Wn = 2.4 and use all the same variables as our nominal case. In Figure 18 we show the effects of PMOS and NMOS width variation on power and frequency. As expected there will be a power consumption increase with the upsizing of the devices due to their self capacitances which need to be charged and discharged. This extra loading on the ring also results in a decrease in the oscillation frequency, proportional to the device size increase. Note that our Mobius-connected oscillator can be made substantially variation tolerant by using long channel devices. Also, since there is exactly one cross-coupled inverter pair, the variation tolerance of this approach is expected to be better than a rotary clock based approach, which uses many cross-coupled inverter pairs.

Next we evaluate the effect of the increase in device width on the skew. As we see in Figure 19, the skew keeps decreasing up to a PMOS width of 420um and then starts rising again; therefore the skew dependency on the active devices width is only local.

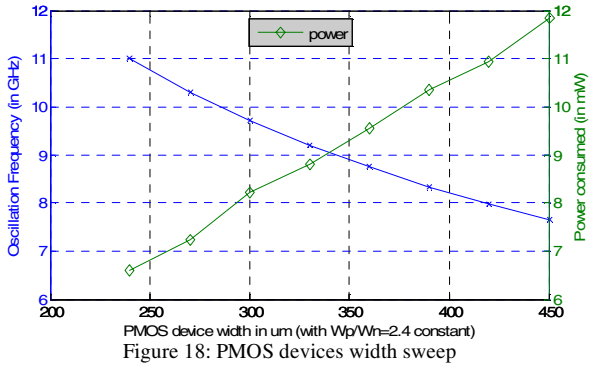

Figure 18: PMOS devices width sweep
Keeping the Wp/Wn ratio constant.

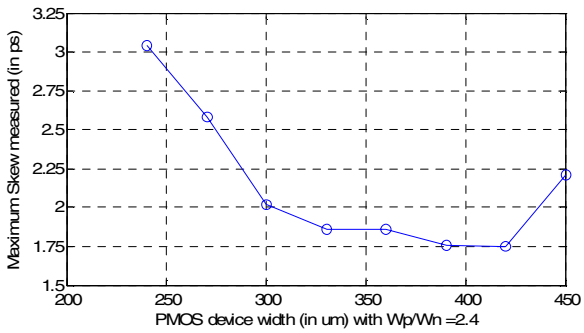

Figure 19: Skew measured to active devices width sweep

3.5 Driver Wp/Wn Ratio Variation Effects.

The last design variable that we sweep is the ratio of Wp/Wn for the devices of the cross coupled inverter pair which sustains the oscillation in the ring. We show the effects of sweeping this ratio in Figure 20. As the ratio grows the overall tendency is to produce a decrease in the oscillation frequency. Also as the ratio grows there is a steady increase in power consumption. Both can be explained by the increase in the self capacitance of the cross coupled inverter pair as the ratio increases.

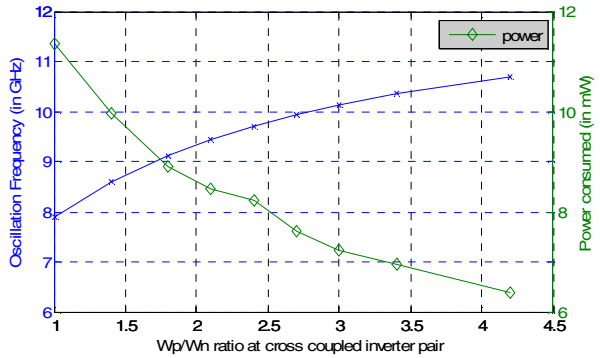

Figure 20: Sweep on Wp/Wn ratio versus power and frequency

We show the effect of sweeping the Wp/Wn ratio on the skew in Figure 21. We can see that for the range of Wp/Wn equal to 2 through 3.5, the skew is fairly constant. As we keep increasing the Wp/Wn ratio, and thus reduce the risetimes to falltimes ratio, this imbalance results in a rapid increase in the skew of the recovered clock. The same applies for the case where the Wp/Wn ratios dropped below 2.0, which generated peaks in the measured skew, however without any systematic trend.

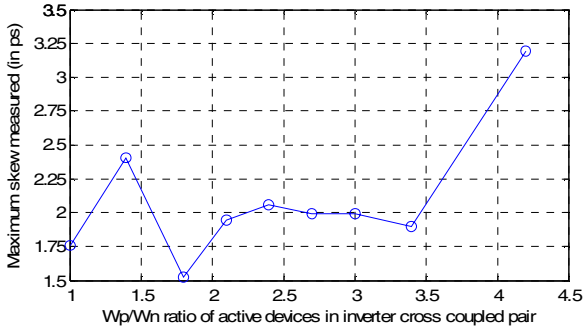

Figure 21: Measured skews for Wp/Wn variable sweep.

3.6 Using the Parameter Variation Plots.

We use all these design parameter variation data to generate a set of long ring configurations. We are especially interested in obtaining design configurations that minimize power, minimize skew, maximize frequency and maximize total ring length. The following table summarizes the best designer configurations that we obtained. The design guidelines plots from this section were used to identify which variable to tune at each step of the iterative process of finding good oscillator configurations.

Total ring length (um)	T-line width (um)	Wp (um)	Beta (wp/wn)	Freq (GHz)	Global Skew max (ps)	Power consumed (mW)
4927.2	40	120	2.4	9.090	0.986	3.640
5407.2	40	100	2.0	9.022	2.870	3.400
5407.2	40	100	2.1	9.075	2.99	3.300
5407.2	40	100	2.4	9.266	3.31	3.120

Table 1: Best configurations for long ring transmission line loops

It is remarkable to mention that the very first configuration of the table, which achieves sub-picosecond skews, uses less power than any of the single design variable sweeps and results in less skew that any of the tests sweeps.

.

4 Conclusions

We have developed a new standing wave oscillator topology with the aim to use it for clock signal propagation in digital ICs. This new scheme could be considered as a hybrid between the rotary clock and the standing wave oscillators. This topology exploits direct cancellation of the undesired traveling waves which result from metal wire losses. This is achieved by forming a Mobius loop, with the cross coupled inverter pair placed exactly at the point of transmission line crossover. This results in the creation of a point on the loop (opposite to the location of the cross-coupled inverter pair) at which both waves from the source meet with an opposite phase. We call this point a virtual short since it is a point at which practically no voltage oscillations occur.

This direct cancellation of the skew-generating traveling wave allows us to use a single cross coupled inverter pair to maintain the oscillation along the ring, while obtaining low skew, low power consumption and a high oscillation frequency. The energy used per gigahertz of oscillation frequency confirms that the Mobius flip is much more efficient than the use short-circuit terminated ends. Also since we do not require cross coupled inverter repeaters (as in the case of the rotary clock scheme), the total self-capacitance of the oscillation generators (the inverters) is kept low, thus allowing even furtherer savings in power due to the presence of fewer active devices.

5 References

[1] William F Andress and Donhee Ham, "Standing Wave Oscillators Utilizing Wave-Adaptive Tapered Transmission Lines" in *IEEE JOURNAL OF SOLID STATE CIRCUITS , March 2005, pp. 638–651*

[2] Frank O'Mahony, C Patrick Yue, Mark A Horowitz and Simon Wong, "Design of a 10GHz Clock Distribution Network Using Coupled Standing Wave Oscillators"

[3] Frank O'Mahony, C Patrick Yue, Mark A Horowitz and Simon Wong,. "A 10 GHz Global Clock Distribution Using Coupled Standing Wave Oscillators" in *IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 38, NO. 11, November 2003, pp. 1813–1820.*

[4] Avant! Corporation, "Star-Hspice Manual", July 1998

[5] Synopsys "HSPICE Signal Integrity User Guide" March, 2007

[6] John Wood, Terence Edwards and Steve Tipa "Rotary traveling wave Oscillator Arrays: A New Clock Technology" *IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 11, November 2001, pp. 1654–1665*

[7] John Wood, Steve Tipa, Paul Franzon, Michael Steer, "Multi gigahertz Low Power Low Skew Rotary Clock Scheme" in *2001 IEEE International Solid State Conference.*

[8] John Wood, Tim Edwards and Conrad Ziesler "A 3.5 GHz Rotary Traveling Wave Oscillator Clocked Dynamic Logic Family in 0.25um" in *2006 IEEE International Solid State Conference.*

[9] G LE Grand de Mercey "A 18 GHz Rotary Travelling Wave VCO in CMOS with I/W Outputs" *IEEE 2006* pp. 489–492.

[10] Haris Basit, John Wood and Ken Pedrotti "Practical Multi-Gigahertz Clocks for ASIC and COT Designs" in *DesignCon 2004.*

[11] Ganesh Venkataraman, Jiang Hu, Frank Liu and Cliff Sze "Integrated Placement and Skew Optimization for Rotary Clocking" in *IEEE'06*