A Radiation Tolerant Phase Locked Loop Design for Digital Electronics

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Abstract— **With decreasing feature sizes, lowered supply voltages and increasing operating frequencies, the radiation tolerance of digital circuits is becoming an increasingly important problem. Many radiation hardening techniques have been presented in the literature for combinational as well as sequential logic. However, the radiation tolerance of clock generation circuitry has received scant attention to date. Recently, it has been shown that in the deep submicron regime, the clock network contributes significantly to the chip level Soft Error Rate (SER). The on-chip Phase Locked Loop (PLL) is particularly vulnerable to radiation strikes. In this paper, we present a radiation hardened PLL design. Each of the components of this design – the voltage controlled oscillator (VCO), the phase frequency detector (PFD) and the loop filter are designed in a radiation tolerant manner. Whenever possible, the circuit elements used in our PLL exploit the fact that if a gate is implemented using only PMOS (NMOS) transistors then a radiation particle strike can result only in a logic 0 to 1 (1 to 0) flip. By separating the PMOS and NMOS devices, and splitting the gate output into two signals, extreme high levels of radiation tolerance are obtained. Our PLL is tested for radiation immunity for critical charge values up to 250fC. Our results demonstrate that over a large number of radiation strikes on a number of sensitive nodes in our design, the worst case jitter is just 18%. In the worst case, our PLL returns to the locked state in 16 cycles of the VCO clock, after a radiation strike.**

I. Introduction

With relentless device scaling, lowered supply voltages and higher operating frequencies, the noise margins of VLSI designs are reducing. Thus VLSI circuits are becoming more vulnerable to noise due to crosstalk, power supply variations and single event effects (SEE) or soft errors. SEEs are caused when radiation particles such as protons, neutrons, alpha particles, or heavy ions strike sensitive diffusion regions in VLSI designs. These radiation particle strikes can deposit a charge, resulting in a voltage glitch on the affected node. This is particularly problematic for memories, since it can directly flip the stored state of a memory element, resulting in a Single Event Upset (SEU) [1], [2]. Although SEU induced errors in sequential elements continue to be problematic, it is expected that soft errors in combinational logic will become problematic in future technologies [3], [4], [5]. In a combinational circuit, a voltage glitch due to a radiation particle strike can propagate to the primary output(s) of the circuit. This can result in an incorrect value being latched in the sequential element(s), and hence result in single or multiple bit upsets. Such radiation strikes in combinational circuits are referred to as Single Event Transients (SETs).

The current pulse that results from a particle strike is traditionally described as a double exponential function [6]. The expression for the pulse is

$$i_{seu}(t) = \frac{Q}{(\tau_\alpha - \tau_\beta)}(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}) \quad (1)$$

Here Q is the amount of charge deposited as a result of the ion strike, while τ_α is the collection time constant for the junction and τ_β is the ion track establishment time constant. The time constants τ_α and τ_β depend upon several process related parameters, and typically τ_α is on the order of 200ps and τ_β is on the order of tens of picoseconds [4], [7].

There has been a great deal of work on radiation hardened circuit design approaches, with a focus on combinational and sequential designs [7], [10], [5], [12], [15]. Very little attention has been paid to SER due to radiation particle strikes on clock nodes despite their significant contribution to the chip level SER. Clock node upsets account for nearly 20% of the overall sequential SER [16]. The global clock distribution network is relatively immune to upsets [16] since it typically contains large buffers and large node capacitances, and has a large RC time constant, thereby acting like a low pass filter. The authors in [16] also report that the contribution to the SER of the global clock grid is negligible (0.1%) compared to that of the regional regenerator circuits and the clock PLL. Strikes in these sections of the clock generation circuitry can result in *radiation-induced clock jitter* and voltage glitches (also referred to as *radiation-induced race*) in the clock nodes. These effects can cause incorrect data to be latched by the sequential elements in the design, potentially resulting in catastrophic failures. The clock distribution network in a chip consists of a global clock generation and distribution network followed by regional clock regeneration buffers. The globally distributed clock signal is relatively immune to radiation strikes due to the large node capacitances [16] of the clock distribution network. However, most modern designs require an on-chip Phase Locked Loop (PLL) to synchronize an external reference clock with the clock signal on-chip. The PLL contains extremely sensitive analog circuitry, and therefore a radiation strike in this circuit can cause catastrophic failure in the design.

In this paper, we present a radiation hardened PLL design. Our design consists of a radiation hardened phase frequency detector (PFD), charge pump (CP) and low pass filter (LPF), voltage controlled oscillator (VCO) and clock divider. Our VCO design consists of two current starved ring oscillator structures, with cross-coupled signals which help to ensure that the effect of a radiation strike on one ring is compensated by the other ring. All the above components of the PLL utilize extremely radiation tolerant split-output gates whenever possible. These gates exploit the fact that if a node is driven using only PMOS (NMOS) transistors then a radiation particle strike can result only in logic 0 to 1 (1 to 0) flip [13], [14].

The main contributions of this paper are:

- We present a highly radiation hardened PLL design, with extremely low radiation induced jitter performance, and a very short time to lock after a radiation event, in comparison to competing radiation hardened PLLs in the literature.
- Our VCO is a novel design utilizing two current starved ring oscillators, whose virtual ground node is controlled separately. The internal signals of any rings are connected to the other ring as well, resulting in a situation where one ring negates a radiation strike on the other ring.
- All the PLL blocks utilize extremely radiation hard standard cells, which were recently reported to protect against radiation with deposited charges up to 650fC.

The rest of the paper is organized as follows. Section II briefly discusses some previous work in this area. In Section III we describe our radiation hardened PLL design. In Section IV we present experimental results, followed by conclusions in Section V.

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II. Previous Work

There has been a great deal of work on radiation hardened circuit design approaches. Many papers report on experimental studies in the area of hardened logic circuits [17], [18], [5], [7], while others focus on radiation hardened memory designs [1], [2], [20], [21], [14]. Since memories are particularly susceptible to SEU/SET events, these efforts were crucial to space and military applications. Yet other approaches address the modeling and simulation of radiation events [23], [24], [25]. Circuit hardening approaches can be classified as device level [8], circuit level [7], [10], [5], [15] and system level [19]. The device and circuit level approaches are typically based on fault *avoidance*, while system level approaches typically depend on error *detection and tolerance* mechanisms. Triple modular redundancy (TMR) is a classical example of a system level design approach. Device level approaches require processing changes to improve the radiation immunity of a design [8], whereas circuit level hardening approaches use special circuit design techniques that reduce the vulnerability of a circuit to radiation strikes.

Although much work has been published in the literature with respect to hardening techniques for combinational and sequential circuits, little attention has been devoted to the problem of clock node upsets and their effect on the chip level sequential SER. Recently, the authors of [16] studied the effect of radiation particle strikes on clock nodes. They partitioned the radiation induced transients on the clock into two categories: *radiation-induced clock jitter* and *radiation-induced race*. The latter category of clock transients is characterized by a missing clock pulse, and can cause catastrophic system failure. The first category can be designed around by guard-banding, provided the jitter is not too large. The authors of [16] report that 20% of total sequential SER is due to clock node upsets. The contribution of radiation-induced jitter is less than 2% of the total sequential SER. This means that most of the upsets occur due to radiation-induced race. Another important conclusion of their experiments was that the contribution of the global clock distribution network is 0.1% of the overall SER due to clock node upsets. Hence, we can conclude that radiation particle strikes on the regional clock regenerator and the clock PLL itself are primarily responsible for the SER due to radiation strikes on the clock network. The authors of [26] performed an experimental analysis to calculate the contribution of clock node upset to SER on the "RH1020" chip in high energy radiation environments. They suggest that the clock upset rate has a strong and linear dependence on clock frequency. They suggest ad-hoc methods to reduce clock node upsets, such as reducing clock frequency and using redundancy in the clock network. However, no experimental results or design approaches were presented.

The vulnerability of conventional digital phase locked loops (D-PLLs) to a radiation particle strike was observed through simulations and experiments [27], [28]. The SET response of the PLL is dominated by the SET response of the charge pump module [27], [28]. In [27], the authors present a hardened PLL operating at 700 MHz. The authors study strikes only on the charge pump output, and observe that a 200 fC strike causes their hardened PLL to require 98ns (68 cycles) to recover lock, with at least one clock pulse being displaced by more than 2Π radians. It was reported in [28] that a radiation particle strike on their proposed hardened PLL (operating at 200 MHz) induced transients last approximately 500ns and result in approximately 120 erroneous clock pulse and a loss of lock for 350ns.

In contrast, we have performed multiple experiments where we strike our hardened PLL at a large number of sensitive nodes (including the charge pump output). We strike our nodes with a Q value of 250 fC (higher than that of [27]). Also, we utilize a more radiation sensitive 65nm process in comparison to a 130nm process for [27]. In the worst of all the strikes that we simulated, we find that we require 16 cycles of the VCO clock to return to the locked state. The maximally disturbed clock pulse exhibits a phase displacement of just 1.18 radians (a worst case jitter of 18% of the clock period).

III. Our Approach

In this section we describe our radiation hardened PLL design. We first describe the general operation of a PLL in Section III-A. Next, in Section III-B, we describe the radiation hardened gates and flip-flops that are used in all the blocks of the PLL. We next discuss the different sub-blocks of our PLL, starting with the VCO (Section III-C), phase frequency detector (Section III-D), charge pump and low pass filter (Section III-E) and clock divider (Section III-F). The system level approach we followed to design the closed loop system is outlined in Section III-G.

A. Phase Locked Loop Operation

A PLL is utilized in almost every modern IC. Its purpose is to synchronize or lock an external reference clock to the clock signal that is distributed within the IC. The common realization of a PLL is shown in Figure 1. A generic PLL

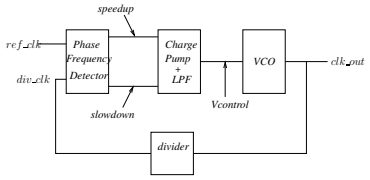


Fig. 1. Block Diagram of a Generic PLL

consists of a phase frequency detector (PFD) which outputs *speedup* (*slowdown*) pulses based on whether the divided clock *div_clk* lags (leads) the reference clock *ref_clk*. The width of these pulses is proportional to the phase difference between the reference and divided clocks. These pulses drive a charge pump (CP) and low pass filter (LPF). Charge is dumped into output node *Vcontrol* of the CP and LPF whenever a *speedup* pulse occurs, thereby increasing the voltage of the *Vcontrol* node. Likewise, charge is removed from the *Vcontrol* node when a *slowdown* pulse occurs, thereby reducing its voltage. The *Vcontrol* node drives a voltage controlled oscillator (VCO), whose frequency increases when *Vcontrol* increases. The output of the VCO is the system clock (*clk_out*) which drives the clock distribution network of the IC. It is divided appropriately to generate *div_clk*. Note that division is required since the internal clock in a modern IC can have a significantly higher frequency (in the low GHz range) than *ref_clk*, which is typically generated by an off-chip crystal oscillator operating in the 10s of MHz range.

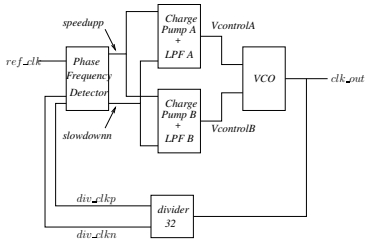


Fig. 2. Block Diagram of our PLL

The block diagram of our radiation hardened PLL is shown in Figure 2. It is conceptually similar to Figure 1, but with significant circuit level differences to achieve radiation hardening. First, it utilizes two independent CP/LPF blocks, which drive two separate VCOs. The VCOs are implemented as current starved ring oscillators (using 3 inverters in the rings). A unique feature of these two VCOs is that their internal nodes are cross-coupled to ensure that if one of them is struck by a radiation particle, the other VCO compensates

for the strike. The *VcontrolA* and *VcontrolB* nodes drive 3 current starving NMOS transistors of their respective ring oscillators, as shown in Figures 5(a) and 5(b). When these signals are low, the ring oscillates at a lower frequency than when these nodes are high. The gates and flip-flops in all the sub-blocks of our VCO are implemented in a split-output manner [29] to achieve radiation hardening. As a consequence, the output of the divider shows two signals in Figure 2.

B. Radiation Hardened Flip-flops and Logic Gates

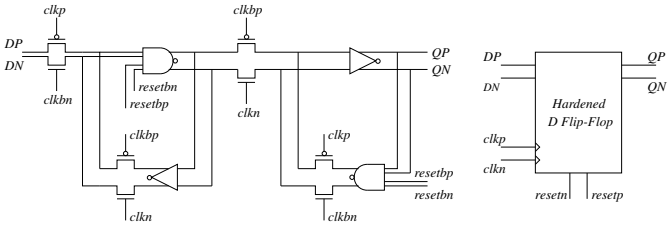


Fig. 4. Radiation Hardened Flip-flop used in our PLL

Logic gates and flip-flops in all the sub-blocks of our PLL are implemented in a radiation hardened manner. A radiation particle strike on the diffusion region of a MOSFET induces a current which always flows from the n-type diffusion to the p-type diffusion through a pn junction [14]. This implies that if a gate is made up of only PMOS (NMOS) transistors then a radiation particle strike cannot flip the node voltage from 1 to 0 (0 to 1). In other words, if a particle strikes the diffusion of a PMOS transistor of an inverter whose output is at logic 1, then this particle strike will not cause the output node voltage to flip. Similarly, a particle strike at the diffusion of a NMOS transistor of the inverter (with an output node at logic 0) will not result in a SET. This key idea suggests that if a logic circuit is made up of only PMOS (NMOS) transistors, then that logic circuit will be tolerant to node flips from 1 to 0 (0 to 1). In [14], [15], this idea was used to design radiation hardened SRAM and flip-flop cells, while in [29], it was used to design highly SEU tolerant standard cell gates. The flip-flop and logic gates used in our design (shown in Figures 4 and 3 respectively, are designed using the approach of [14], [15] and [29]).

A traditional inverter can experience both positive or negative glitches[1] since the PMOS and NMOS transistors are both connected to the output node. We refer the reader to [29], [14], [15] for a detailed description about why the gates in Figure 3 and the flip-flop of 4 are radiation tolerant, and also functionally correct.

Before proceeding further, we briefly state some observations that were made in [29], [14], [15] about the hardened gates [29] and flip-flops [14], [15] that we used in our PLL. Note that the hardened inverter shown in Figure 3 has 2 inputs (inp and inn) and 2 outputs ($out1p$ and $out1n$). Both inputs and both outputs of INV1 are of the same polarity. Note that the output nodes $out1p$ and $out1n$ of INV1 respectively drive only PMOS or NMOS transistors of the gates in their fanout. Note that such a gate has $2n$ inputs (compared to n inputs for any unmodified gate) and 2 outputs (of the same polarity), as indicated in the gate symbols below each of the gates in Figure 3. Note that the transistors M3 and M4 of the inverter in Figure3 are selected to be low threshold voltage transistors (indicated by a thicker line in the figure). This is done so as to increase the voltage swing at nodes $out1p$ and $out1n$, and bring them closer to the rail voltages. Also, note that the reduced voltage swings at $out1p$ and $out1n$ do not increase the leakage currents in a similar inverter in its fanout. This is because, when the node $out1p$ is at $|V_T^{M4}|$ then $out1n$ is at GND due to which the NMOS device of the fanout inverter is completely turned off while its PMOS device is turned on. A similar argument holds for the case when $out1p$ is at VDD and $out1n$ is at VDD-V_T^{M3} Therefore, the leakage currents in a fanout inverter do not increase due to non-rail voltage swing at its inputs.

Note, as stated in [29], [14], [15], that these approaches result in radiation immunity to extremely high energy particle strikes. The width of the voltage glitch induced by a radiation particle strike at $out1p$ should be less than the clock period T for correct operation. Hence the critical charge (Q_{cri}) for the circuit is the maximum amount of charge dumped by a radiation particle such that a voltage glitch of pulse width T is encountered in the circuit. Even for the smallest (most sensitive to radiation) inverter in a circuit operating at 1.5 GHz, (implemented in a 65nm process) the authors of [29] show that a radiation strike with deposited charge as high as 650fC can be tolerated.

Our flip-flop design is shown in Figure 4, along with its circuit symbol. Our flip-flop is conceptually a traditional resettable D flip-flop, with the individual gates implemented in a radiation hardened manner with split outputs, as described above.

C. Radiation Hardened VCO

Our radiation hardened VCO is shown in Figure 5(a). Note that it consists of two ring oscillators (*ringA* and *ringB*). Each ring oscillator consists of three current starved inverters. The control voltage signals (called *VcontrolA* and *VcontrolB* respectively) drive a NMOS device in the inverter, which acts as a current starving mechanism. A low value of *VcontrolA* or *VcontrolB* causes the rings to operate at a lower frequency.

Just like the inverter shown in Figure 3, each of the inverters in the 2 ring oscillators is radiation hardened. However, unlike the inverter shown in Figure 3, each of the inverters in the any of the ring oscillators has 4 inputs. Two of these inputs are driven by an inverter in the same ring, while the other two inputs are driven by an inverter in the other ring. We refer to this inverter as a *ring inverter*, and it is shown in Figure 5(b) (which shows the circuit of the ring inverter of *ringA*). Effectively, the ring inverter of Figure 5(b) consists of two copies of the hardened inverter of Figure 3, whose outputs (*outp_A* and *outn_A* are shorted together. One of the two hardened inverters in Figure 5(b) is connected to a driving inverter from *ringA* via signals *inp_A* and *inn_A*, while the other is connected to the corresponding driving inverter from *ringB* via signals *inp_B* and *inn_B*. The ring inverter of *ringB* is constructed similarly.

Each ring inverter is radiation hardened since it uses two copies of the hardened inverter of Figure 3. Since the outputs of these two hardened inverters are shorted, each ring compensates for radiation strikes in the other ring. For instance, in Figure 5(b), consider the situation where all 4 inputs are high, and just about to fall. Now if there is a strike on the *inp_A* input such that it experiences an upward voltage glitch which causes its falling transition to be delayed, then *ringA* would ordinarily experience a delayed rising transition on *outp_A*, causing the two rings to lose synchronization (in case we did not use ring inverters but rather just used the inverter from Figure 3). However, in the ring inverter there is an alternate inverter driving *outp_A*, and therefore the rising transition on *outp_A* would be minimally delayed since the input signals from the other ring (*inp_B* and *inn_B*) are unaffected by the strike. In this manner, the ring inverters of each ring help compensate for radiation strikes on the other ring. Alternately stated, there is never a time when the output of any inverter in either ring is at a high impedance (something that would be possible if we used the hardened inverters of Figure 3 instead of the ring inverter of Figure 5(b)).

Note that each ring has its own control voltage, and therefore we need two charge pumps and two low pass filters in our design, as we will explain in the sequel. The final output of the ring oscillator consists of 4 signals (two output

[1]A positive glitch is defined as the condition in which the node voltage switches from 0 to 1 and then back to 0. Similarly, a negative glitch is defined as a node voltage transition from 1 to 0 to 1.

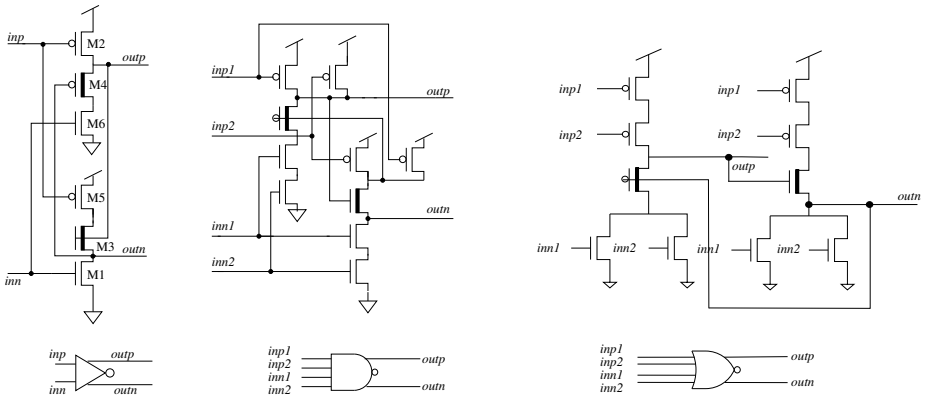
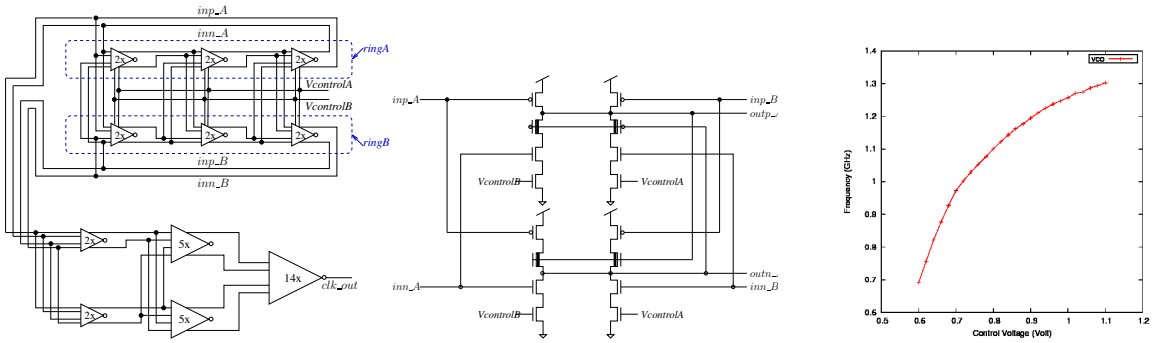


Fig. 3. Radiation Hardened Logic Gates (INV, NAND2 and NOR2) used in our PLL



(a) Radiation Hardened VCO (b) Ring Inverter Design (c) VCO Frequency Vs Control Voltage

Fig. 5.

signals from each ring). These drive a chain of inverters (also implemented in the same manner as ring inverters) shown in the bottom of Figure 5(a). When the drive strength of both inverter chains is sufficiently strong, a single inverter is used to produce the final output *clk_out* of the VCO.

Figure 5(c) shows our VCO's frequency transfer characteristic. Note that the ring inverter devices were sized to achieve a VCO center frequency of 1.0 GHz, with a operating range of 800 MHz to 1200 MHz.

D. Phase Frequency Detector

The PFD of our design is shown in Figure 6. It consists of two hardened D flip-flops, whose clock signals are connected to the reference clock *ref_clk* and the divided VCO output *div_clk*. Note that the *div_clk* signal is a split output signal driven by the frequency divider. The split *D* signals (*DP* and *DN*) of each hardened flip-flop are connected to *VDD*. If the *ref_clk* signal leads the *div_clkp* and *div_clkn* signals, then the signals *speedupp* and *speedupn* rise. When the *div_clkp* and *div_clkn* signals rise, then *slowdownp* and *slowdownn* rise, causing both the hardened flip-flops to reset. Therefore, in this case, the width of the *speedupp* and *speedupn* signals is larger than that of the *slowdownp* and *slowdownn* signals by an amount which is proportional to the amount by which the *speedupp* and *speedupn* lead the *slowdownp* and *slowdownn* signals. A similar discussion applies for the case when the *slowdownp* and *slowdownn* signals lead the *speedupp* and *speedupn* signals.

E. Charge Pump and Low Pass Filter

The charge pump and low pass filter of our design are shown in Figure 7. The charge pump consists of a current mirror, which dumps a constant current into the output node *Vcontrol* when the *speedupp* is high. This causes the voltage of *Vcontrol* to rise. Conversely, when the *slowdownn* signal is high, a constant current is drawn from the *Vcontrol* node, thereby reducing its voltage.

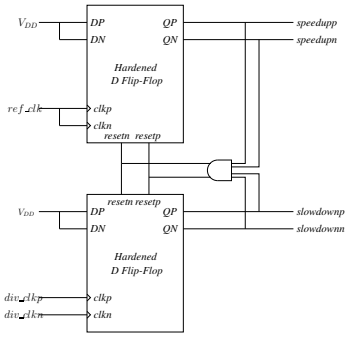


Fig. 6. Phase Frequency Detector

The values of the low pass filter are shown in Figure 7. In Section III-G, we discuss how these values were obtained.

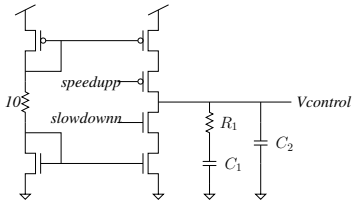


Fig. 7. Charge Pump and Low Pass Filter

F. Frequency Divider

The frequency divider of our radiation hardened PLL is shown in Figure 8. Conceptually it is a simple 5-bit synchronous counter, except that all the gates and flip-flops used in its implementation are based on the radiation hardened split-output designs described in Section III-B. The

outputs of the frequency divider are the signals *div_clkp* and *div_clkn*. Since the center frequency of our PLL is 1.06 GHz, the frequency of the divide clock is about 33 MHz. This is also the frequency of the reference clock *ref_clk* in our simulations. A frequency of about 30MHz is easily realized using crystal oscillators, and is commonly used for the external reference clock frequency in modern VLSI systems.

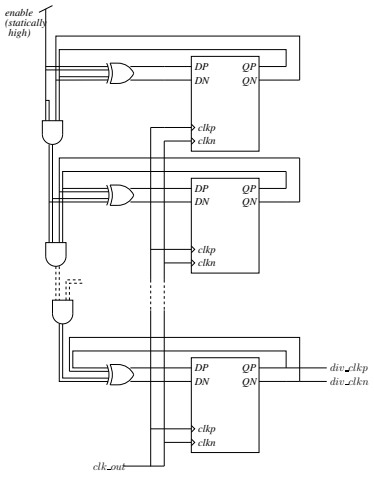


Fig. 8. Frequency Divider

G. System Level Considerations

The loop filter in our PLL consists of resistor R_1 and capacitors C_1 and C_2. Since this is a second order filter, the PLL is therefore a third order system. If we only used a capacitor at the charge pump output, this would result in a open loop transfer function of second order, with both poles located at the origin. This would result in an unstable system, since each pole causes a phase shift of 90°, resulting in an 180° phase shift before the unity gain crossover frequency, thereby causing the system to oscillate. Hence we introduce a zero in the loop gain by adding a resistor R_1 in series with the loop filter capacitance C_1. This stabilizes the system. In this situation, the series combination of R_1 and C_1 could result in a significant ripple in the voltage of *VControl*. Hence an additional capacitance C_2 was added for ripple suppression. We chose the value of charge pump current to be 150 μA. Using the design equations in [32] , we obtained the values of R_1, C_1 and C_2 as 994 Ω, 721 pF and 56 pF respectively . The stability of the system was verified in MATLAB, using the above values.

IV. Experimental Results

To evaluate the performance of our hardened PLL, we conducted several circuit level simulations. We ensured that locking capability of our PLL, and also conducted multiple simulations of radiation strikes on several sensitive nodes of the PLL. All our simulations were conducted in HSPICE [30], using 65nm PTM [31] model cards, with VDD = 1.1V. The reference clock frequency was 33.3 MHz. Since the output clock is divided by 32 in our PLL, the nominal operating frequency was 1.07 GHz. Our VCO was tuned to operate in a range of 800 MHz through 1200 MHz, with a center frequency of 1000 MHz.

As discussed earlier, the individual components of our radiation hardened PLL were first separately tested for radiation hardness. For all our radiation hardening tests, we utilized a double exponential current pulse of Equation 1 to model the radiation strike. For all our radiation strikes, we utilized $\tau_\alpha = 150ps$ and $\tau_\beta = 38ps$, which are reasonable numbers for a 65nm process [7]. Also, we utilized Q = 250fC.

Our experiments consisted of first starting up the PLL and waiting for it to reach a locked condition. At this point, we collected 960 cycles of statistics on the *clk_out* signal. We computed the clock period of the *clk_out* signal for each of these cycles. Let T_{max} be the maximum period, and T_{min} be the minimum period of *clk_out* over these 960 cycles. From this information, we computed the worst case jitter of the PLL under locked conditions as follows, where T = 938ps is the nominal period of the PLL.

$$jitter = \frac{T_{max} - T_{min}}{T} \quad (2)$$

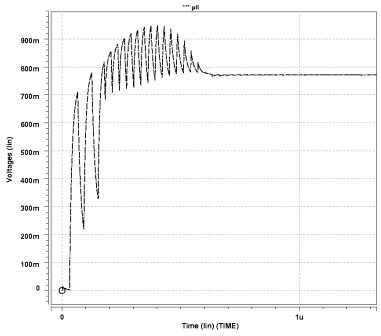


Fig. 9. Waveform of *VcontrolA* during Lock Phase

Figure 9 illustrates the waveform of the *VcontrolA* node as locking is accomplished by our PLL. We found the power of our PLL under locked conditions to be 0.75 mW.

Next we performed a series of strikes on the nodes of our PLL. We struck multiple nodes in each sub-block of the PLL, taking special care to strike nodes that interface different sub-blocks. After each strike, we collected 960 cycles of statistics of the jitter, computed as in Equation 2 above. Table I summarizes these results.

Table I is organized as follows. Column 1 reports the sub-circuit of the PLL that was struck. "NONE" refers to a nominal simulation without any radiation strikes. For each of the sub-circuits listed in this column, we conducted multiple strikes (one per row). Column 2 of Table I reports T_{max}, while Column 3 reports T_{min}. The percentage jitter (computed as shown in Equation 2 above) is listed in Column 4. From Table I, we note that under a locked condition, with no radiation strikes, our PLL has a percentage jitter of 0.85%. Strikes in the various various sub-blocks result in varying amounts of percentage jitter. Each of the sub-blocks has nodes for which the percentage jitter under a radiation strike is about 10%. The worst case is when an internal node in the ring inverter is struck. This results in a percentage jitter of about 18.7%. This is a significant improvement over past radiation hardened PLL approaches. The main reason for the robustness of our design is that each component (down to gates and flip-flops) are designed in a manner that is extremely radiation tolerant. In past approaches [27], [28], the focus was on the hardening of the charge pump alone. Our approach has a higher area than a traditional unhardened PLL. However, the area of a PLL is usually a very portion of the area of an IC, so the increase in area does not prove to be problematic.

In [27], the authors present a hardened PLL operating at 700 MHz. The authors study strikes only on the charge pump output since the goal of the paper is to harden the charge pump. No other nodes are struck, and the radiation resilience of the PLL is therefore not conclusively known. The authors observe that a 200 fC strike causes their hardened PLL to require 98ns (68 cycles) to recover lock, with at least one clock pulse being displaced by more than 2Π radians. It was reported in [28] that a radiation particle strike on their proposed hardened PLL (operating at 200 MHz) induced transients last approximately 500ns and result in

Strike Subckt	T_{max} (ps)	T_{min} (ps)	% Jitter
NONE	933.06	941.22	0.85
Divider	933.09	940.35	0.76
	927.71	1022.8	9.91
	933.09	940.59	0.78
	933.06	940.39	0.76
Chg Pump	933.13	940.82	0.80
	933.08	940.41	0.76
	933.16	940.42	0.76
	933.16	940.61	0.78
	886.43	992.16	11.01
	912.24	986.39	7.72
	887.28	991.50	10.86
	911.89	985.58	7.68
Phase Det	933.11	940.41	0.76
	933.06	940.32	0.76
	933.05	940.68	0.79
	893.41	1042.3	15.51
	933.27	940.36	0.74
	888.59	995.68	11.16
	933.08	940.41	0.76
	933.12	939.99	0.72
VCO	927.58	1107.3	18.72
	933.06	940.59	0.78
	926.97	1105.2	18.57
	929.65	940.52	1.13
	932.76	970.66	3.95
	928.15	1055.6	13.28
	932.78	971.60	4.04
	929.19	1056.2	13.23
VCO drivers	931.21	1028.0	10.08
	931.87	1025.8	9.78
	927.49	1083.5	16.25
	928.03	1084.5	16.30
	933.12	940.40	0.76
	933.14	940.69	0.79
	931.06	940.81	1.02
	932.27	949.66	1.81
	932.12	940.81	0.91
	933.06	948.34	1.59
	933.05	940.32	0.76
	933.12	940.67	0.79
	933.23	940.70	0.78
	933.05	940.88	0.82
WORST			18.72

TABLE I

JITTER STATISTICS FOR OUR PLL

approximately 120 erroneous clock pulse and a loss of lock for 350ns.

In contrast, we have performed multiple experiments where we strike our hardened PLL at a large number of sensitive nodes (including the charge pump output). Our simulations are performed in a more radiation susceptible 65nm process (compared to a 130nm process for [27]). We strike our nodes with a Q value of 250 fC (as compared to 200 fC in [27]). In the worst of all these strikes, we find that we return to the locked state after 16 cycles of the VCO clock. The single disturbed clock pulse exhibits a worst case phase displacement of just 1.18 radians (a worst case jitter of 18% of the clock period).

V. CONCLUSIONS

The radiation tolerance of digital circuits is becoming an increasingly important problem in deep sub-micron technologies. Most of the existing approaches focus on combinational or sequential logic. However, little attention has been paid to the clock generation circuitry. It has been shown that in the deep submicron regime, the clock network contributes significantly to the chip level Soft Error Rate (SER). The on-chip Phase Locked Loop (PLL) is particularly vulnerable to radiation strikes. In this paper, we present a radiation hardened PLL design. Each of the components of this design – the voltage controlled oscillator (VCO), the phase frequency detector (PFD) and the loop filter are designed in a radiation tolerant manner. Whenever possible, the circuit elements used in our PLL exploit the fact that if a gate is implemented using only PMOS (NMOS) transistors then a radiation particle strike can result only in a logic 0 to 1 (1 to 0) flip. By separating the PMOS and NMOS devices, and splitting the gate output into two signals, extreme high levels of radiation tolerance are obtained. Our PLL is tested for radiation immunity for critical charge values up to 250fC, and over a large number of radiation strikes, demonstrates a remarkable ability to recover rapidly from the radiation event.

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