An efficient Pulse Flip-flop based Launch-on-Shift Scan Cell

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***Abstract*— At-speed testing is essential for VLSI ICs implemented in nanometer technologies, operating at high clock speeds. Traditional scan based methodologies can be used for at-speed testing using a transition delay fault model. There are two common techniques to launch the transition - launch-on-shift (LOS) and launch-on-capture (LOC). LOS gives better fault coverage than LOC, but the main drawback of LOS is its requirement of a global at-speed scan enable (SE) signal that needs to be distributed across the IC. In this paper, we propose a pulsed flip-flop based LOS scan cell (PUFLOS cell) and a fast local scan enable generation circuit. Our pulsed flip-flop based scan cell has 23.2% lower power dissipation and 27.3% better timing than a conventional muxed D-flip-flop based LOS scan cell. The layout area of our PUFLOS cell is 21% smaller than conventional LOS scan cell. Monte Carlo simulations demonstrate that our design is more robust to process variations than the conventional scan cell.**

I. Introduction

Constant advances in VLSI design and the increased number of battery powered applications have set us a goal of higher performance with lower power consumption [1]. Flip-flops and latches are fundamental building blocks of sequential digital circuits. The timing of a design significantly depends on the speed of these flip-flops, particularly in heavily pipelined designs. Flip-flops also have a major contribution in the total power consumption of the design [2]. Traditionally, flip-flops are made up of a master-slave latch, with data being latched at the master and delivered to the slave at the sampling edge of the clock. Such an implementation has a positive setup time and the sum of clock to Q delay (T_{cq}) and setup time (T_{su}) is high. This sum is the figure of merit for a flip-flop, since these two delays, added with the combinational logic delay, determine the operating frequency of a design. The desire to reduce this figure of merit ($T_{cq}+T_{su}$) motivates to develop a pulse based flip-flop. A pulsed flip-flop consists of a pulse generator circuit and a latch as shown in Figure 1.

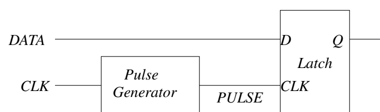

Fig. 1. Block diagram of a pulsed flip-flop

The latch becomes transparent for the short time duration in which the *PULSE* signal is high. The pulse is derived from the input clock edge and hence is generated *after* the clock edge. This allows the data to arrive later than the clock edge, hence making T_{su} negative. This fact helps reduce the $T_{su}+T_{cq}$. The pulse generator circuit can be shared across several flip-flops, amortizing its area and power cost.

Modern VLSI circuits routinely contain hundreds of millions of transistors operating in the gigahertz range. Deep sub-micron technologies exhibit significant inter- and intra-die process variations. Hence, in order to ensure correct logical and temporal functionality, semiconductor manufacturers need to carry out both functional and timing checks on the fabricated chip. It is not enough to just perform stuck-at fault tests for a design because of the growing number of timing related defects in a chip [3]. Therefore, at-speed tests are necessary for higher delay fault coverage [4]. At-speed testing is used to identify the *delay faults* in the circuit.

At-speed testing requires two test vectors, V_1 and V_2. V_1 is used to initialize the inputs of combinational logic, before applying test vector V_2 at-speed. After initialization, V_2 is launched into the combinational logic, the corresponding $V_1 \rightarrow V_2$ transition driven to the circuit under test (CUT). The propagated response of the CUT is then captured into the scan chain during a capture cycle, which is clocked at the operating speed of the design.

Depending on how the transition is launched and captured, there are three methods to generate transition fault patterns. In the first method, referred as launch-on-shift (LOS), the second delay test vector V_2 is one-bit shifted version of V_1. The timing waveforms for LOS are shown in Figure 2. In this figure, scan-in and scan-out cycles are clocked at a lower clock speed (as shown) while the launch and capture cycles are clocked at speed. The *SE* signal must remain high until after the first (launch) fast clock edge. After the first fast clock edge, vector V_2 is present at the output of flip-flops. *SE* must be switched low (in order to transition to functional mode) so that the CUT's response to V_2 can be captured back into the scan chain in the second (capture) fast clock edge. The *SE* signal must switch within a fast clock period making it difficult to distribute this signal across the IC. The *SE* signal is a global signal shared among many scan cells. Hence it is typically hard to meet this tight timing constraint, making the *SE* signal for LOS a timing-critical signal. Our PUFLOS cell addresses this issue. Another drawback of LOS is a potential yield loss since the LOS test is not functional.

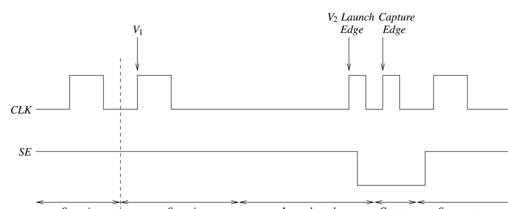

Fig. 2. Timing Diagram for LOS

Figure 3 shows the waveforms of the second approach, referred to as launch-on-capture (LOC). In this method, *SE* must be held high for the duration when the first vector V_1 is scanned into the scan chain. This is done by using a slow clock as shown in Figure 3. *SE* is then made low and enough time is allowed for the transitions to get stabilized throughout the combinational logic. At this point, the second vector V_2, which is the CUT's response to vector V_1, is available at the D input of the scan flip-flops. After this, two fast clock pulses are applied to launch the vector V_2 and to capture the CUT's response corresponding to the $V_1 \rightarrow V_2$ input change. This can be described in two steps. In the first fast clock edge (*launch edge*), the vector V_2 is captured into the flip-flops. This new input vector at the output of the scan cell is propagated through CUT. Now, the second fast clock edge is used to *capture* the response of the CUT to the $V_1 \rightarrow V_2$ transition into scan chain. The clock period of the launch and capture cycles is the same as that of functional clock, as shown in Figure 3. These captured test results are finally scanned out with the slow scan clock, with *SE* is held high. LOC typically results in a lower fault coverage than LOS.

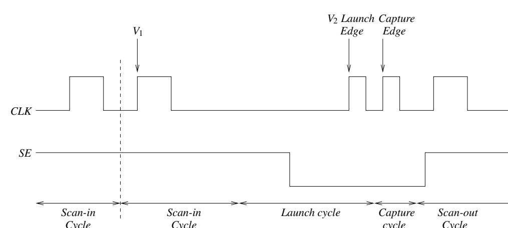

Fig. 3. Timing Diagram for LOC

In the third technique, known as *enhanced scan*, one additional flip-flop is interleaved with each of the functional flip-flops in the design. The vectors V_1 and V_2 can now be *simultaneously* scanned in and loaded into the scan chain, in an interleaved manner. At the end of the *SCAN_IN* phase of the test, bits of the vector V_1 are loaded into the functional flip-flops, while bits of vector V_2 are loaded into

the corresponding additional flip-flop. Since the bits in the additional flip-flops can be chosen arbitrarily, we can achieve any combination of $V_1 \rightarrow V_2$. The drawback of enhanced scan is its area overhead [5] since it uses two flip-flops per scan cell. Also, the length of the scan chain is doubled in this approach compared to LOS and LOC.

The LOS method provides higher controllability and observability than LOC. LOC does not guarantee high fault coverage due to the relationship between V_1 and V_2; since V_2 is the response of the CUT to V_1, LOC allows no flexibility in the choice of V_2. The main concern about LOS is its requirement of an at-speed SE signal.

This paper focuses on the design of an efficient and robust (pulsed flip-flop based) LOS scan cell, which eliminates the need to distribute an at-speed SE signal. The SE signal in our approach is derived locally. The key contributions of this paper are:

- A pulsed flip-flop based LOS scan cell (PUFLOS cell) is presented.
- The proposed PUFLOS cell operates at higher speed and consumes less power as compared to a conventional muxed D-flip-flop based LOS scan cell.
- Our PUFLOS cell has 21% lower area overhead than the conventional LOS cell.
- We present a fast, local scan enable signal generation circuit that can be used with our PUFLOS cell to capture the CUT response at-speed, without requiring an at-speed SE signal to be distributed globally.
- Monte Carlo simulations demonstrate that the proposed PUFLOS cell is more robust to process variations than a conventional scan cell.

II. Previous Work

Several flip-flop designs have been proposed over the years, which aim to minimize power dissipation and to increase the speed of operation. The transmission gate based master-slave flip-flop [6] is one of the simplest implementations. In order to reduce the delay, area and power of the flip-flop, a pulsed flip-flop was introduced. In most pulsed flip-flops, a separate pulse generator and latch are used. In [7], the authors present a dual pulse generator circuit and a NAND keeper latch. However, their design occupies a larger area and also consumes higher power. In [8], the authors proposed an explicit pulsed flip-flop. Their latch circuit is clocked using a single transistor and the pulse generator circuit simply delays the clock and inverts it before ANDing the inverted delayed clock with the original clock for pulse generation. The pulse generator circuit is very simple, but the T_{cq} of the flip-flop is high which leads to a higher value of the figure of merit T_{cq} + T_{su}. The pulsed flip-flop proposed in [9] has a dynamic pulse generator circuit and a static latch. By using a dynamic pulse generator, the authors achieved a better setup time. Also, T_{cq} + T_{su} is low which means that their circuit can operate at higher speed. However, their layout area is large and also their power consumption is high. In [10], authors proposed an improved hybrid latch flip-flop with reduced power consumption. By modifying the dynamic master stage of the hybrid latch flip-flop, they reduce the power consumption significantly. However, due to a higher T_{cq}, their speed of operation is slower. In recent work [11], we proposed a pulsed flip-flop which has a significantly lower T_{cq} + T_{su} and still consumes very low power compared to [9], [10] and a master-slave flip-flop. Our design is robust to process variations with better $\mu + 3 * \sigma$ values of the T_{cq} + T_{su} figure of merit than [9], [10], as evidenced by Monte Carlo simulations. In this paper, we use the pulsed flip-flop of [11] for our proposed LOS scan cell.

In advanced technologies, designs with several hundred thousand flip-flops are common. Therefore the distribution of the *SE* signal for LOS is challenging, much like the distribution of the clock signal. This problem can be solved by increasing the number of *SE* ports, but this is not practical for low-cost testers [12]. A hybrid architecture is proposed in [13], which controls a subset of scan cells by LOS, with the rest are controlled by LOC. The effectiveness of this method depends on the selection criteria of LOS controlled scan cells. Typically this approach would result in lowered at-speed fault coverage due to the use of LOC.

In industrial practice, the *SE* signal is pipelined [14]. Special attention is needed to select the group of scan cells controlled by each *SE* signal. Additional effort is required to partition the flip-flops, and to place and route the design to meet the timing closure of the pipelined *SE* signal.

In [15] a new scan cell, referred to as last transition generator (LTG) is inserted in each of the scan chains, to generate the fast local scan enable signal. The scan enable signal information is encapsulated in the scan test data. The LTG uses two D flip-flops and one OR gate to generate the fast local scan enable signal. More than one LTG will be needed per scan chain if there is a large capacitive load on local scan enable signal. However, our proposed local scan enable generation circuitry can be used across different scan chains, making it easier to route the local scan enable signal in our case. Our proposed scan enable generator circuitry also has a lower area than the LTG.

Some researchers have also focused on other issues related to transition fault testing, such as fault coverage. In [16], an enhanced scan based delay fault testing approach is proposed, which reduces the area overhead compared to conventional enhanced scan design. However, the proposed method has a high area and delay overhead compared to the LOS and LOC approaches. An alternative method is presented in [17], where flip-flop sharing between different state machines is performed to reduce the total number of flip-flops. Here, an extra hold latch is implemented in parallel with the slave latch of the scan flip-flop, by using transmission gates to demultiplex the signal paths. The drawback of this method is that the testing session time gets increased by a large amount. Another technique called First Level Hold [18] uses supply gating at the first level of logic gates to hold the state of a combinational circuit, instead of using an extra latch (as in other enhanced scan methods). This method claims to have a lower area overhead but the amount of logic added is actually dependent on the number of first level gates connected to the flip-flops. It also slows down the logic gates considerably, leading to an additional delay in the combinational logic.

In this paper, we propose a novel pulsed flip-flop based LOS scan cell design. Our design has better area, timing, power and reliability characteristics compared to a conventional muxed D-flip-flop based scan cell design. We also present a circuit to generate the scan enable signal locally, in a manner that works with our pulsed scan cell for LOS.

III. Proposed pulsed flip-flop based based scan cell (PUFLOS)

We will discuss our proposed design in two steps. First we will discuss the pulsed flip-flop that we have used in our PUFLOS cell, and then we will discuss how this pulsed flip-flop has been modified used to design a LOS scan cell with a fast, locally generated scan enable circuit.

A. Pulsed Flip-flop

A pulsed flip-flop consists of a pulse generator circuit and a latch. The pulse generated from this pulse generator circuit determines many of the important characteristics of the pulsed flip-flop such as setup time (T_{su}), hold time (T_h) and clock to Q delay (T_{cq}). The figure of merit of a flip-flop is $T_{su} + T_{cq}$. We first explain why $T_{su} + T_{cq}$ is a useful figure of merit for a flip-flop. Consider the circuit shown in Figure 4. Let D be the maximum delay of the combinational logic between the two flip-flops. T_{su} is the setup time of the flip-flop and T_{cq} is the clock to Q delay. If T is the clock period then $T > T_{su} + T_{cq} + D$ is required for the data to be sampled correctly. Since D is circuit dependent, the figure of merit for a flip-flop is $T_{su} + T_{cq}$. If this quantity is lower, the speed of operation will be higher and vice-versa. Note that we could potentially include the effect of hold time (T_h) as well. The governing equation is $\Delta + T_h < T_{cq} + d$, where Δ is the clock jitter and d is the minimum circuit delay. In this case the flip-flop is most tolerant to jitter if $T_{cq} - T_h$ is maximized. However it is common practice to avoid short paths by introducing dummy delays (and effectively increasing d), thereby eliminating the need to consider T_h. Therefore, we do not include T_h in our figure of merit.

Keeping this in mind, we use a pulse generator circuit shown in Figure 5. The pulse is generated by ANDing the clock with a delayed, inverted clock signal. The pulse width can be easily controlled by appropriately sizing the inverters. For our latch, the required pulse width was generated by slowing down the second inverter in the inverter chain by using long channel devices.

The other component of a pulsed flip-flop is a latch. We have used the latch shown in Figure 6. This latch is transparent when the pulse

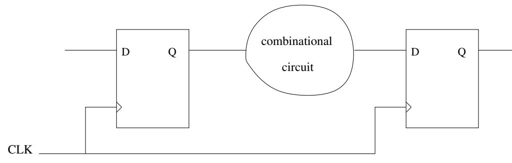

Fig. 4. A sequential circuit

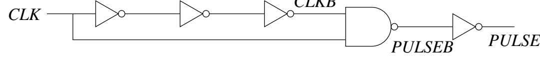

Fig. 5. Pulse generator

is high. The latch circuit is a tristate inverter with a static keeper. The pulse signal is fed to the lower NMOS transistor (N2), while it's compliment is fed to the upper PMOS transistor (P1). The input D is fed to the gates of transistors P2 and N1 as shown in Figure 6. The keeper circuit consists of two back to back inverters. The feedback inverter uses long channel devices.

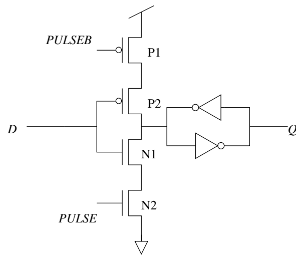

Fig. 6. Latch structure

B. Pulsed Flip-flop based Scan (PUFLOS) Cell

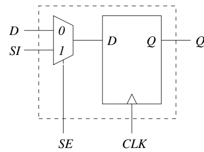

Fig. 7. Conventional muxed-D flip-flop based LOS scan cell

Figure 7 shows a conventional muxed-D flip-flop based scan cell. It consists of a multiplexer and a D flip-flop. The data input *D* and the scan in signal *SI* are the inputs of the multiplexer and scan enable signal *SE* acts as the select signal. The *SE* signal is low during normal operation of the scan flip-flop. In *scan mode* SE is high. Under this condition, the D input of the flip-flop is driven by the scan-in signal *SI*. The *SI* input of scan flip-flop *i* is driven by the *Q* signal of scan flip-flop *i-1*. The *Q* signal of scan flip-flop *i* drives the *SI* signal of scan flip-flop *i+1*. In this way, scan cells are connected to form one or more shift register chains called *scan chains*, which can be accessed through the IO pads. With external access, one can control the internal states of a digital circuit by simply shifting a test vector into the scan chain. After driving the test vector to the combinational logic, one can observe the test response by applying a *CLK* pulse with *SE* = 0, and then shifting out the data from the scan chain.

Figure 8 shows our proposed pulsed LOS scan cell. It consists of a tristate inverter based latch (with output *Q*), a pulse generator and two transmission gates. The pulse generator used for the LOS scan cell is the same circuit discussed in Section III-A (Figure 5), and is not shown in Figure 8. The two transmission gates in Figure 8 are used to implement a 2-input multiplexer. *SI* and *D* are the two inputs of the MUX, and *SCAN* is the select signal of the multiplexer. The timing of the *SCAN* signal is critical for correct LOS operation. *SCAN* is locally generated from the global signal *SE*, which has significantly relaxed timing requirements.

Note that we use a local signal (*SCAN*) instead of global signal *SE*, to control the transmission gates. The *SCAN* signal is generated from *SE* and *PULSE* using the circuit shown in Figure 9. The *SCAN*

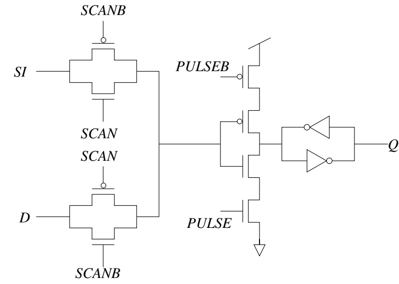

Fig. 8. The proposed pulsed scan cell

signal is high whenever *SE* goes high. However, *SCAN* does not go low with the falling edge of *SE*. The *SCAN* signal goes low at the rising edge of *PULSE*, which occurs after the falling edge of *SE*. This extra circuitry is used to avoid the need to generate and distribute a global, high speed *SE* signal which is otherwise necessary for LOS.

The timing waveforms for *CLK*, *PULSE*, *SE* and *SCAN* signals are shown in Figure 10. In test mode, *SE* is kept high and test bits are scanned in. *PULSE* is generated at every rising edge of *CLK*. The tristate inverter becomes transparent when *PULSE* goes high. After scanning in all the test bits, vector V_1 is applied at the inputs of the combinational logic. Vector V_2 is launched into the combinational logic using the fast clock edge, with a high *SCAN* signal. To capture the data at the next fast clock edge (capture edge), *SCAN* needs to go low before the capture edge, which is ensured by the circuit of Figure 9.

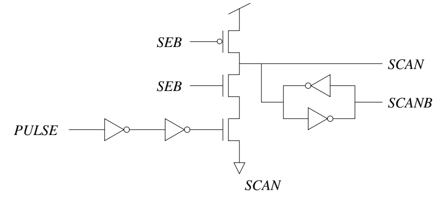

Fig. 9. Proposed local scan enable generation circuitry

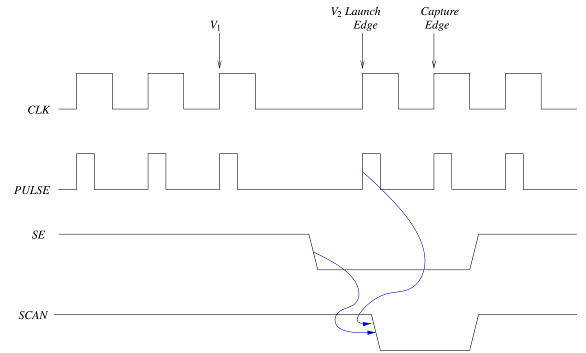

Fig. 10. Timing diagram of proposed enhanced scan flip-flop

IV. Experimental Results

We simulated the proposed PUFLOS cell in HSPICE [19], using a 100nm BSIM [20] model card. The performance of our PUFLOS cell design was compared with the conventional muxed-D flip-flop based scan cell (DFFLOS cell). We compared the performance of our local *SCAN* signal generation circuitry with [15] and [14]. Monte Carlo simulations were performed in order to verify the robustness of our design against process variations. The Monte Carlo simulations were performed for variations in *L* (channel length), V_t (threshold voltage) of transistors and VDD (supply voltage). A total of 500 simulations were run with 3σ variation value as 10% of the nominal value for each parameter.

Table I shows the experimental results for the PUFLOS and the DFFLOS cells. When computing the area and power of our

Scan cell	Nominal Simulations				Monte Carlo Simulations		Layout Area (μm^2)
	T_{cq} (ps)	T_{su} (ps)	$T_{cq}+T_{su}$ (ps)	Power (μW)	$T_{cq}+T_{su}$ (ps)		
					Mean	Sigma	
PUFLOS cell	155.8	-67.2	91.6	12.9	91.8	5.12	28.9
DFFLOS cell	77.8	48.1	126.0	16.8	129.4	6.11	36.6

TABLE I

SIMULATION RESULTS FOR PUFLOS AND DFFLOS

PUFLOS cell, the pulse generator is assumed to be shared between 10 PUFLOS cells. We found that using 10 PUFLOSs per pulse generator minimized the dynamic power per PUFLOS cell while ensuring precise *PULSE* signal timing. Our proposed PUFLOS cell is 27.3% faster than a conventional muxed-D flip-flop based LOS scan cell. The proposed design consumes 23.2% lower power compared to the DFFLOS cell. The mean (σ) of the figure of merit of the PUFLOS cell is 29.0% (19.30%) better than that of the DFFLOS cell. The μ + 3*σ of the figure of merit of the PUFLOS cell is 27.5% better than that of the DFFLOS cell.

We also compared our design with a DFFLOS cell in terms of layout area. Our proposed PUFLOS cell occupies an area of 28.9μm^2 (this area includes $\frac{1}{10}$th of the area of the pulse generation circuit of Figure 5. In contrast, a D flip-flop based LOS scan cell occupies an area of 36.6μm^2. The layouts of conventional scan cell and the proposed PUFLOS cell are shown in Figures 11 and 12 respectively. Figure 12 illustrates the pulse generator (top) and the PUFLOS structure (bottom). Note that the pulse generator is shared between 10 PUFLOSs.

For the performance evaluation of our local *SCAN* signal generation circuitry we have compared the power consumed by our approach per scan cell in the test mode, with [15] and [14]. In all of these three cases we assumed that local scan enable generation circuitry is shared between 10 scan cells. Our scan cell dissipates 14.9μW power, which is 21.3% and 21.5% less power than [15] and [14], which dissipates 18.3μW and 19.0μW respectively.

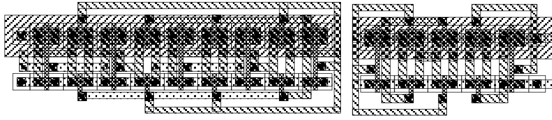

Fig. 11. DFFLOS cell layout

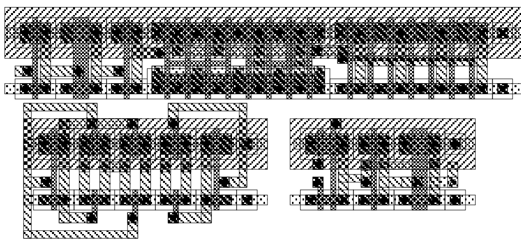

Fig. 12. Pulse generator (top) and PUFLOS cell (bottom) layout

V. CONCLUSIONS

In this paper, we present a pulsed flip-flop based LOS scan cell. Our pulsed scan cell consumes less power, and occupies lower area while achieving higher performance compared to conventional muxed-D flip-flop based scan cell. The robustness of our design was verified by performing Monte Carlo simulations. Our PUFLOS cell has 27.3% lower $T_{cq}+T_{su}$ delay and also consumes 23.2% less power compared to DFFLOS cell. Our design also has 21.0% lower layout area compared to DFFLOS cell.

REFERENCES

[1] A. Chandrakasan, S. Sheng, and R. Brodersen, "Low power CMOS digital design," *IEEE Journal of Solid State Circuits*, vol. 27, pp. 473–484, 1995.

[2] J. Rabaey and M. Pedram, *Low Power Design Methodologies*. Kluwer Academic Publishers, Norwell, MA, 1996.

[3] R. Wilson in *Delay-fault testing mendatory, author claims. EE Design*, Dec. 2002.

[4] J. Savir, "Skewed-load transition test: Part 1, calculus," pp. 705–713, 1992.

[5] B. Dervisoglu and G. Stong, "Design for testability: Using scanpath techniques for path-delay test and measurement," in *Proceedings of the IEEE International Test Conference on Test*, (Washington, DC, USA), pp. 365–374, IEEE Computer Society, 1991.

[6] V. Stojanovic and V. Oklobdizija, "Comparative analysis of master-slave latches and flip-flops for high performance and low power systems," *IEEE jnl of Solid State Circuits*, pp. 636–548, April 1999.

[7] J. Kim and B. Kong, "Dual edge triggered flip-flop with modified nand keeper for high performance VLSI," *J. Current Appl. Phys.*, 2004,.

[8] P. Zhao and M. Bayoumi, "Low power and high speed explicit pulsed flip-flops," *The 45th midwest Symp. on Circuits and Systems, Tulsa, OK, USA,*, Aug 2002,.

[9] M. Phyu, W. Goh, and K. Yeo, "Low-power/high performance explicit-pulsed flip-flop using static latch and dynamic pulse generator," *IEE Proc. Circuits Devices and Syst.*, vol. 153, June 2006.

[10] S. Goel and M. Bayoumi, "Improved Hybrid Latch flip-flop for low-power VLSI systems," tech. rep., VLSI Research Lab, Centre for Advanced Computer Studies, University of Lousiana at Lafayette.

[11] R. Kumar, K. Bollapalli, and S. Khatri, "A robust pulsed flip-flop and its use in enhanced scan design," in *International Conference on Computer Design*, (Lake Tahoe, California, USA), Oct. 2009.

[12] J. Saxena, K. Butler, J. Gatt, R. Raghuraman, S. Kumar, S. Basu, D. Campbell, and J. Berech, "Scan-based transition fault testing " implementation and low cost test challenges," in *ITC '02: Proceedings of the 2002 IEEE International Test Conference*, (Washington, DC, USA), p. 1120, IEEE Computer Society, 2002.

[13] S. Wang, X. Liu, and S. Chakradhar, "Hybrid delay scan: A low hardware overhead scan-based delay test technique for high fault coverage and compact test sets," in *DATE '04: Proceedings of the conference on Design, Automation and Test in Europe*, (Washington, DC, USA), p. 21296, IEEE Computer Society, 2004.

[14] "Synopsys application note," in *Tutorial on Pipelining Scan Enables*, 2004.

[15] N. Ahmed, C. P. Ravikumar, M. Tehranipoor, and J. Plusquellic, "At-speed transition fault testing with low speed scan enable," in *VTS '05: Proceedings of the 23rd IEEE VLSI Test Symposium*, (Washington, DC, USA), pp. 42–47, IEEE Computer Society, 2005.

[16] S. Bhunia, H. Mahmoodi, A. Raychowdhury, and K. Roy, "A novel low-overhead delay testing technique for arbitrary two-pattern test application," in *DATE '05: Proceedings of the conference on Design, Automation and Test in Europe*, (Washington, DC, USA), pp. 1136–1141, IEEE Computer Society, 2005.

[17] J. Hurst and N. Kanopoulos, "Flip-flop sharing in standard scan path to enhance delay fault testing of sequential circuits," in *ATS '95: Proceedings of the 4th Asian Test Symposium*, (Washington, DC, USA), p. 346, IEEE Computer Society, 1995.

[18] S. Bhunia, H. Mahmoodi, A. Raychowdhury, and K. Roy, "A novel low-overhead delay testing technique for arbitrary two-pattern test application," in *Design Automation and Test in Europe (DATE)*, March 2005.

[19] I. Meta-Software, "HSPICE user's manual," Campbell, CA.

[20] "BSIM3 Homepage." http://www-device.eecs.berkeley.edu/~bsim3/intro.html.