A Modified Scan-D Flip-flop Design to Reduce Test Power.

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Abstract— **Power consumption in scan based testing is high due to the toggling of the combinational logic during the scan shift. In this paper, we present a modified Scan Flip-flop architecture with a minimal area overhead which completely eliminates the switching power dissipation and also reduces the leakage power in the combination circuit during the shift phase of a scan based test. This also enables us to increase the shift frequency since power is no longer a limiting factor during scan shift and help in achieving test time reduction.**

Index Scan based test. Scan Flip-flop, scan per vector.

I. INTRODUCTION

Testing of VLSI circuits can lead to generation of excessive heat which can damage the chips under test. In scan based testing methodology, high-performance CMOS circuits consume significant dynamic power during testing because of enhanced switching activity. The power and energy consumption of digital systems may increase significantly during testing. This extra power consumption during test application may reduce circuit reliability. The consumed energy directly corresponds to the switching activity generated in the circuit during test application. This has an impact on battery lifetime during remote self-testing. ***Test-per-scan*** techniques involve applying test patterns from a loaded scan chain to a ***circuit under test*** (CUT) every *m+1* clock cycles, where *m* is the number of flip-flops in the scan chain. Most of the power-dissipation in the CUT will occur during the shifting of bits into the scan chain. The two types of power consumption that are of importance, during test mode of a circuit, are ***peak power*** and ***average power.***

- The *average power* consumption is given by the ratio between the total energy and the test time. This parameter is more important than the instantaneous energy as hot spots and reliability problems may be caused by sustained high power consumption.
- The *peak power* consumption corresponds to the highest switching activity generated in the circuit under test, during one clock cycle. The peak power determines the thermal and electrical limits of components and the system packaging requirements. If the peak power exceeds certain limits, the correct functioning of the entire circuit is no longer guaranteed.

The main motivation for considering power consumption during test application is that power and energy of a digital system can be considerably higher in test mode than in system mode. The reason is that test patterns can cause many combinational nodes switch while a power saving system mode only activates a few modules at the same time. Another reason is that successive functional input vectors applied to a given circuit during system mode have a significant correlation. There is no specific correlation between the consecutive test patterns generated by an ATPG tool (for external testing) or that created by an LFSR (for BIST) for testing such circuits. This can cause considerably larger switching activity in the circuit during test than during its normal operation. Since power dissipation in CMOS circuits is proportional to switching activity, this excessive switching activity during test can cause several problems. In particular, it is shown that this increased power may be responsible for increased cost, reduced reliability, harder performance verification and technology related problems. Reduced power dissipation during test application is thus becoming an equally important figure of merit in today's VLSI circuits design and is expected to become one of the major objectives in the near future. Practiced solutions include:

- Over designing the power supply, package and cooling to tolerate the increased current during testing. Breaks are inserted into the test process for avoiding hot spots.
- Testing with reduced operation frequency.
- Partitioning of the system under test and appropriate test planning

The first solution increases both hardware costs and test application time. The second proposal uses less hardware, but the reduced system frequency increases test application time and may lead to a loss of defect coverage as dynamic faults may be masked. Moreover, this solution reduces the power consumption at the expense of a longer test time, but does not reduce the total energy consumption during test. Test partitioning and test planning allows the detection of dynamic faults, but increases hardware overhead and test time during BIST.

II. BACKGROUND

The two components of power dissipated in a CMOS circuit are:

i) Static dissipation due to leakage current through the channel and the tunneling current through the gate oxide

ii) Dynamic dissipation due to switching transient currents and charging and discharging of load capacitances.

Power consumption can be reduced by applying the test patterns at a slower frequency. Average dynamic power consumed due to charging and discharging of load capacitances is given by $1/2CV^2f * N_G$ where C is the output capacitance, V is the voltage at which the test is run, f is the frequency of operation during the test and N_G is the total number of Gate output transitions[3]. Reducing f obviously reduces the power consumption. This method of power reduction causes an unacceptable increase in test time. As designs get more complex, the test pattern volume grows, resulting in increased test time. Reducing frequency during test only worsens the problem.

With the shrinking of technology, the power due to leakage currents dominates the power due to active switching. The following graph from Cadence shows the trend in leakage current with reduction in gate length.

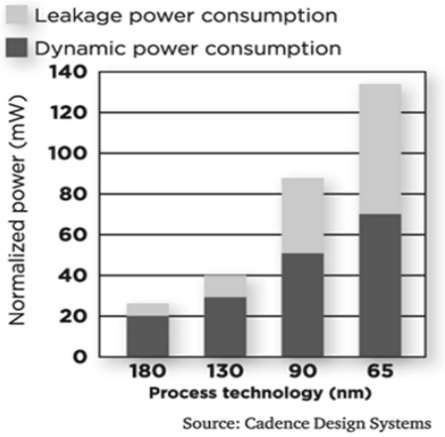

Figure 1: Power Trends in Recent Technologies

This clearly shows that power contribution due to leakage currents is a major factor and needs to be reduced.

III. PREVIOUS WORK

Previous work on low-power test-per-scan IC design can he classified into two broad categories: ***circuit modifications*** and ***test vector alterations*** [4], [5], [6]**.** Circuit modification techniques can be further divided into two categories, CUT and scan D flip-flop (DFF**)** modifications. Circuit partitioning divides the CUT into a number of smaller modules; each can be tested pseudo-exhaustively to reduce the average power consumption. Previous work also describes a toggle suppression technique that reduces circuit activity and average power consumption with the use of a modified D-Flip-flop that supplies constant 0 values to the CUT during the scan operation. One approach uses an additional slave latch in a normal master slave Flip-flop and uses the additional slave latch to maintain a constant value at the Q output which feeds to the combinational cloud during scan shift [1]. The design of such a Flip-flop with additional slave latch is shown in Figure2.

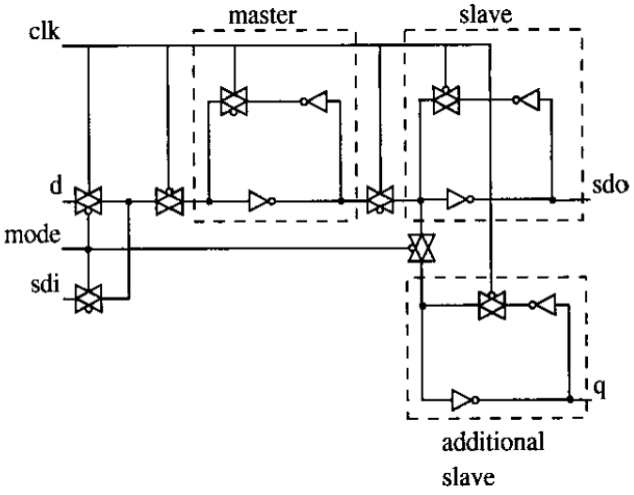

Figure 2: Scan D-Flip-flop with Latch as gating logic

The additional overhead in this scheme is an extra latch. Another approach uses an AND gate instead of a latch to maintain a constant value at the Q output during the scan shift operation [2]. This approach compared to the approach of [1] has a reduced area penalty. The structure of such a D-Flip-flop, gated by an AND gate is shown in Figure-3.

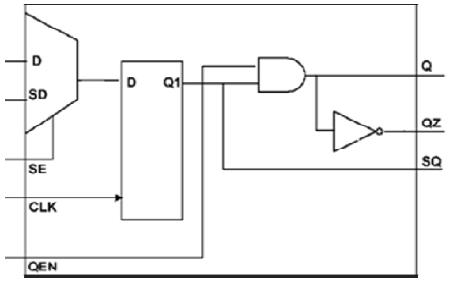

Figure 3: Scan D-Flip-flop with AND gate as gating logic.

IV. PROPOSED TECHNIQUE.

The current proposed technique also gate the Q output during the scan shift operation. This method uses a transmission logic gate followed by a pull-up or pull down transistor to gate the Q output and maintain it to a constant value of 1 or 0. Using this scheme, the combinational logic can be set to a desired low leakage input pattern, thereby minimizing the leakage power.

The two main advantages of this approach over the other previous approach are:

- Reduced area overhead (only 3 transistors)
- The ability to control the leakage of the combinational logic by setting the inputs of the combinational logic to a low leakage state during scan shift.

The structure of the D-Flip flop with pull-up and pull-down are as shown in the Figure-4 and Figure-5:

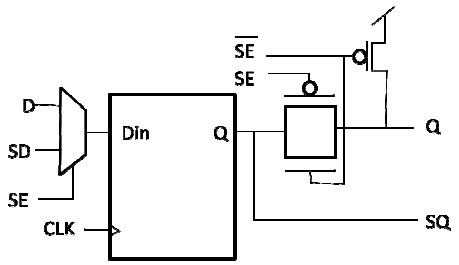

Figure 4: D-Flip-flop with pull up structure

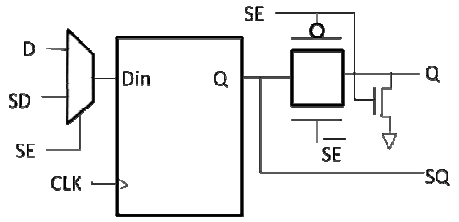

Figure 5: D-Flip-flop with pull down structure

We clearly see that the above structures have a less area compared to a latch or an AND gate approach, Along with the additional benefit of allowing us to park the combinational circuit at its lowest leakage input.

V. Experimental Results

To demonstrate the modified D-Flip-flop's functionality, the circuits of Figure-4 and Figure-5 was created in the 65nm technology and simulated in Spectre to verify its functionality.

In order to demonstrate the reduction in leakage power with input values compared to the input of all 0's (which is the input state of the combinational logic if the technique of [1] or [2] are used), we developed standard cells for the 65 nm technology in Cadence. Their leakage power was calculated using Spectre. The results are shown in Table 1, 2 and 3.

Input	0	1
Cell	INV	INV
65nm	3.912	29.17

Table 1: leakage power for Inverter (in nW)

Input	00	01	10	11
Cell	NAND2	NAND2	NAND2	NAND2
65nm	0.93	10.5	3.96	61.7

Table 2: Leakage power for NAND gate (in nW)

Input	00	01	10	11
Cell	2I-NOR	2I-NOR	2I-NOR	2I-NOR
65nm	7.92	29.62	12.7	2.81

Table 3: Leakage power for NOR gate (in nW)

We compare the leakage power in combinational logic (whose inputs are fed by Flip-Flop's *Q* output) during the scan-shift for our approach and that of approach [1] or [2]. We synthesized and mapped a set of benchmark combinational designs using SIS. The library cells used during mapping were NAND2, NOR2 and INV as described earlier. The leakage power of benchmark circuits with all 0 inputs was computed. This corresponds to the leakage if methods [1] or [2] are implemented. For our method, the leakage over 10,000 random input vectors was calculated. The pattern resulting in the least leakage is driven out to the combinational logic by using one of the modified DFFs (Figures-2 and 5). The results are as shown in Table-4.

Benchmark Circuit	All '0' pattern	Random pattern	% Saving
ALU2	5719	5333.6	6.73894
apex6	12578	12578	0
apex7	3929	3818	2.825146
C17	108	108	0
C432	4008.4	3370	15.92655
C449	10966	10946	0.182382
C880	7733	6445	16.65589
C1355	10966	10946	0.182382
C1908	10608	9554	9.935897
C3540	26785	23057	13.91824
C5315	39816	33397	16.12166
C6288	64561	51808	19.75341
C7552	46740	44684	4.398802
Dalu	15165	13954	7.985493
Decod	243.5	243.5	0
I1	787.1	549.6	30.17406
I2	5094.9	1573.6	69.11421
I3	1053	618.6	41.25356

Table 4: Leakage power in benchmark designs.

VI. Conclusion

We present an approach which apart from eliminating the switching power in the combinational logic during scan shift also minimizes the leakage power. Also this approach has a low area overhead compared to previous schemes.

VII. References

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