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Impedance Matching Techniques for VLSI Packaging

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Impedance Matching Techniques for VLSI Packaging

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Acknowledgement

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Problem Statement

- **Reflections from interconnect will limit VLSI system performance**

- **This is caused by :**

1) Parasitics of the Package Interconnect

2) Faster Risetimes in Off-chip Driver Circuitry

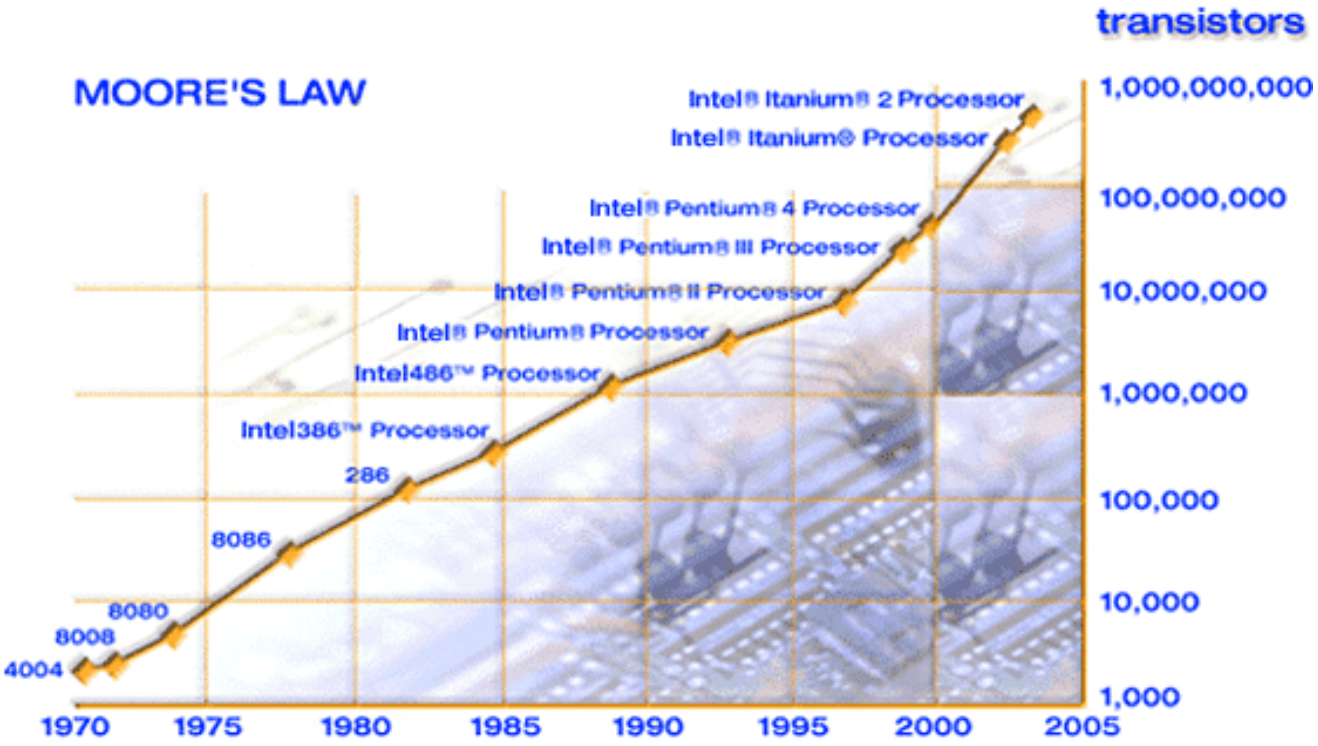
Agenda

1) Package Interconnect Parasitics

2) Proposed Solution

3) Experimental Results

Why is packaging limiting performance?



Transistor Technology is Outpacing Package Technology

Why is packaging limiting performance?

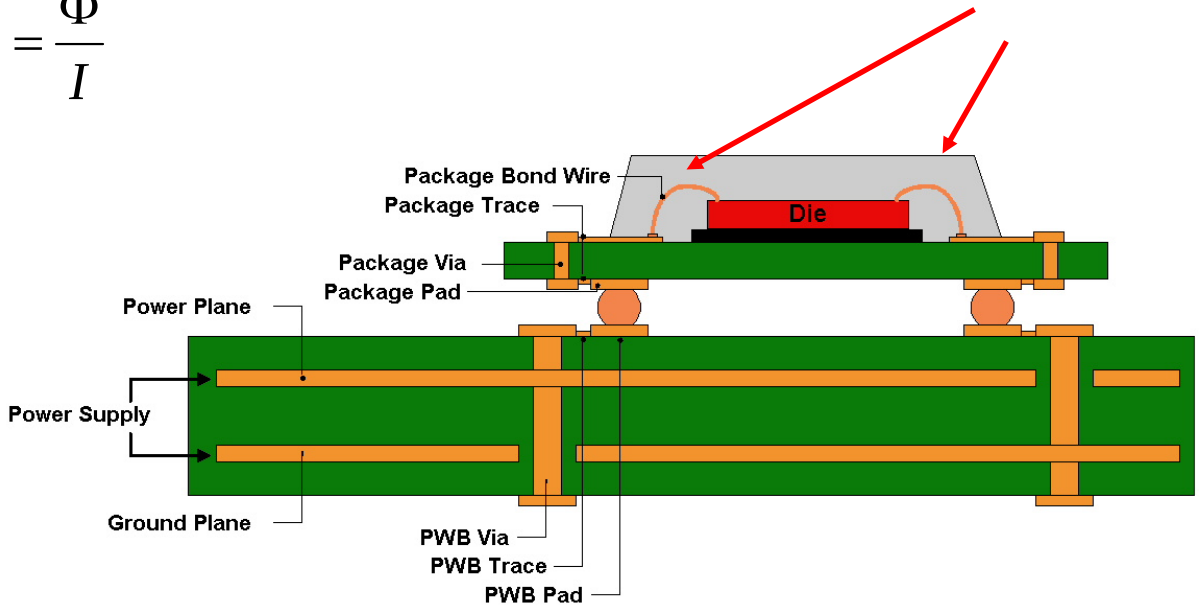
- **Today's Package Interconnect Looks Inductive**

  - Long interconnect paths

  - Large return loops

  - $L = \frac{\Phi}{I}$

Wire Bond Inductance (~2.8nH)

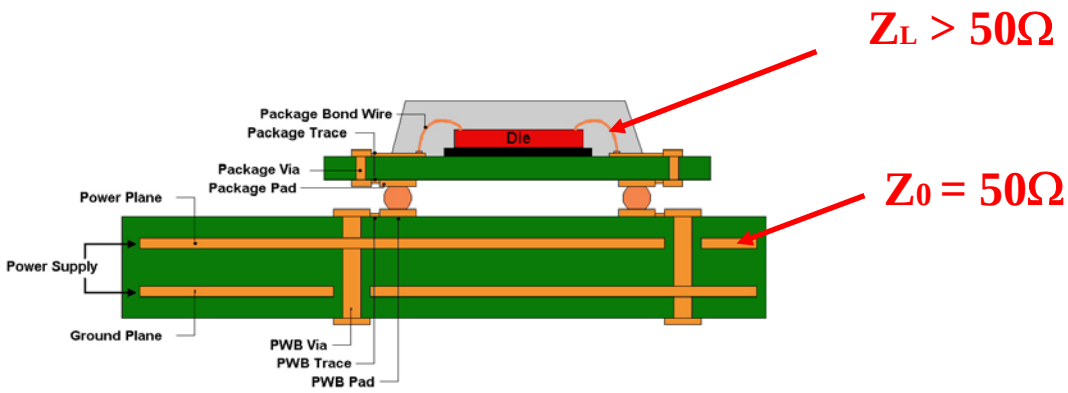


Why is packaging limiting performance?

- **Inductive Interconnect Leads to Reflections**

  - Interconnect is not matched to system

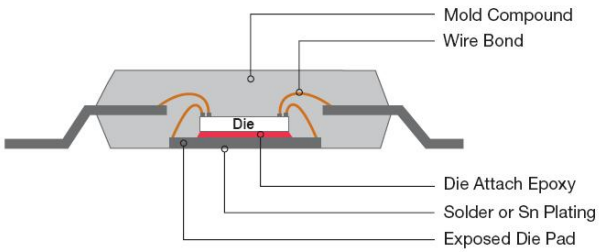
  - Reflections occur due to interconnect



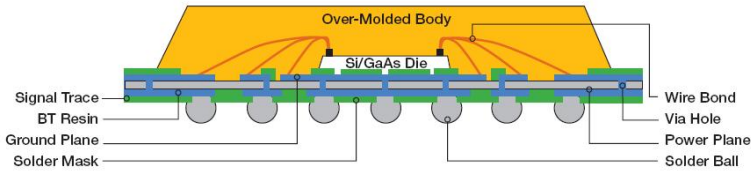
$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}$$

Why is packaging limiting performance?

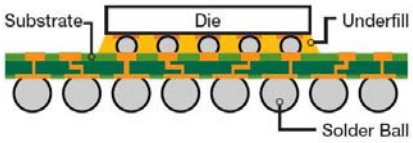
- **Aggressive Package Design Helps, but is expensive…**
  - **95% of VLSI design-starts are wire bonded**
  - **Goal: Extend the life of wire bonded packages**



QFP – Wire Bond : 4.5nH → $0.22 / pin



BGA – Wire Bond : 3.7nH → $0.34 / pin ***



BGA – Flip-Chip : 1.2nH → $0.63 / pin

Why Now?

Cost

- Historically, the transistor delay has dominated performance.
- Inexpensive packaging has met the electrical performance needs.

Faster Risetimes

- As transistors shrink, faster risetimes can be created.
- Everything in the package becomes a transmission line.

Impedance Matching

- The impedance of the package is not matched to the system.
- This leads to reflections from the inductive wire bond in the package

Current Solution to Reflections

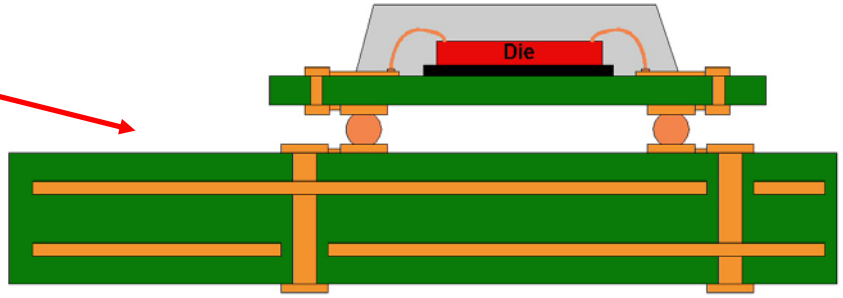
- **Live with the Signal Path Reflections**

1) Run the signals slow enough so that reflections are small

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \quad < 10\%$$

2) Terminate Signals on the Mother board so that reflections are absorbed

On Mother Board Termination



Current Solution to Reflections

- **Limitations of Approach**

1) Run the signals slow enough so that reflections are small

- **Limits System Performance**

2) Terminate Signals on the Mother board so that reflections are absorbed

- **This only eliminates primary reflections, the second still exists**

Proposed Solutions – Impedance Compensation

- **Add Capacitance Near Bond Wire to Reduce Impedance**

- Adding additional capacitance lowers the wire bond impedance
- Impedance can be matched to system, reducing reflections

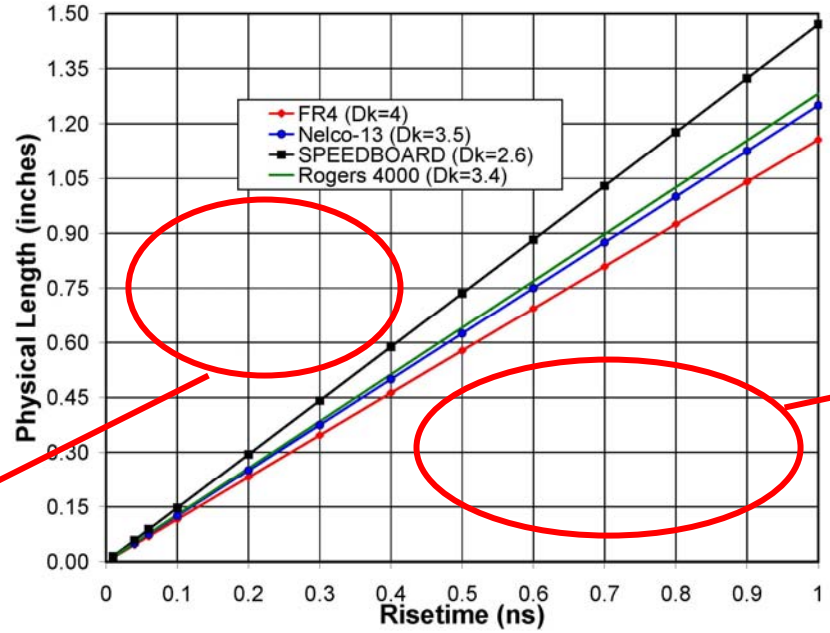
$$Z_{WireBond} = \sqrt{\frac{L_{WireBond}}{C_{WireBond}}}$$

Add Capacitance to lower Z

Proposed Solutions – Impedance Compensation

- **If the capacitance is close to the wire bond, it will alter its impedance**

- Electrical lengths less than 20% of risetime are treated as lumped elements
- For modern dielectrics, anything within 0.15" of wire bond is lumped

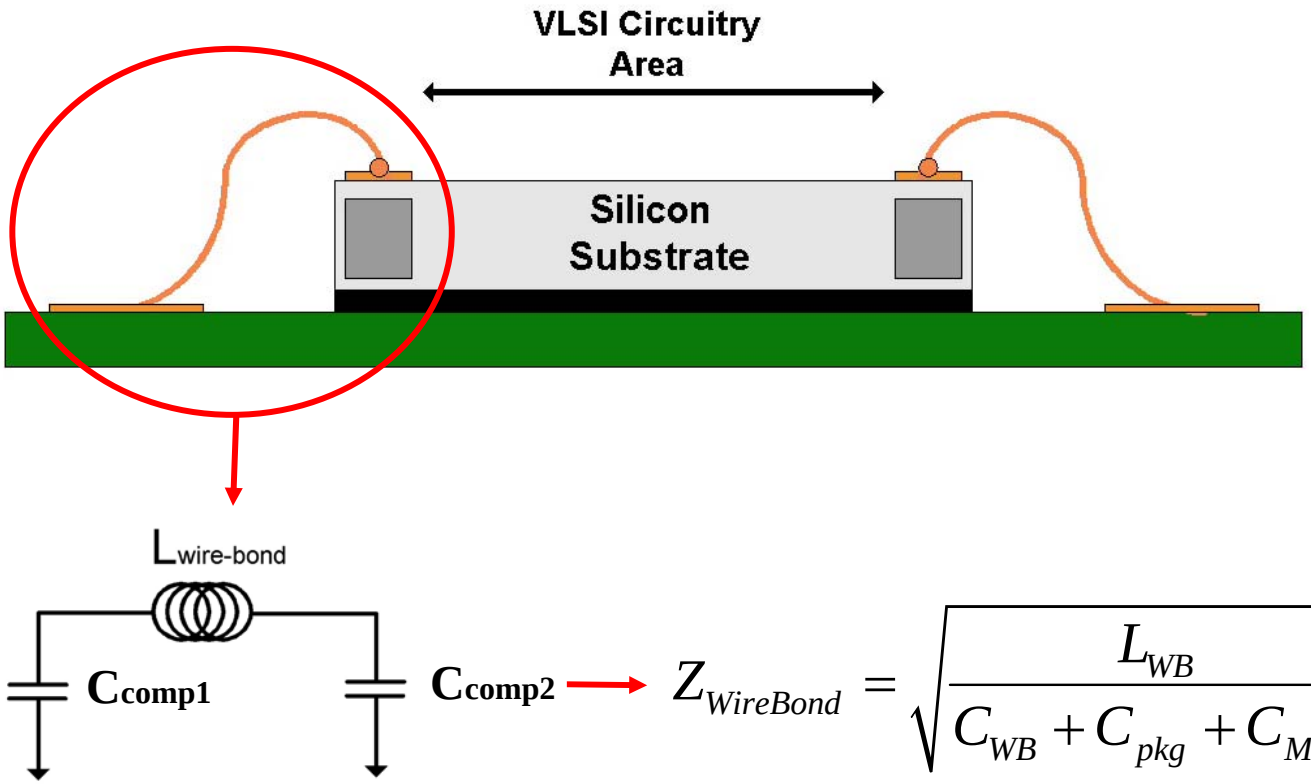


Treated as Lumped Element

Treated as Distributed Element

Proposed Solutions – Impedance Compensation

- **Capacitance on the IC or Package is close enough to alter impedance**

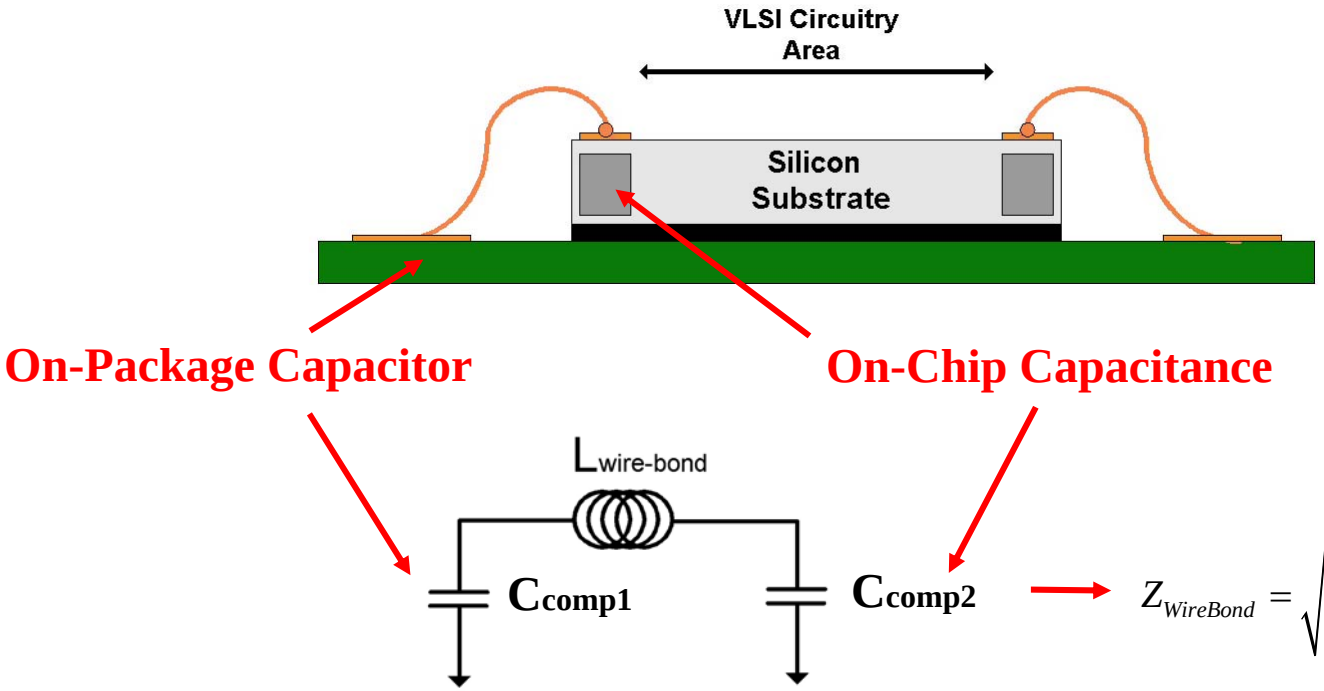


$$Z_{WireBond} = \sqrt{\frac{L_{WB}}{C_{WB} + C_{pkg} + C_{MIM}}} = 50\Omega's$$

Static Compensator

- **Capacitor values chosen prior to fabrication**

  - Equal amounts of capacitance are used on-chip and on-package

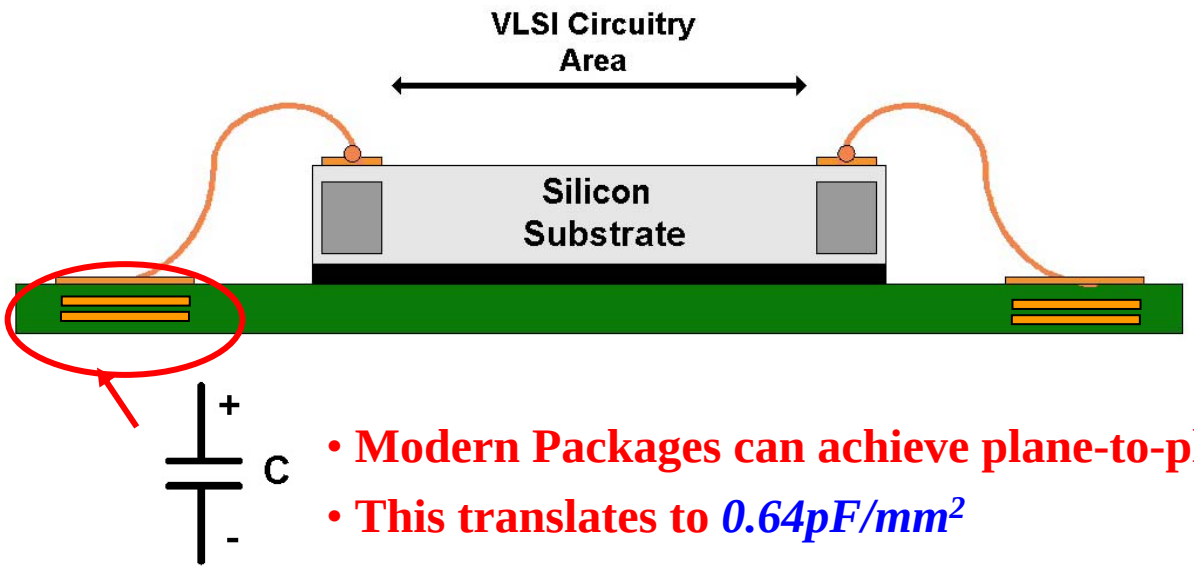


$$Z_{WireBond} = \sqrt{\frac{L_{WB}}{C_{WB} + C_{pkg} + C_{MIM}}} = 50\Omega's$$

Static Compensator

- **On-Package Capacitors**

  - Embedded capacitor construction is used
  - No components are needed, reducing package cost
  - Capacitance values needed can be implemented using this construction

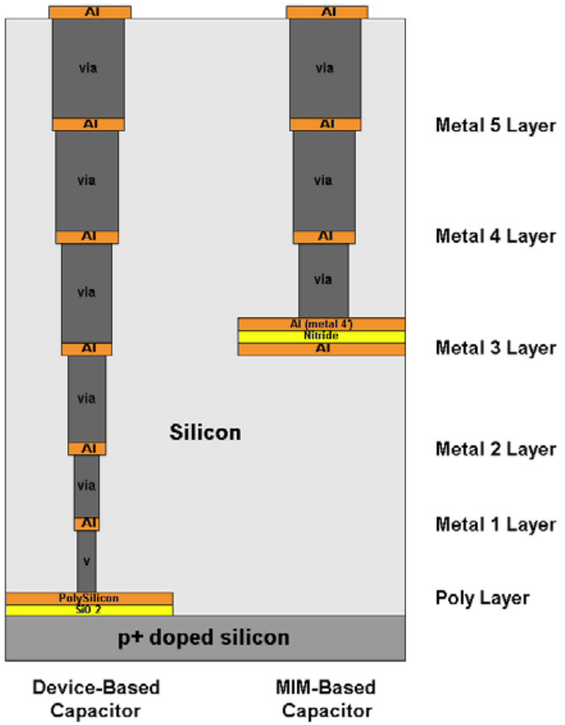


- Modern Packages can achieve plane-to-plane separations of *t=0.002”*
- This translates to *0.64pF/mm²*

Static Compensator

- **On-Chip Capacitors**

  - Device and MIM capacitors are evaluated
  - Targeting area beneath wire bond pad, which is typically unused



0.1um BPTM Process

- **Device-Based Capacitor : *13 fF/um²***
- **MIM-Based Capacitor : *1.1 fF/um²***

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Static Compensator

- **Wire Bond Modeling**

  - Typical VLSI wire bond lengths range from 1mm to 5mm
  - Electrical parameter extraction is used to find L and C or wire bond

Length	L	C	Z_0
1mm	0.569nH	26fF	148Ω
2mm	1.138nH	52fF	148Ω
3mm	1.707nH	78fF	148Ω
4mm	2.276nH	104fF	148Ω
5mm	2.845nH	130fF	148Ω

Static Compensator

- **On-Package Capacitor Sizing**

  - Capacitor values are found to match wire bond to 50Ω
  - Area is evaluated for feasibility

Length	C_{comp1}		C_{comp2}		
L	C	Area	C	$Area_{MIM}$	$Area_{Device}$
1mm	102 fF	388 um^2	102 fF	10 um^2	2.7 um^2
2mm	208 fF	554 um^2	208 fF	14 um^2	3.9 um^2
3mm	325 fF	692 um^2	325 fF	18 um^2	4.9 um^2
4mm	450 fF	815 um^2	450 fF	21 um^2	5.8 um^2
5mm	575 fF	921 um^2	575 fF	24 um^2	6.5 um^2

Experimental Results: Static Compensator

- **Time Domain Analysis (TDR)**

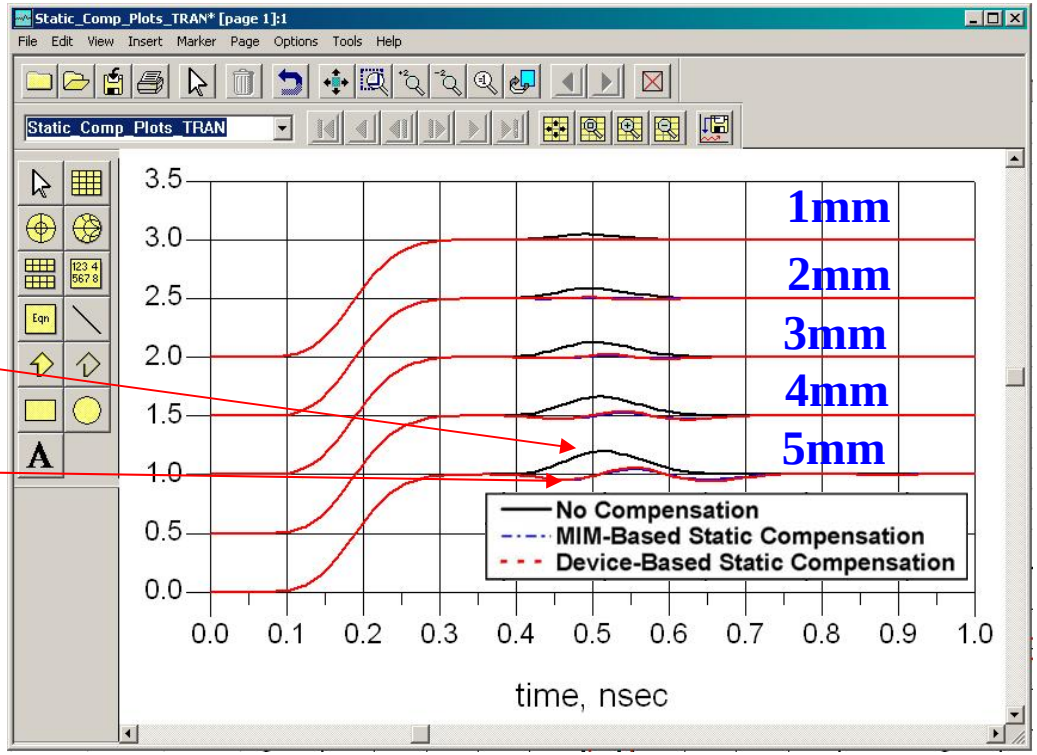
- Simulation Performed using
Advanced Design System* from *Agilent

$Length_{wb}$	$\Gamma_{No-Comp}$	$\Gamma_{MIM-Comp}$	$\Gamma_{Device-Comp}$
1 mm	4.5%	0.05%	0.5%
2 mm	8.7%	0.4%	1.2%
3 mm	12.7%	1.3%	2.4%
4 mm	16.4%	2.7%	4.1%
5 mm	19.8%	4.8%	6.0%

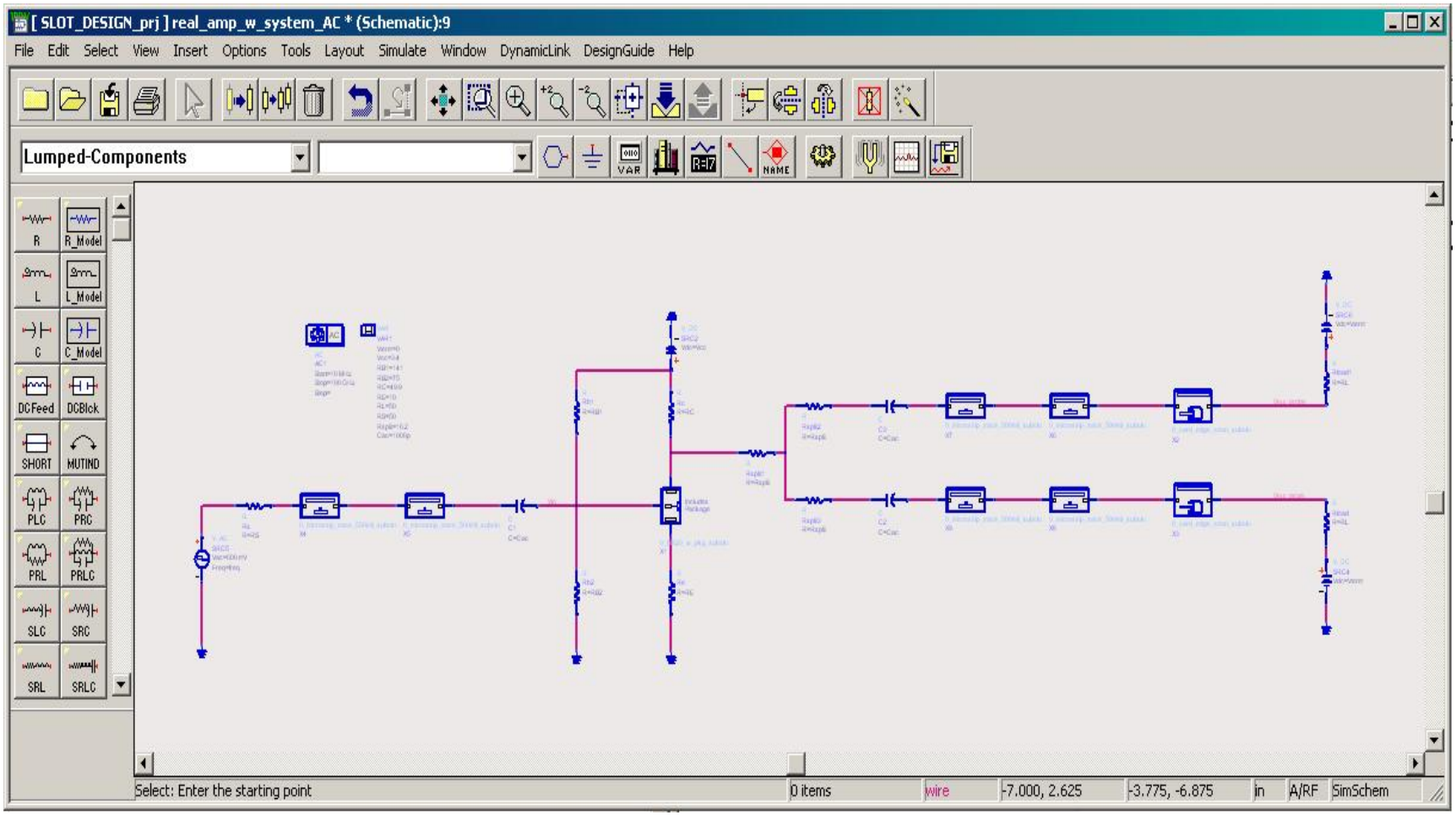
Worst Case : 5mm

No Static Capacitance = 19.8%

w/ Static Capacitance = 4.8%

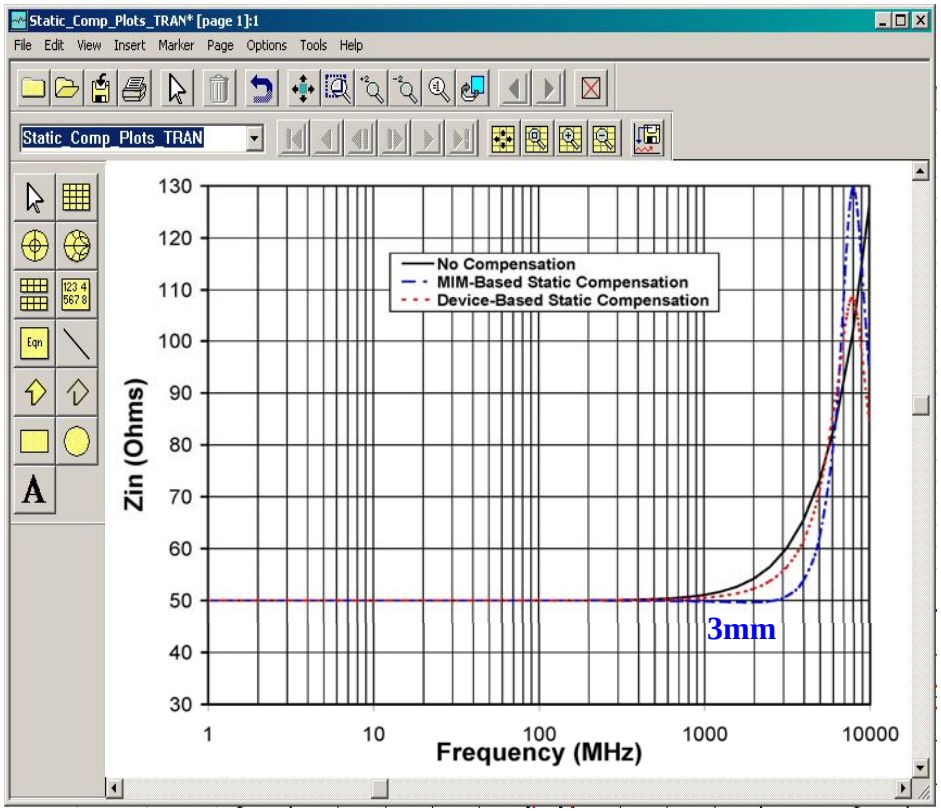


Frequency Domain Analysis (Z_{in})



Experimental Results: Static Compensator

- **Frequency Domain Analysis (Z_{in})**



Worst Case : 5mm

$f_{+/-10\%}$ No Static Capacitance = 1.9 GHz

$f_{+/-10\%}$ w/ Static Capacitance = 3.0 GHz

$Length_{wb}$	$f_{No-Comp}$	$f_{MIM-Comp}$	$f_{Device-Comp}$
1 mm	9.3 GHz	14 GHz	12 GHz
2 mm	4.7 GHz	7.1 GHz	5.7 GHz
3 mm	3.1 GHz	4.8 GHz	3.8 GHz
4 mm	2.4 GHz	3.7 GHz	2.9 GHz
5 mm	1.9 GHz	3.0 GHz	2.5 GHz

Static Compensator

- **Limitations of Approach**

  - **Process/Design variation in wire bonds and capacitors lead to error**
  - **Each wire bond must be evaluated for compensation requirements**

- **Possible Enhancement**

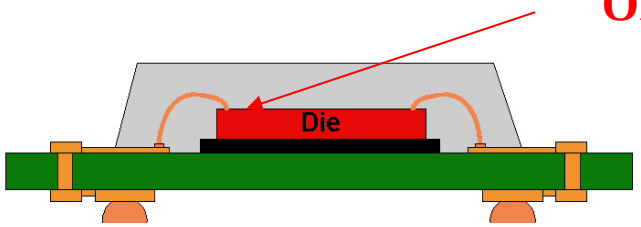
  - **Altering compensation capacitance after fabrication**
  - **i.e., *Dynamic Compensator***

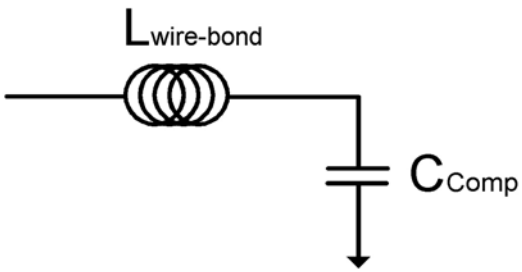
Dynamic Compensator

- **Programmable capacitance is placed on-chip**

  - On-chip capacitance is close enough to alter wire bond impedance
  - Active circuitry on-chip can switch in different amounts of capacitance

On-Chip Programmable Compensation



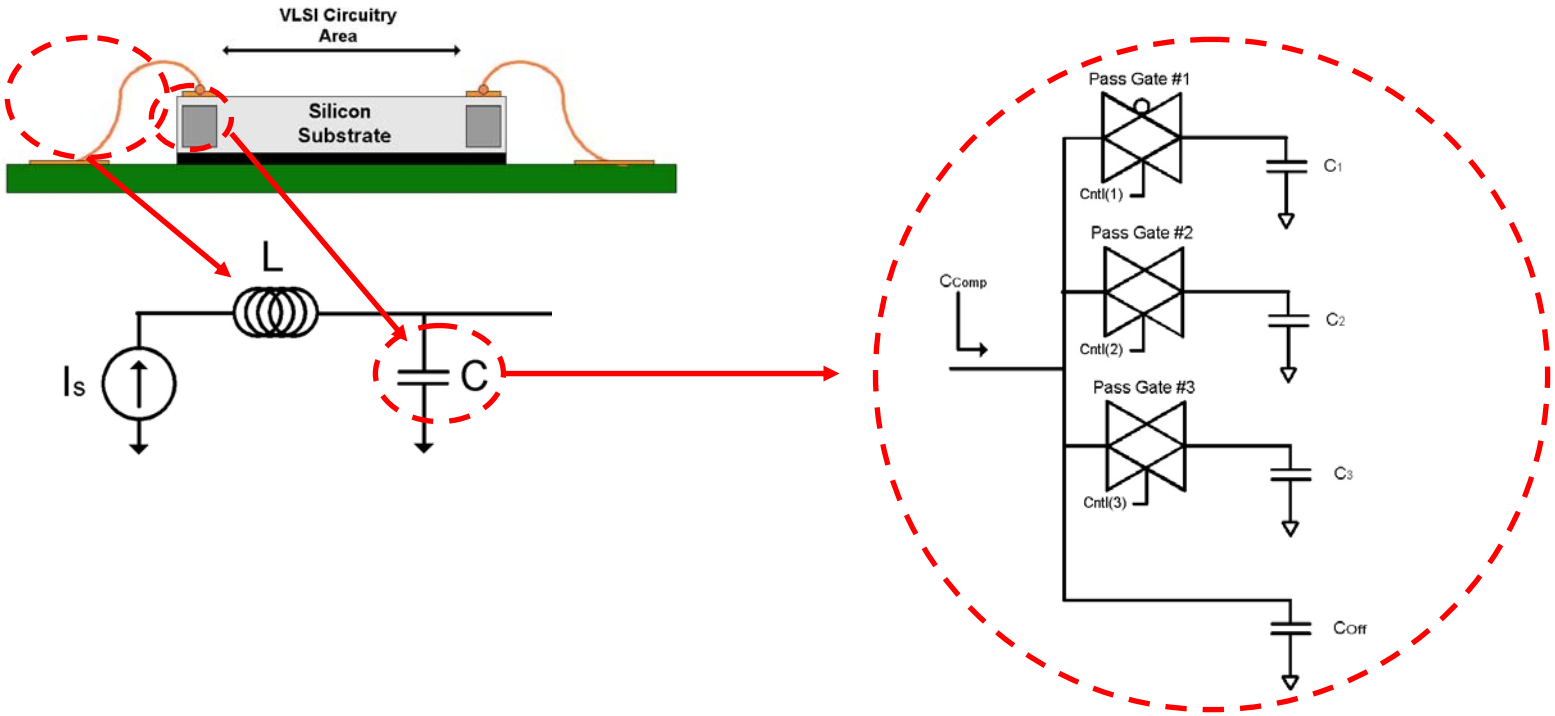


$$\Rightarrow \quad Z_{WireBond} = \sqrt{\frac{L_{WB}}{C_{WB} + C_{Comp}}} = 50\Omega's$$

Dynamic Compensator

- **Pass Gates are used to switch in on-chip capacitors**

  - **Pass gates connect on-chip capacitance to the wire bond inductance**
  - **Pass gates have control signals which can be programmed after fabrication**

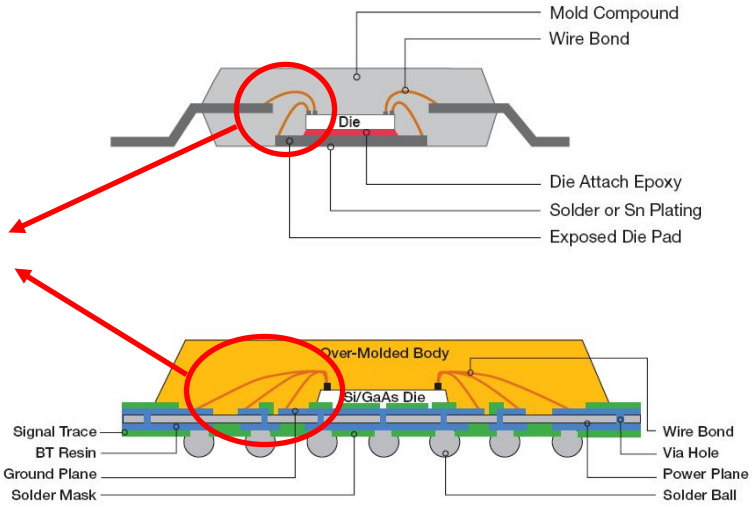


Dynamic Compensator

- **On-Chip circuitry is independent of package**

  - **Compensation works across multiple package technologies**
  - **This decouples IC and Package design**

Only IC technology is used for compensation



Dynamic Compensator

- **On-Chip capacitor sizing**

  - The on-chip capacitance performs the compensation to 50Ω
  - The circuit must cover the entire range of wire bond inductances
  - The diffusion capacitance of the pass gates must be included in the analysis

Length	C_{comp}
L	C
1mm	202 fF
2mm	403 fF
3mm	605 fF
4mm	806 fF
5mm	1008 fF

$200\ fF \leq C_{comp} \leq 1010\ fF$

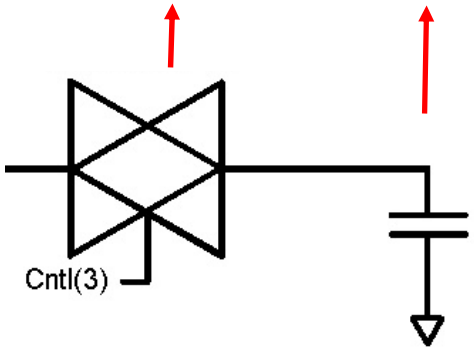
Dynamic Compensator

- **Compensator Design**

  - The on-chip capacitance performs the compensation to 50Ω
  - The diffusion capacitance of the pass gates must be included in the analysis

Length	C_{comp}
L	C
1mm	202 fF
2mm	403 fF
3mm	605 fF
4mm	806 fF
5mm	1008 fF

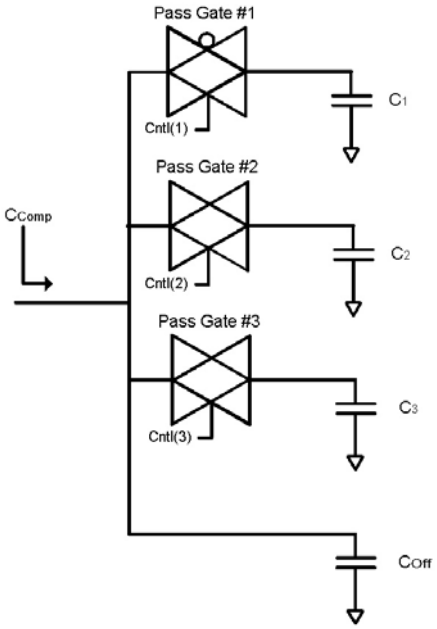
$$C_{bank} = {}^{1}/_{3}(C_{bank}) + {}^{2}/_{3}(C_{bank})$$



Dynamic Compensator

- **Capacitance Design**

  - Pass Gates are sized to drive the on-chip capacitance
  - Each *bank* of capacitance includes the pass gates



$C_{bank1} = C_{pg1} + C_{int1}$

$C_{bank2} = C_{pg2} + C_{int2}$

$C_{bank3} = C_{pg3} + C_{int3}$

C_{Off} = Range Offset

Dynamic Compensator

- **Capacitance Design**

- Again, both MIM and Device-based capacitors are evaluated for area

	MIM-Based	Device-Based
Component	Area (W $\times$ L)	Area (W $\times$ L)
Pass Gate #1	32.4μm x 0.1μm	32.4μm x 0.1μm
Pass Gate #2	62.5μm x 0.1μm	62.5μm x 0.1μm
Pass Gate #3	129.6μm x 0.1μm	129.6μm x 0.1μm
C_{off}	8.5μm x 8.5μm	2.5μm x 2.5μm
C_1	11μm x 11μm	3.3μm x 3.3μm
C_2	15.5μm x 15.5μm	4.6μm x 4.6μm
C_3	22μm x 22μm	6.6μm x 6.6μm
Total	65μm x 65μm	25μm x 25μm

Experimental Results: Dynamic Compensator

- **Time Domain Analysis (TDR)**

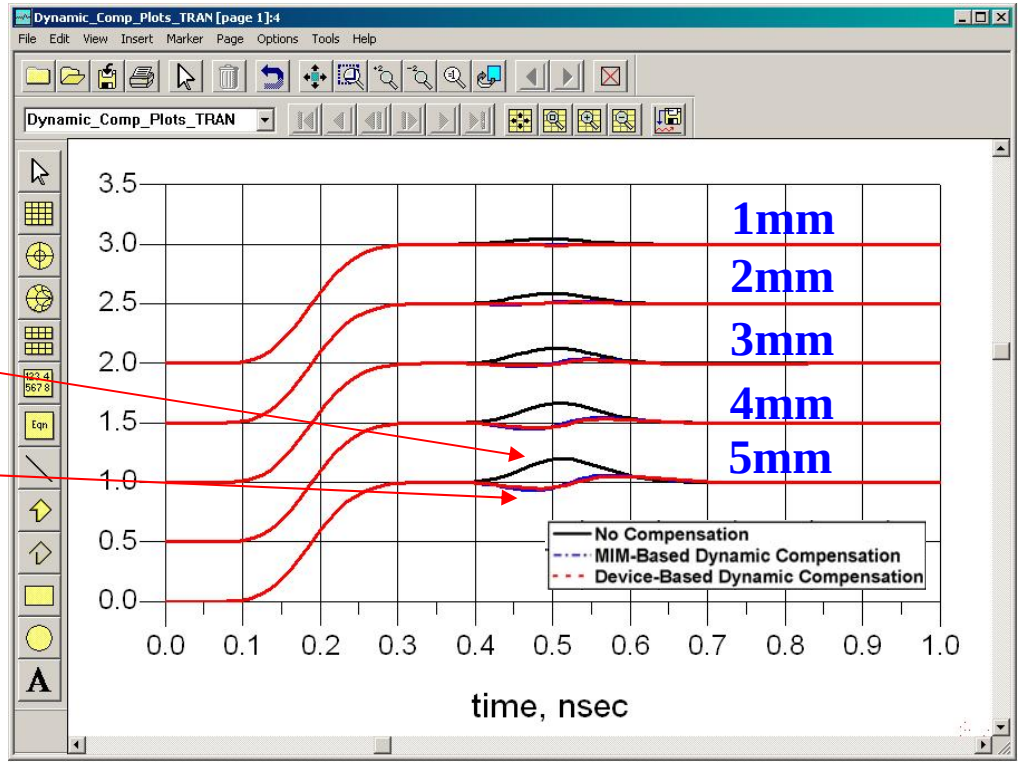
- Simulation Performed using
Advanced Design System* from *Agilent

$Length_{wb}$	$\Gamma_{No-Comp}$	$\Gamma_{MIM-Comp}$	$\Gamma_{Device-Comp}$	Setting
1 mm	4.5%	1.0%	1.0%	001
2 mm	8.7%	1.8%	1.3%	011
3 mm	12.7%	3.6%	3.0%	100
4 mm	16.4%	4.3%	3.3%	110
5 mm	19.8%	6.0%	5.0%	111

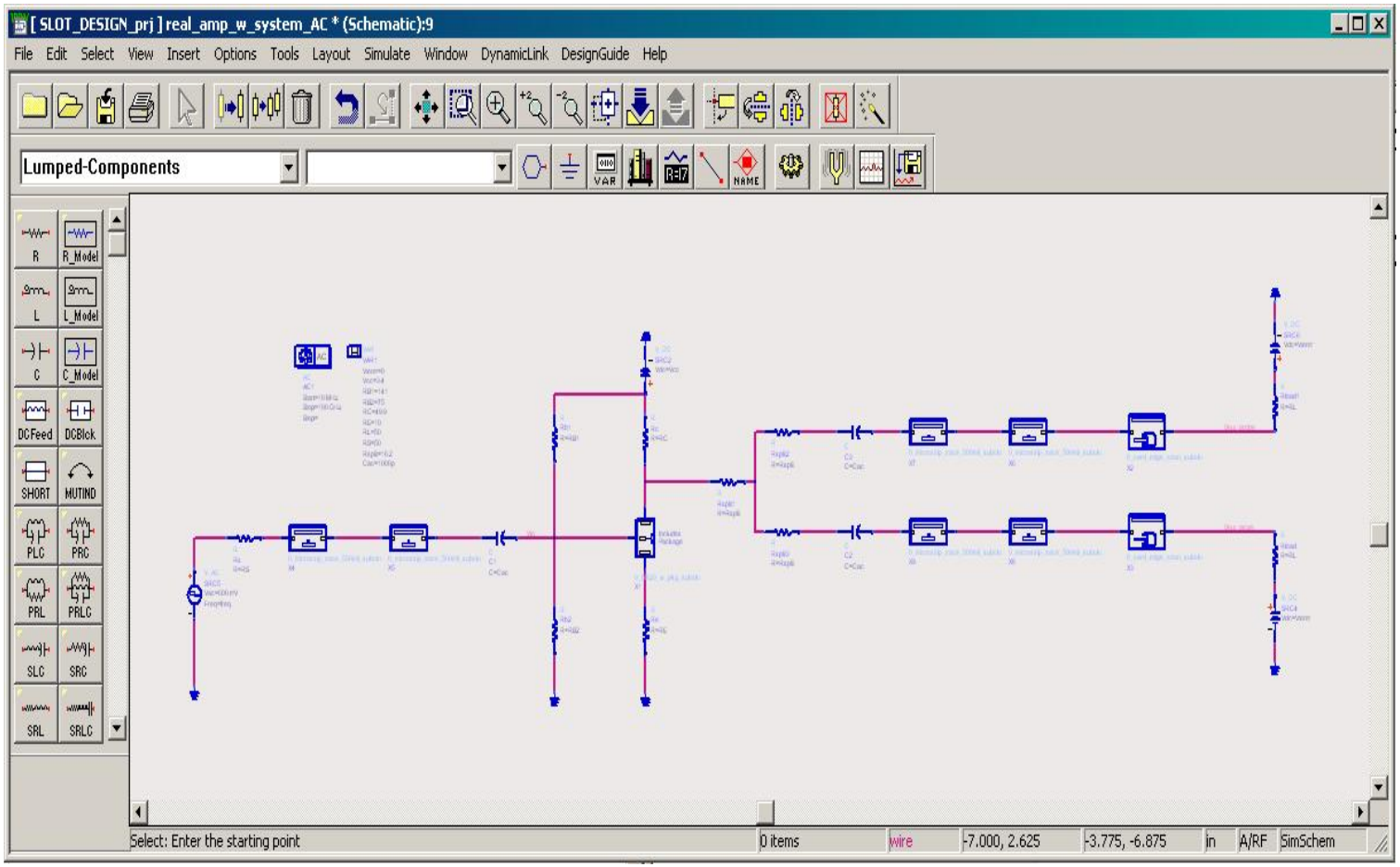
Worst Case : 5mm

No Dynamic Capacitance = 19.8%

w/ Dynamic Capacitance = 5.0%

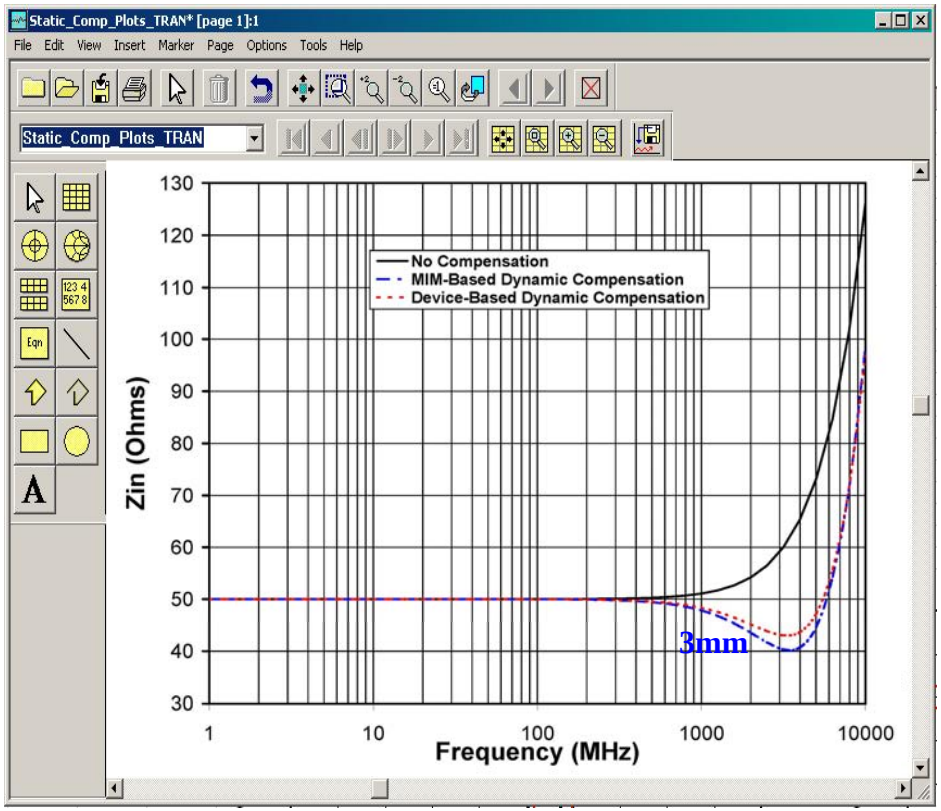


Frequency Domain Analysis (Z_{in})



Experimental Results: Dynamic Compensator

- **Frequency Domain Analysis (Z_{in})**



Worst Case : 5mm

$f_{+/-10\%}$ No Dynamic Capacitance = 1.9 GHz

$f_{+/-10\%}$ w/ Dynamic Capacitance = 4.1 GHz

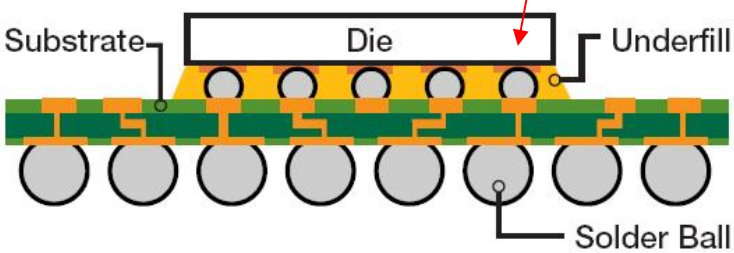
$Length_{wb}$	$f_{No-Comp}$	$f_{MIM-Comp}$	$f_{Device-Comp}$
1 mm	9.3 GHz	20 GHz	20 GHz
2 mm	4.7 GHz	10.1 GHz	10 GHz
3 mm	3.1 GHz	6.8 GHz	6.7 GHz
4 mm	2.4 GHz	5.2 GHz	5.1 GHz
5 mm	1.9 GHz	4.2 GHz	4.1 GHz

Inductive Compensator

- **The same theory can be applied to capacitive interconnect**
- **Spiral Inductors can be added on-chip**

- On-chip inductance is close enough to alter capacitive interconnect impedance
- Spiral inductors are a proven on-chip technology

On-Chip Spiral Inductors



$$\Rightarrow \quad Z_{Flip-Chip} = \sqrt{\frac{L_{FC} + L_{Comp}}{C_{FC}}} = 125\Omega's$$

Experimental Results: Inductor Compensator

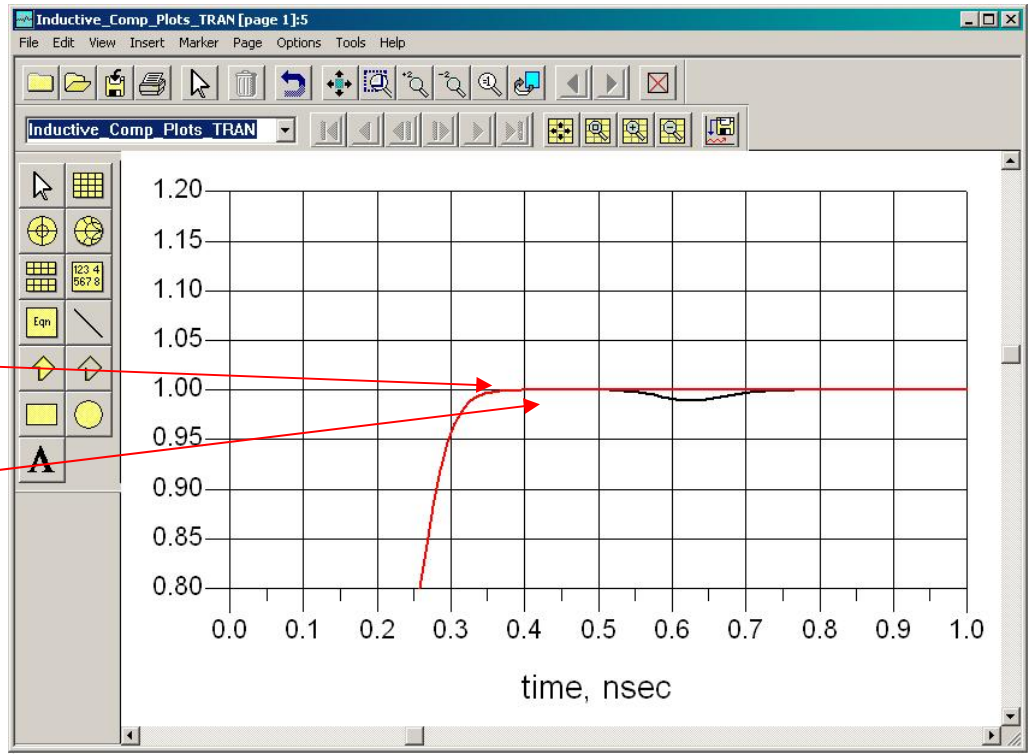
- **Time Domain Analysis (TDR)**

- Simulation Performed using
Advanced Design System* from *Agilent

Worst Case : 5mm

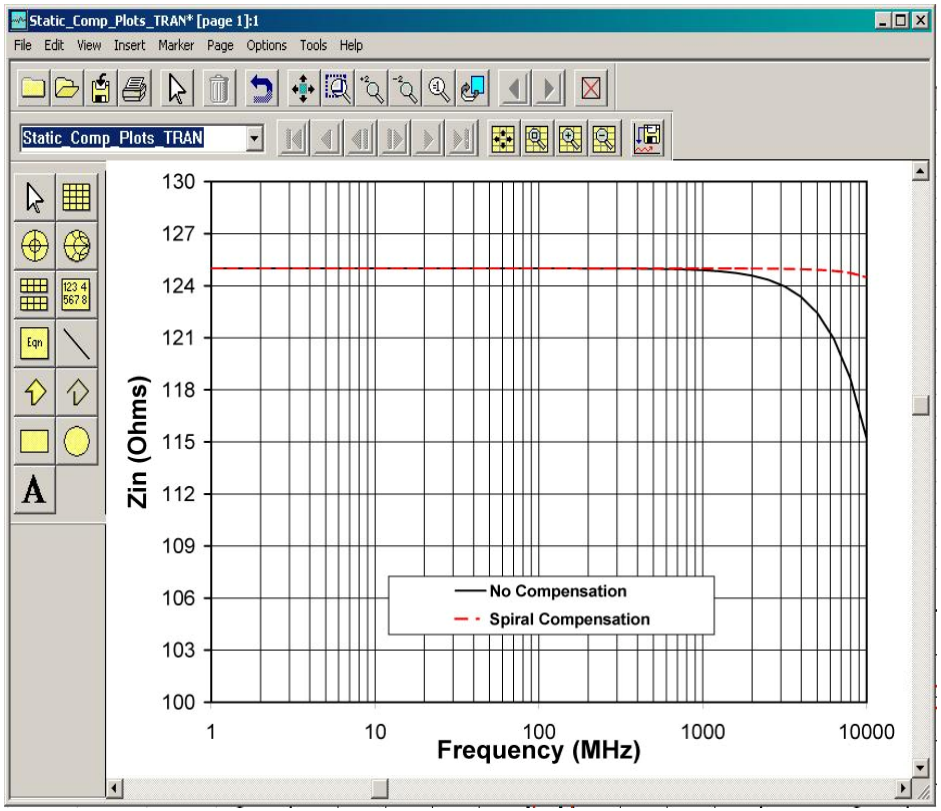
No Inductance = 2%

w/ Spiral Inductance = >0.1%



Experimental Results: Inductive Compensator

- **Frequency Domain Analysis (Z_{in})**



Flip-Chip Matching

$f_{+/-10\%}$ No Spiral Inductance = 10 GHz

$f_{+/-10\%}$ w/ Spiral Inductance > 15 GHz

Summary

- Package Interconnect causes reflections which limits system performance

- The move toward Advanced Packaging is Resisted due to Cost

- Adding On-Chip & On-Package capacitors does not add cost

- A Static and Dynamic Compensation Approach can match the package interconnect impedance to the system

- The same approach can be applied to future interconnect structures which look capacitive

Questions?

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