ECEN689: Special Topics in Optical Interconnects Circuits and Systems
Spring 2022

Lecture 5: Transimpedance Amplifiers (TIAs)

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Announcements

- Homework 2 is posted on website and due today

- Exam 1 Mar 10
  - In class
  - One double-sided 8.5x11 notes page allowed
  - Bring your calculator
  - Covers through Lecture 6

- Reading
  - Sackinger Chapter 5
  - Razavi Chapter 4

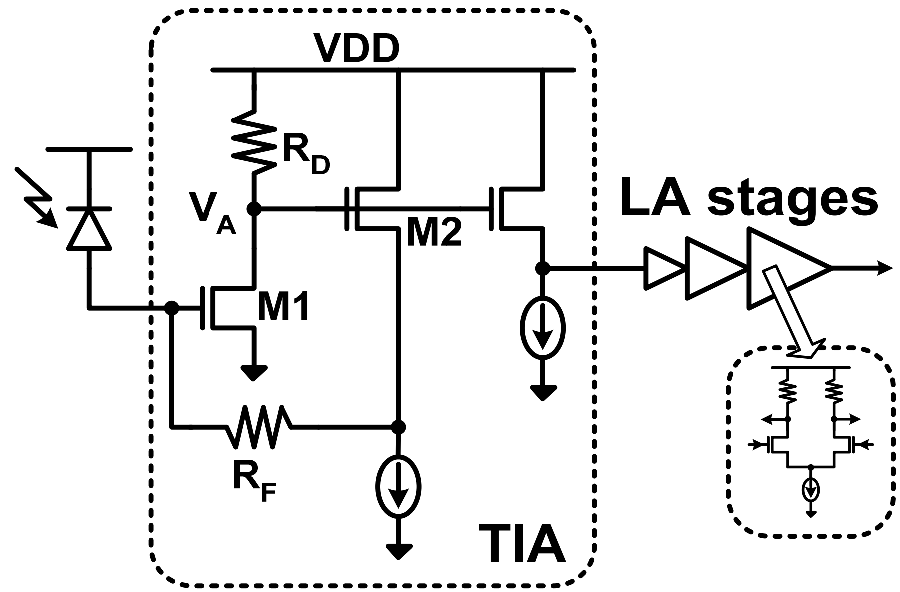
Agenda

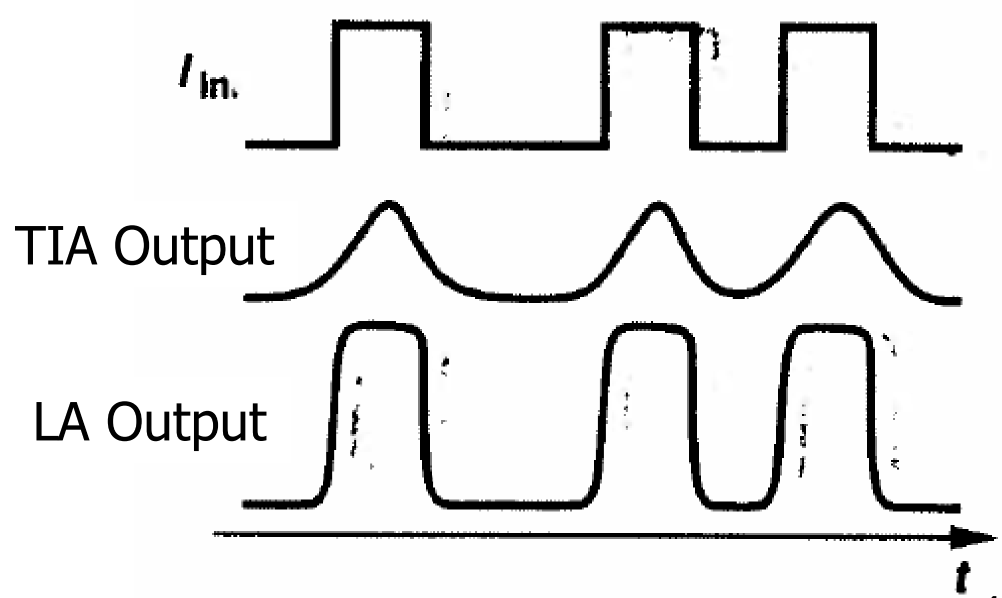
- Optical Receiver Overview
- Transimpedance Amplifiers
  - Common-Gate TIAs
  - Feedback TIAs
  - Common-Gate & Feedback TIA Combinations
  - Differential TIAs
- Integrating Optical Receivers
- Equalization in Optical Front-Ends

Optical Receiver Technology

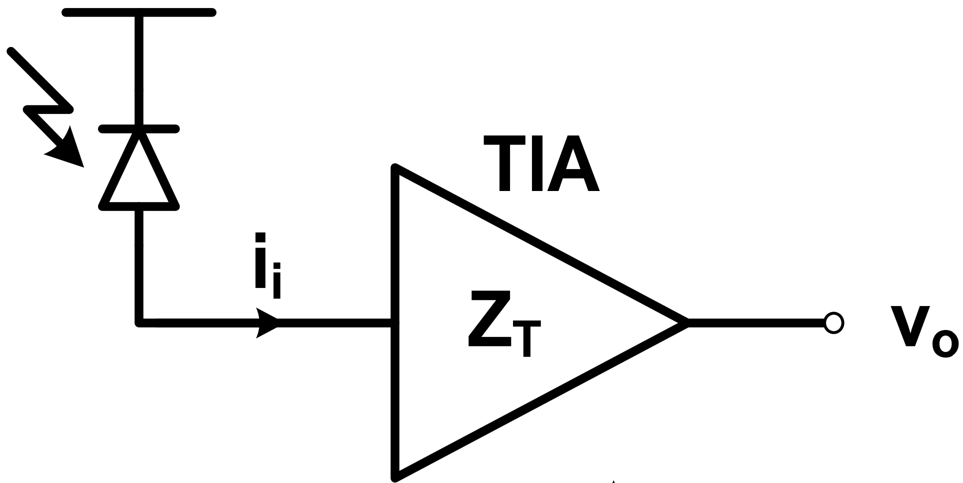
- Photodetectors convert optical power into current
  - p-i-n photodiodes
  - Waveguide Ge photodetectors

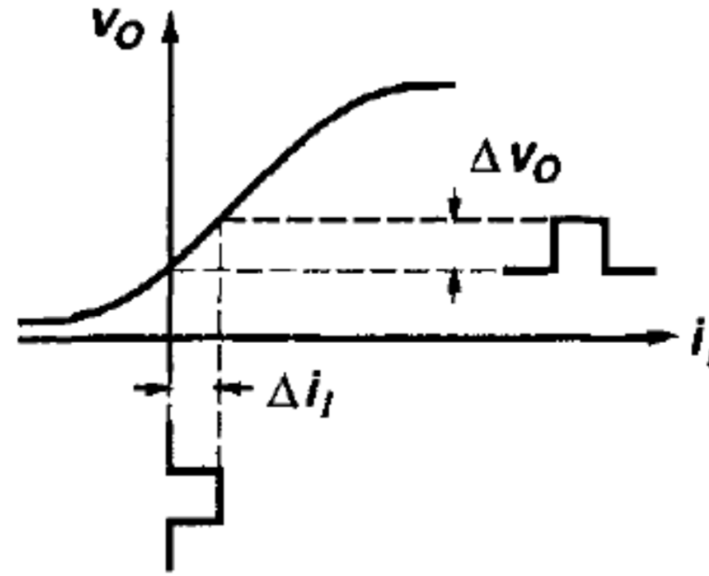
- Electrical amplifiers then convert the photocurrent into a voltage signal
  - Transimpedance amplifiers
  - Limiting amplifiers
  - Integrating optical receiver





Transimpedance Amplifier (TIA)



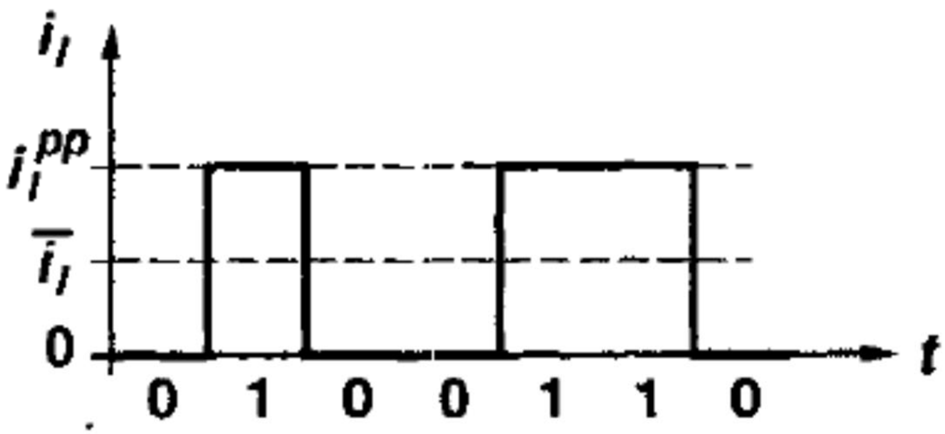


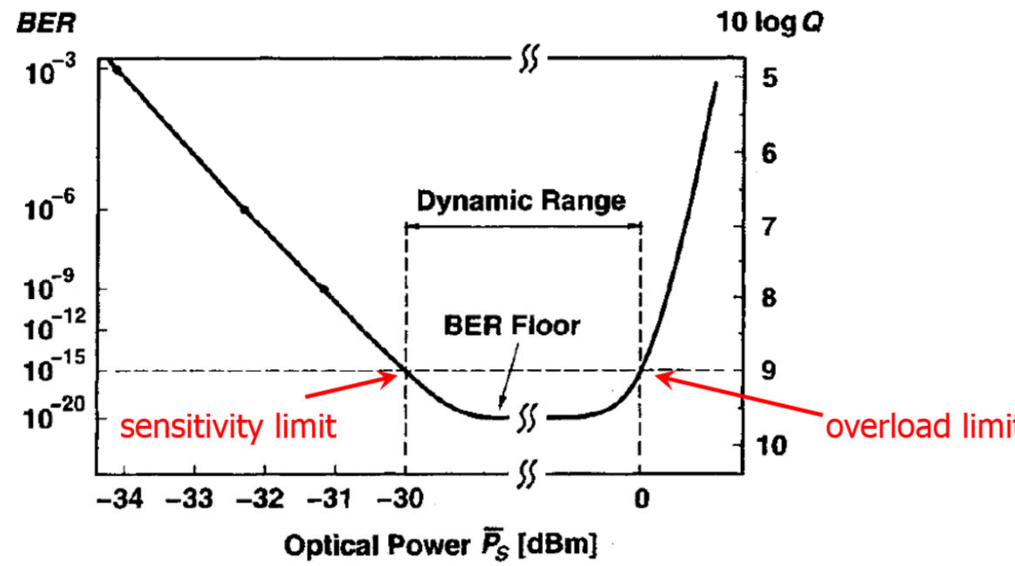
Transimpedance $Z_T = \dfrac{\Delta v_o}{\Delta i_i} \quad (\Omega)$

Also expressed in units of dBΩ by $20\log(|Z_T|)$

- Key design objectives
  - High transimpedance gain
  - Low input resistance for high bandwidth and efficient gain
- For large input currents, the TIA gain can compress and pulse-width distortion/jitter can result

Maximum Currents



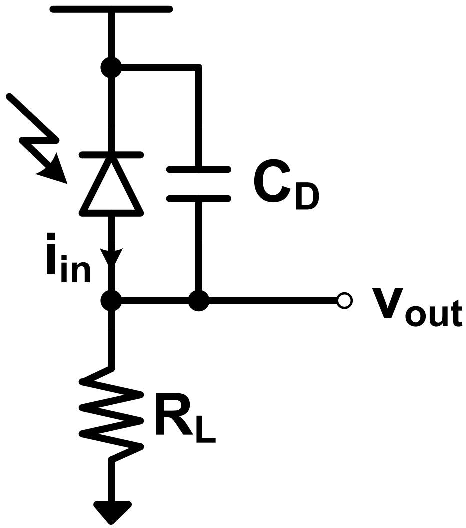


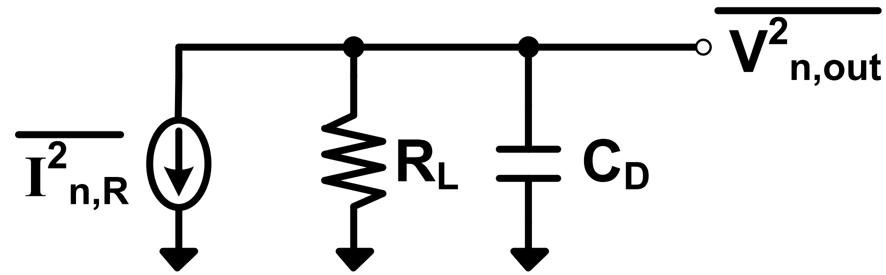
- Input Overload Current
  - The maximum peak-to-peak input current for which we can achieve the desired BER
  - Assuming high extinction ratio $i_{ovl}^{pp} = 2R\overline{P}_{ovl}$
- Maximum Input Current for Linear Operation
  - Often quantified by the current level for a certain gain compression (1dB)

$$i_{lin}^{pp} < i_{ovl}^{pp}$$

Resistive Front-End

[Razavi]





$$\overline{V^2_{n,out}} = \int_0^\infty \overline{I_n^2} Z_T^2 df = \int_0^\infty \frac{4kT}{R_L}\left(\frac{R}{1+j2\pi fRC}\right)^2 df = \frac{kT}{C_D}$$

$$R_T = R_{in} = R_L$$

$$BW_{3dB} = \omega_p = \frac{1}{R_{in}C_D} = \frac{1}{R_L C_D}$$

$$\overline{I^2_{n,in}} = \frac{\overline{V^2_{n,out}}}{R_L^2} = \frac{kT}{R_L^2 C_D}$$

$$I_{n,in,rms} = \frac{\sqrt{KT/C_D}}{R_L}$$

- Direct trade-offs between transimpedance, bandwidth, and noise performance

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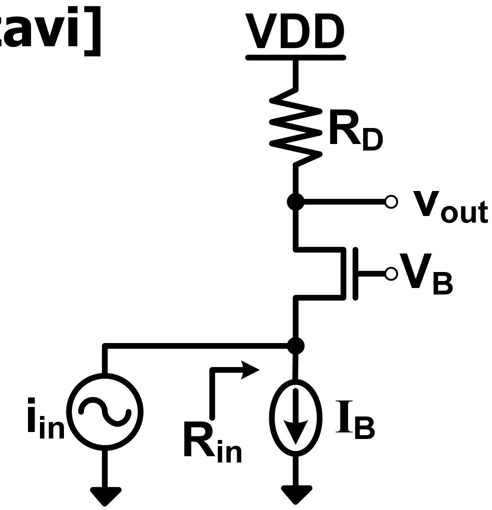
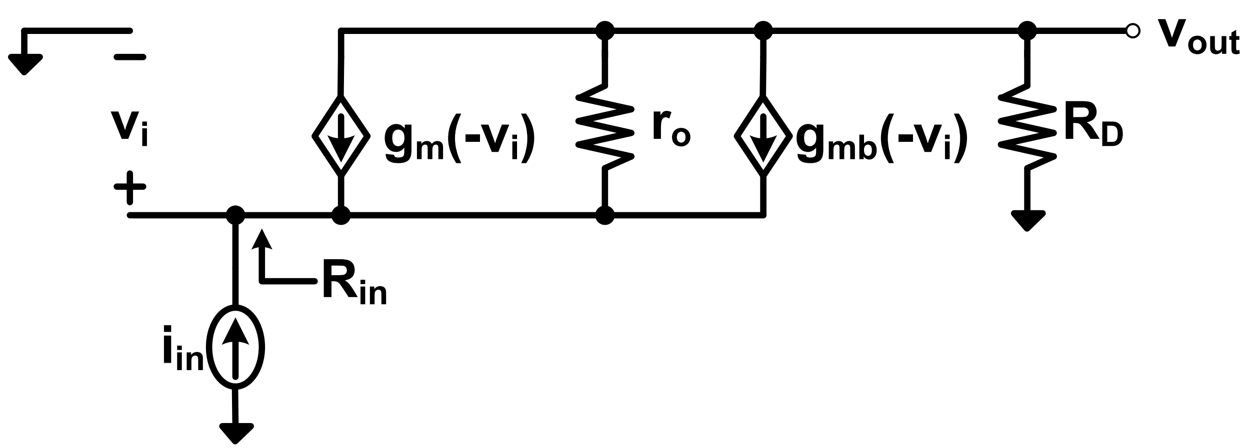
Common-Gate TIA

[Razavi]





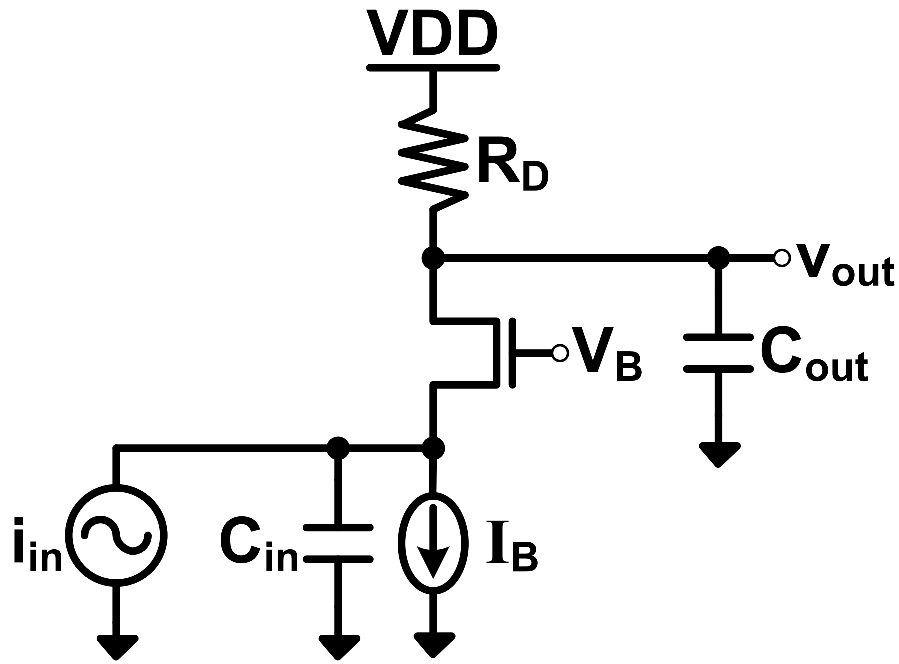
$$R_T = R_D$$

$$R_{in} = \frac{r_o + R_D}{1 + (g_m + g_{mb})r_o} \approx \frac{1}{g_m}$$

- Input resistance (input bandwidth) and transimpedance are decoupled

Common-Gate TIA Frequency Response

[Razavi]

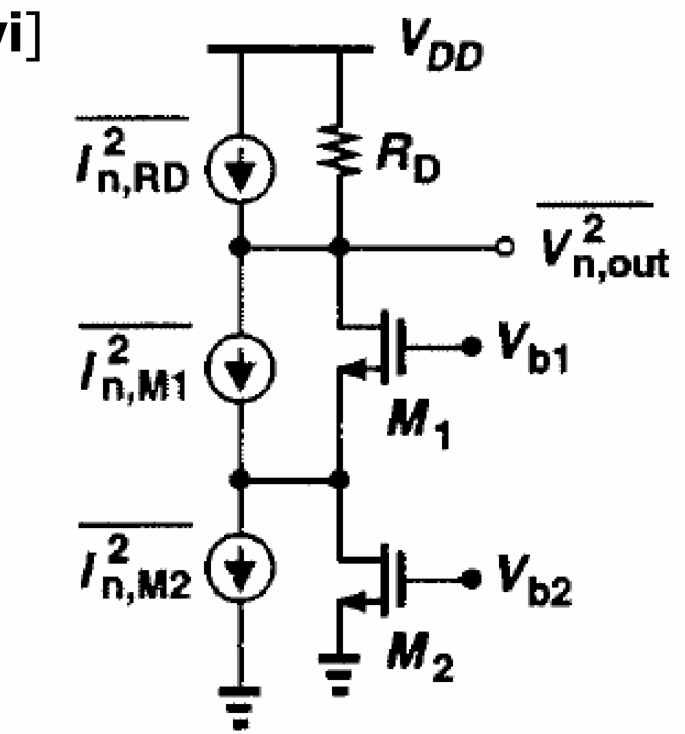


Neglecting transistor r_o : $$\frac{v_{out}}{i_{in}} = \frac{R_D}{\left(1 + s\dfrac{C_{in}}{g_{m1} + g_{mb1}}\right)\left(1 + sR_D C_{out}\right)}$$

- Often the input pole may dominate due to large photodiode capacitance (100 – 500fF)

Common-Gate TIA Noise

[**Razavi**]



Neglecting transistor r$_o$:

$$\overline{V^2_{n,out}} = \left(\overline{I^2_{n,M2}} + \overline{I^2_{n,RD}}\right) R_D^2 = 4kT\left(\frac{2}{3}g_{m2} + \frac{1}{R_D}\right) R_D^2 \quad \left(\frac{\mathbf{V}^2}{\mathbf{Hz}}\right)$$

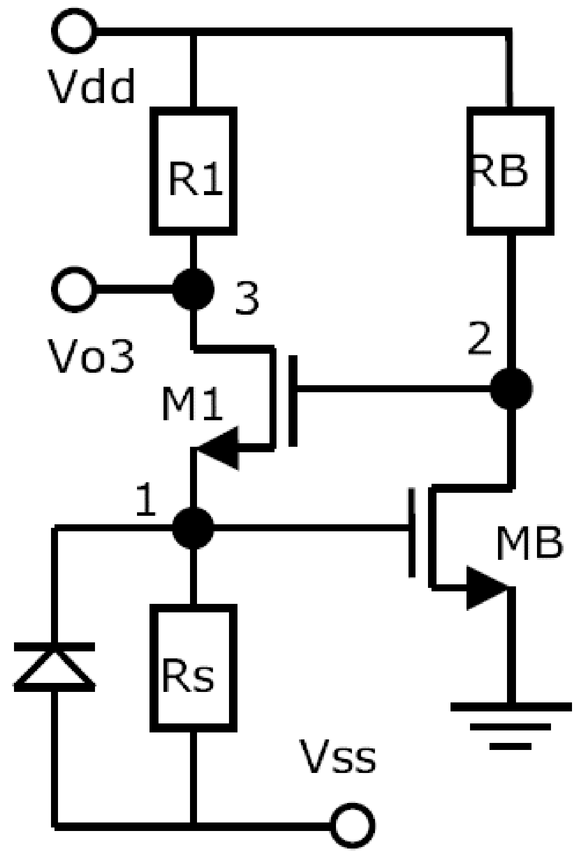
$$\overline{I^2_{n,in}} = 4kT\left(\frac{2}{3}g_{m2} + \frac{1}{R_D}\right) \quad \left(\frac{\mathbf{A}^2}{\mathbf{Hz}}\right)$$

- Both the bias current source and RD contribute to the input noise current
- RD can be increased to reduce noise, but voltage headroom can limit this
- Common-gate TIAs are generally not for low-noise applications
- However, they are relatively simple to design with high stability

Regulated Cascode (RGC) TIA

- Input transistor gm is boosted by common-source amplifier gain, resulting in reduced input resistance
- Requires additional voltage headroom
- Increased input-referred noise from the common-source stage

[Park ESSCIRC 2000]

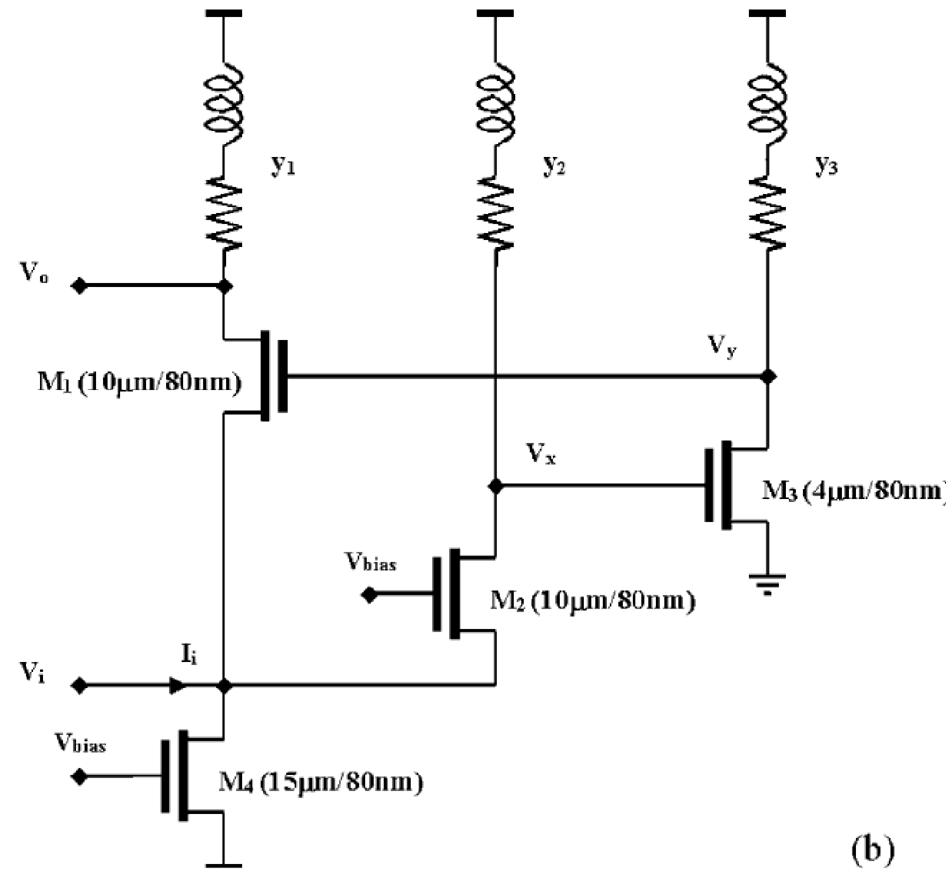


$$Z_{in}(0) \cong \frac{1}{g_{m1}(1+g_{mB}R_B)}$$

CMOS 20GHz TIA

- An additional common-gate stage in the feedback provides further gm-boosting and even lower input resistance
- Shunt-peaking inductors provide bandwidth extension at zero power cost, but very large area cost

[Kromer JSSC 2004]



$$Z_i \approx \frac{1}{g_{m1}\left(1+|A_2A_3|\right)+j\omega C_{\mathrm{i,tot}}}$$

$$A_2 = g_{m2}R_2 \qquad A_3 = -g_{m3}R_3$$

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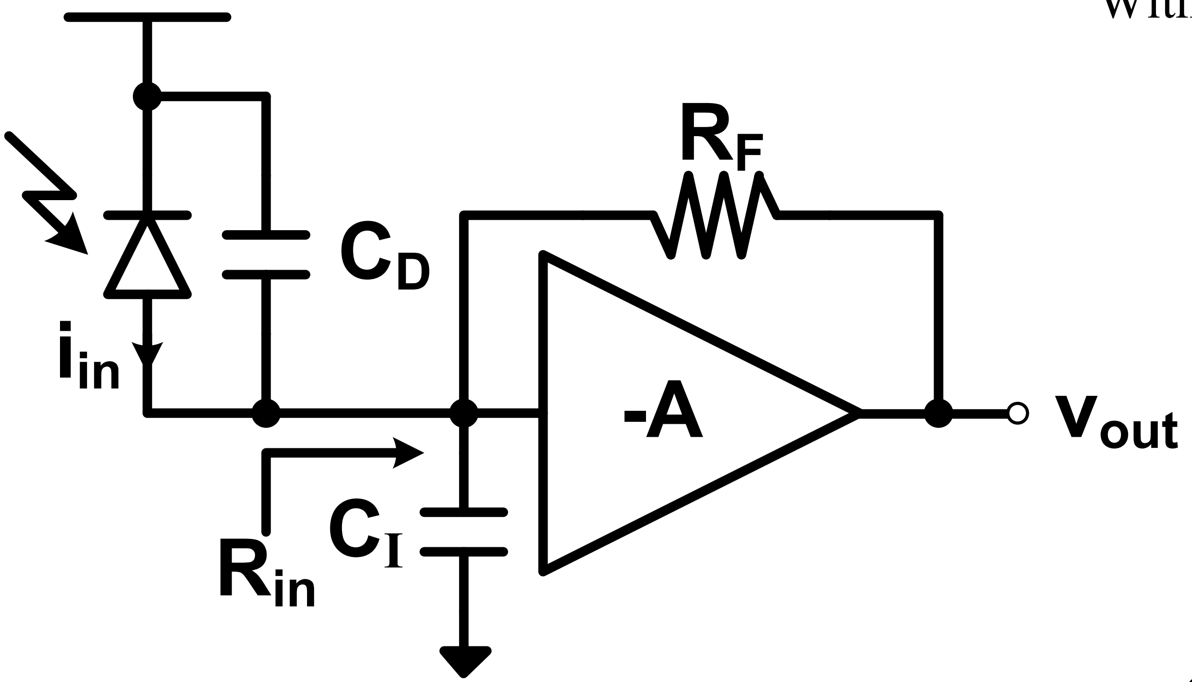
Feedback TIA w/ Ideal Amplifier



With Infinite Bandwidth Amplifier:

$$Z_T(s) = -R_T\left(\frac{1}{1+s/\omega_p}\right)$$

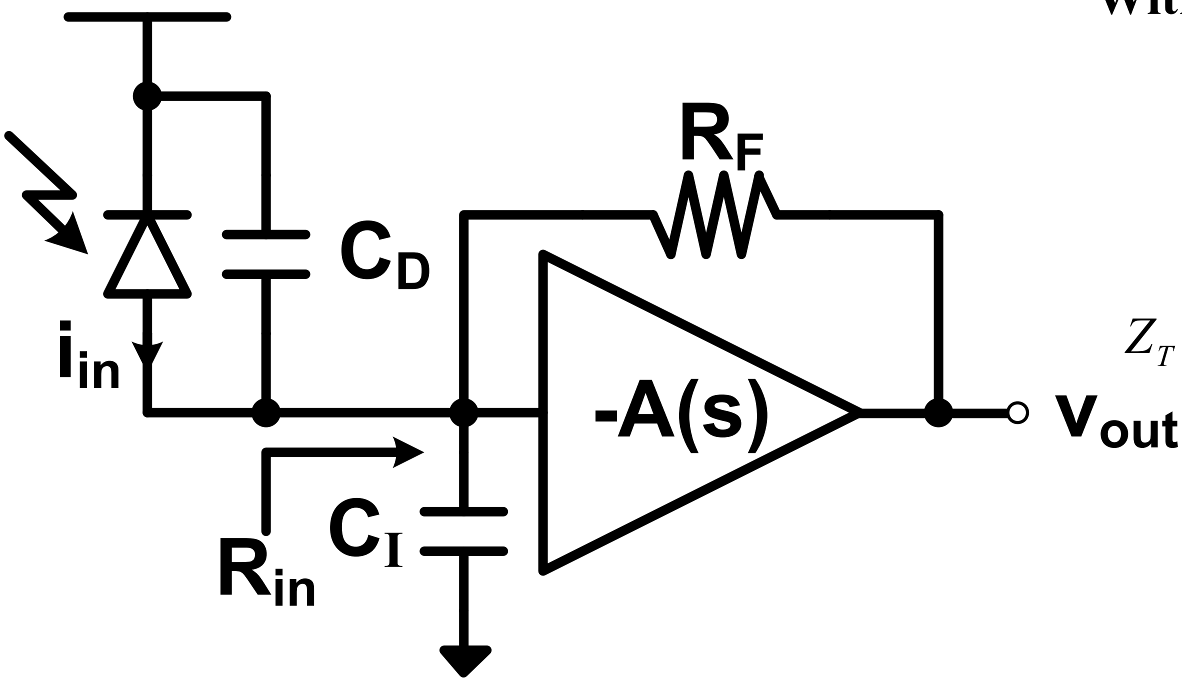
$$R_{in} = \frac{R_F}{A+1}$$

$$R_T = \frac{A}{A+1}R_F$$

$$\omega_p = \frac{1}{R_{in}C_T} = \frac{A+1}{R_F(C_D+C_I)}$$

- Input bandwidth is extended by the factor A+1
- Transimpedance is approximately R_F
- Can make R_F large without worrying about voltage headroom considerations

Feedback TIA w/ Finite Bandwidth Amplifier



With Finite Bandwidth Amplifier :

$$A(s) = \frac{A}{1+\frac{s}{\omega_A}} = \frac{A}{1+sT_A}$$

$$Z_T(s) = -R_T\left(\frac{1}{1+s/(\omega_o Q)+s^2/\omega_o^2}\right)$$

$$R_T = \frac{A}{A+1}R_F$$

$$\omega_o = \sqrt{\frac{A+1}{R_F C_T T_A}}$$

$$Q = \frac{\sqrt{(A+1)R_F C_T T_A}}{R_F C_T + T_A}$$

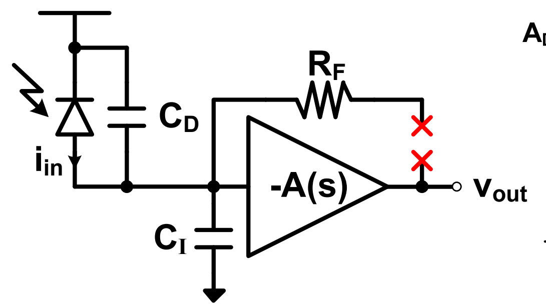
$$R_{in} = \frac{R_F}{A+1}$$

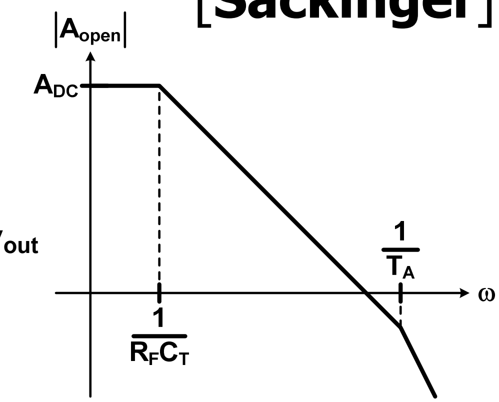
- Finite bandwidth amplifier modifies the transimpedance transfer function to a second-order low-pass function

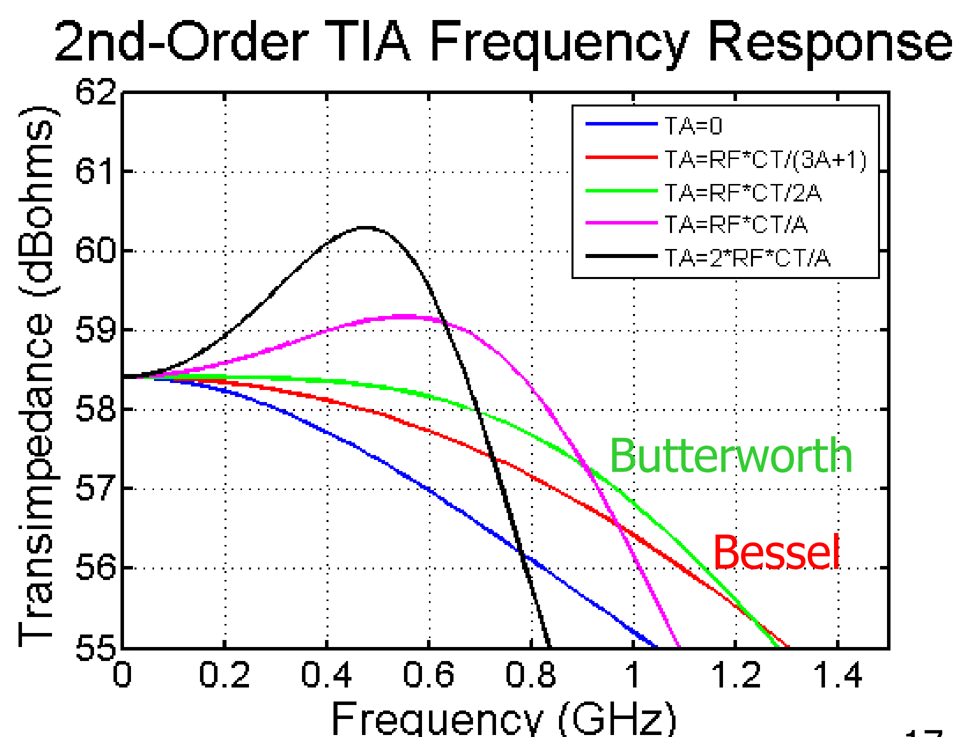
Feedback TIA w/ Finite Bandwidth Amplifier

- Non-zero amplifier time constant can actually increase TIA bandwidth!!
- However, can result in peaking in frequency domain and overshoot/ringing in time domain
- Often either a Butterworth (Q=1/sqrt(2)) or Bessel response (Q=1/sqrt(3)) is used
  - Butterworth gives maximally flat frequency response
  - Bessel gives maximally flat group-delay

[**Sackinger**]







Feedback TIA Transimpedance Limit

If we assume a Butterworth response for mazimally flat frequency response:

$$Q = \frac{1}{\sqrt{2}} \qquad \Rightarrow \qquad \omega_A = \frac{1}{T_A} = \frac{2A}{R_F C_T}$$

For a Butterworth response:

$$\omega_{3\text{dB}} = \omega_0 = \sqrt{\frac{(A+1)\omega_A}{R_F C_T}} = \frac{\sqrt{(A+1)2A}}{R_F C_T} \approx \sqrt{2} \text{ times larger than } T_A = 0 \text{ case of } \frac{A+1}{R_F C_T}$$

Plugging $R_T = \frac{A}{A+1} R_F$ into above expression yields the maximum possible R_T for a given bandwidth

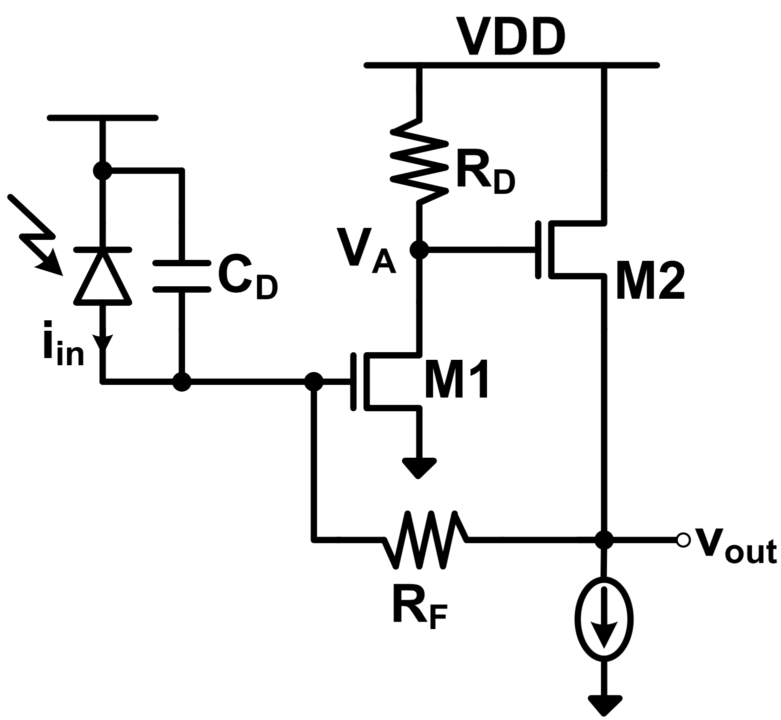
$$\sqrt{\frac{(A+1)\omega_A}{\left(\frac{A+1}{A}\right) R_T C_T}} \geq \omega_{3\text{dB}}$$

$$\boxed{\textbf{Maximum } R_T \leq \frac{A\omega_A}{C_T \omega_{3dB}^2}}$$

[**Mohan JSSC 2000**]

- Maximum R_T proportional to amp gain-bandwidth product
- If amp GBW is limited by technology f_T, then in order to increase bandwidth, R_T must decrease quadratically!

Feedback TIA



Assuming that the source follower has an ideal gain of 1

$$A = g_{m1} R_D$$

$$R_T = \frac{g_{m1} R_D}{1 + g_{m1} R_D} R_F$$

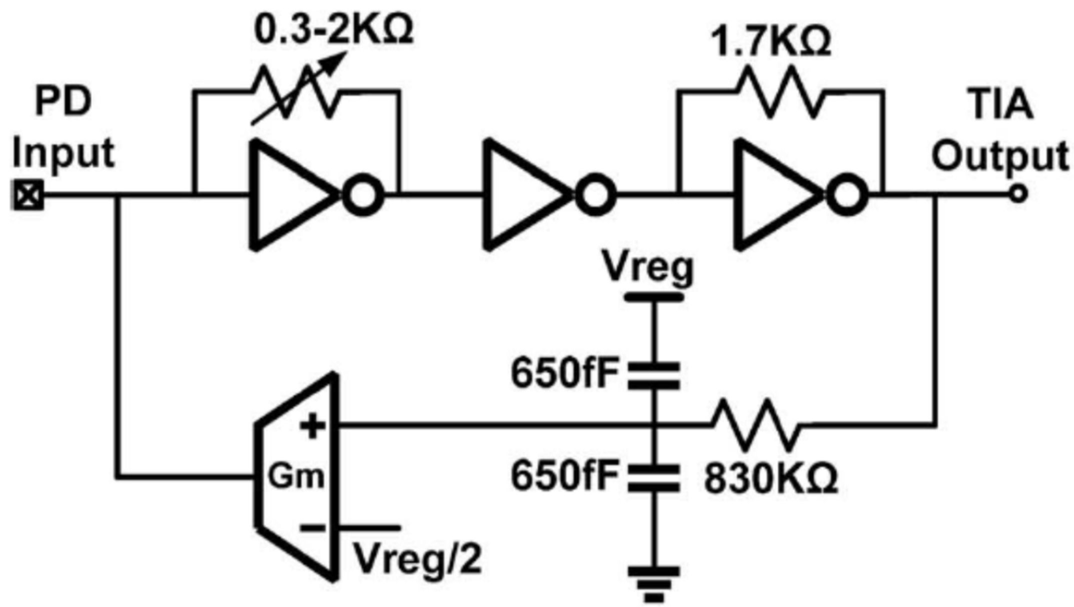
$$R_{in} = \frac{R_F}{1 + g_{m1} R_D}$$

$$R_{out} = \frac{1}{g_{m2}\left(1 + g_{m1} R_D\right)}$$

- As power supply voltages drop, there is not much headroom left for RD and the amplifier gain degrades

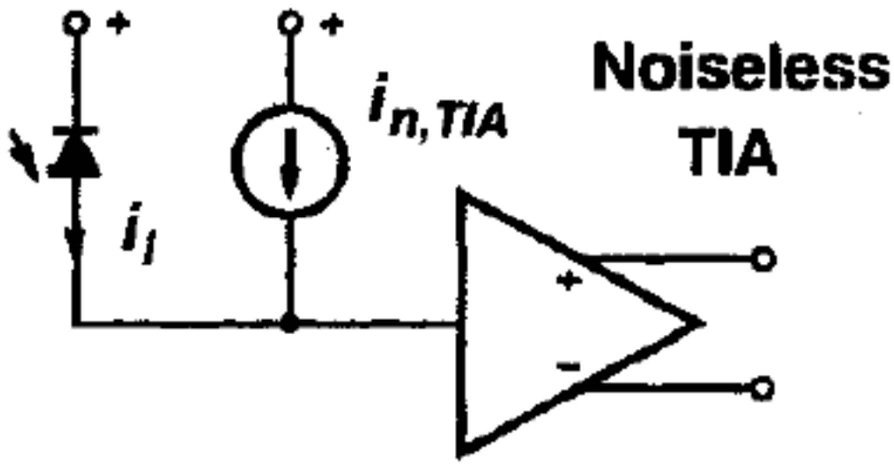
CMOS Inverter-Based Feedback TIA

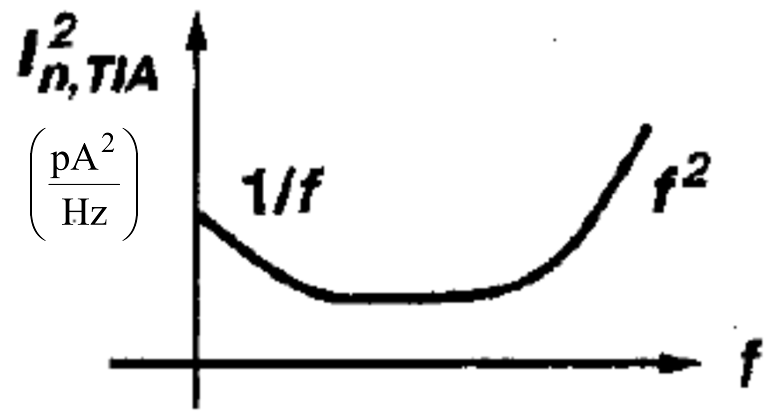
[**Li JSSC 2014**]



- CMOS inverter-based TIAs allow for reduced voltage headroom operation
- Cascaded inverter-gm + TIA stage provide additional voltage gain
- Low-bandwidth feedback loop sets the amplifier output common-mode level

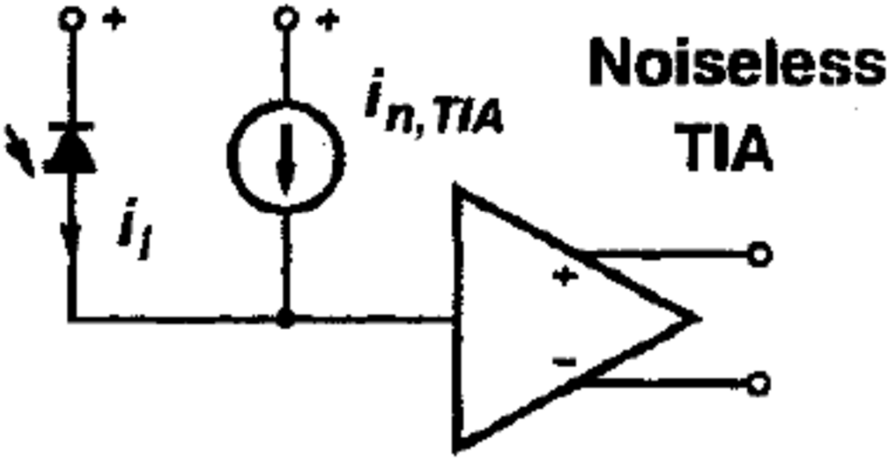
Input-Referred Noise Current

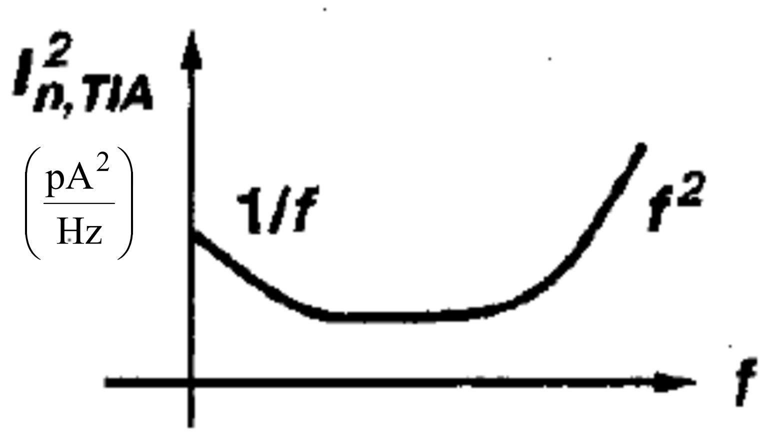




- TIA noise is modeled with an input-referred noise current source that reproduces the output TIA output noise when passed through an ideal noiseless TIA
- This noise source will depend on the source impedance, which is determined mostly by the photodetector capacitance

Input-Referred Noise Current Spectrum





- Input-referred noise current spectrum typically consists of uniform, high-frequency f², & low-frequency 1/f components
- To compare TIAs, we need to see this noise graph out to ~2X the TIA bandwidth
  - Recall the noise bandwidth tables

Input-Referred RMS Noise Current

- The input-referred rms noise current can be calculated by dividing the rms output noise voltage by the TIA's midband transimpedance value

$$i_{n,TIA}^{rms} = \frac{1}{R_T}\sqrt{\int_0^{>2BW} \left|Z_T(f)\right|^2 I_{n,TIA}^2(f)\,df}$$

- If we integrate the output noise, the upper bound isn't too critical. Often this is infinity for derivations, or 2X the TIA bandwidth in simulation
- This rms current sets the TIA's electrical sensitivity

$$i_{sens}^{pp} = 2Q i_{n,TIA}^{rms}$$

- To determine the total optical receiver sensitivity, we need to consider the detector noise and responsivity

Averaged Input-Referred Noise Current Density

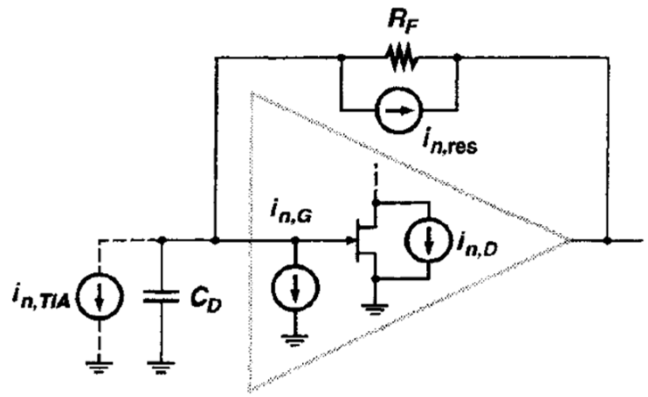
- TIA noise performance can also be quantified by the averaged input-referred noise current density

$$i_{n,TIA}^{avg} = \frac{i_{n,TIA}^{rms}}{\sqrt{BW_{3dB}}}$$

This quantity has units of $\left(\frac{\text{pA}}{\sqrt{\text{Hz}}}\right)$.

Note, this is different than averaging the input - referred noise spectrum, $I_{n,TIA}^2(f)$ over the TIA bandwidth.

FET Feedback TIA Input-Referred Noise Current Spectrum



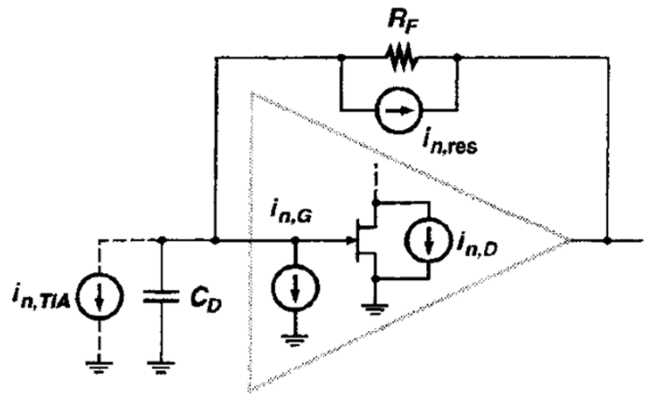
- The feedback resistor and amplifier front-end noise components determine the input-referred noise current spectrum

$$I^2_{n,TIA}(f) = I^2_{n,res}(f) + I^2_{n,front}(f)$$

- The feedback resistor component is uniform with frequency

$$I^2_{n,res}(f) = \frac{4kT}{R_F}$$

FET Feedback TIA Input-Referred Noise Current Spectrum



- Gate current-induced shot noise

$$I_{n,G}^2 = 2qI_G$$

This is typically small for CMOS designs

- FET channel noise

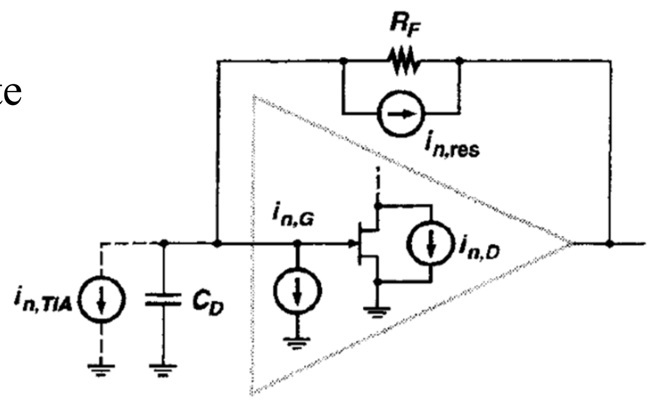
$$I_{n,D}^2 = 4kT\Gamma g_m$$

Γ is the channel noise factor, typically 0.7 - 3 depending on the process.

Input-Referring the FET Channel Noise

To do this, we could calculate $\dfrac{i_{n,TIA}}{i_{n,D}} = \dfrac{\left(\dfrac{v_{out}}{i_{n,D}}\right)}{Z_T}$

But it is easier (and equivalent) to ground the output and calculate



$$\left(\frac{i_{n,D}}{i_{n,TIA}}\right)^{-1}$$

$$i_{n,D} = g_m v_{n,TIA} = \frac{g_m i_{n,TIA}}{sC_T + \dfrac{1}{R_F}} = \frac{g_m R_F}{1 + sR_F C_T} i_{n,TIA}$$

where $C_T = C_D + C_I$, the summation of the detector and amplifier input capacitance.

$$\left(\frac{i_{n,D}}{i_{n,TIA}}\right)^{-1} = \frac{1 + sR_F C_T}{g_m R_F}$$

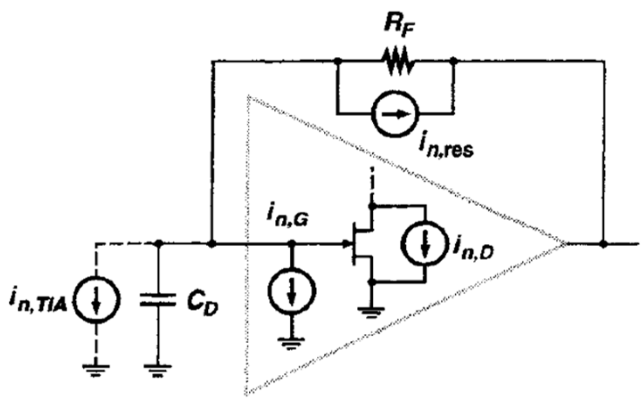
Using this high - pass transfer function, the input - referred FET channel noise is

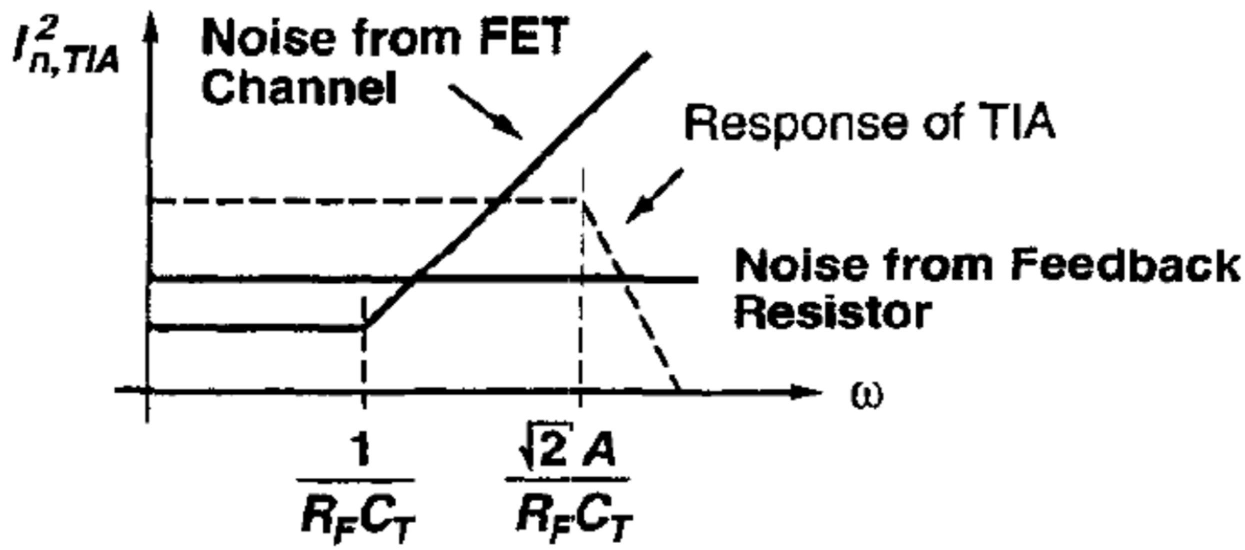
$$I^2_{n,front,D}(f) = \frac{1 + (2\pi f R_F C_T)^2}{(g_m R_F)^2} \cdot 4kT\Gamma g_m$$

$$= 4kT\Gamma\left(\frac{1}{g_m R_F^2}\right) + 4kT\Gamma\left(\frac{(2\pi C_T)^2}{g_m}\right) f^2$$

Uniform and f^2 component!

Total Input-Referred FET Feedback TIA Noise





$$I^2_{n,TIA}(f) = \frac{4kT}{R_F} + 2qI_G + 4kT\Gamma\left(\frac{1}{g_m R_F^2}\right) + 4kT\Gamma\left(\frac{(2\pi C_T)^2}{g_m}\right) f^2$$

Feedback Resistor Gate Shot Noise FET Channel Noise

- Note that the TIA input-referred noise current spectrum begins to rise at a frequency lower than the TIA bandwidth

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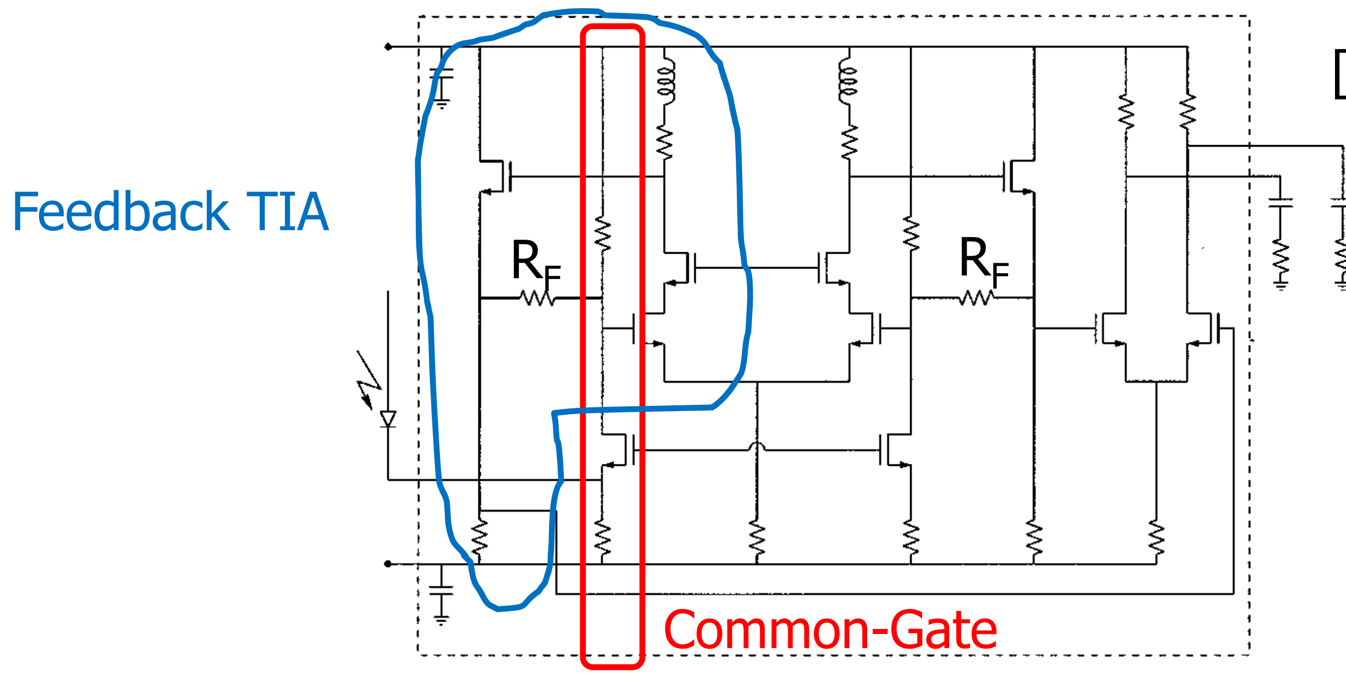
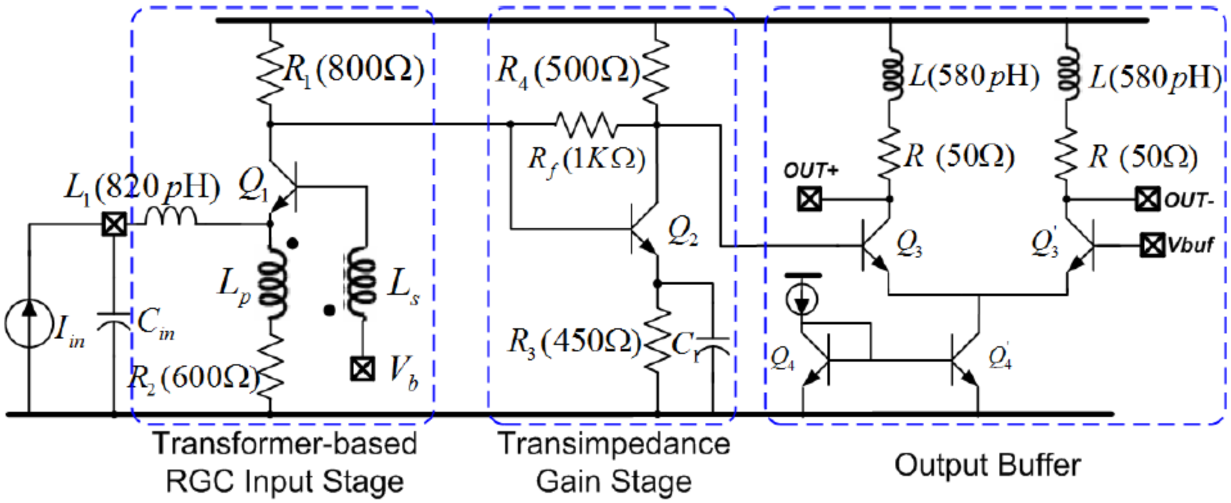
Common-Gate & Feedback TIA

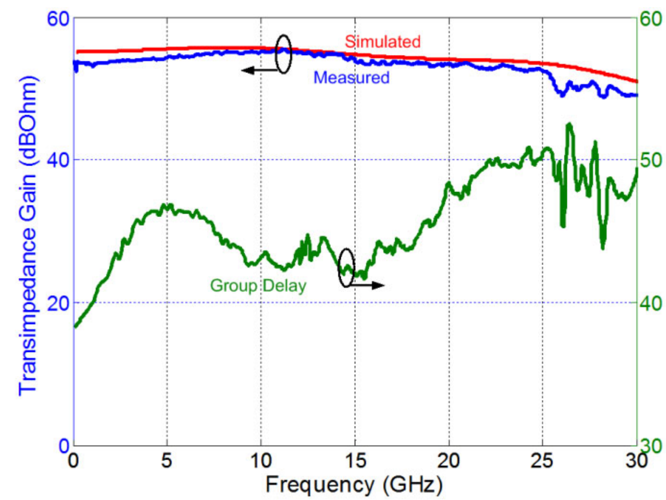


[Mohan JSSC 2000]

- Recall that the feedback TIA stability depends on the ratio of the input pole (set by C_D) and the amplifier pole
  - Large variation in C_D can degrade amplifier stability
- Common-gate input stage isolates C_D from input amplifier capacitance, allowing for a stable response with a variety of different photodetectors
- Transimpedance is still approximately $R_F A/(1+A)$

BJT Common-Base & Feedback TIA





- Transformer-based negative feedback boosts gm with low power and noise overhead
- Input series peaking inductor isolates the photodetector capacitance from the TIA input capacitance
- High frequency techniques allow for 26GHz bandwidth with group delay variation less than 19ps

[**Li JSSC 2013**]

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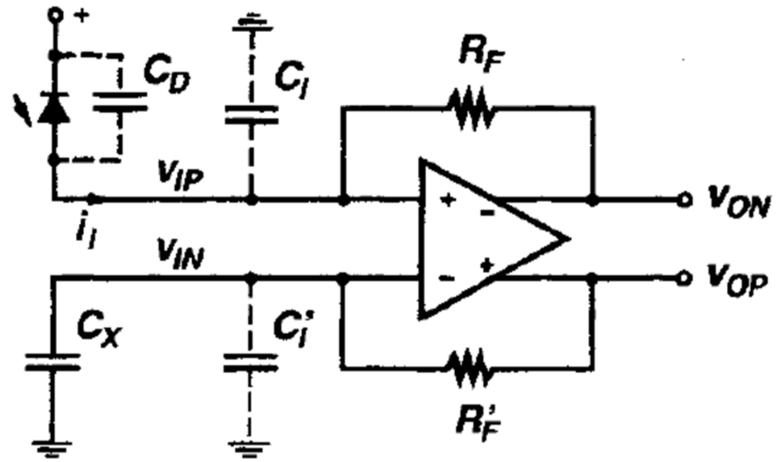
Differential TIAs

- Differential circuits have superior immunity to power supply/substrate noise
- A differential TIA output allows easy use of common differential main/limiting amplifiers
  - This comes at the cost of higher noise and power
- How to get a differential output with a single-ended photocurrent input?
  - Two common approaches, based on the amount of capacitance applied at the negative input

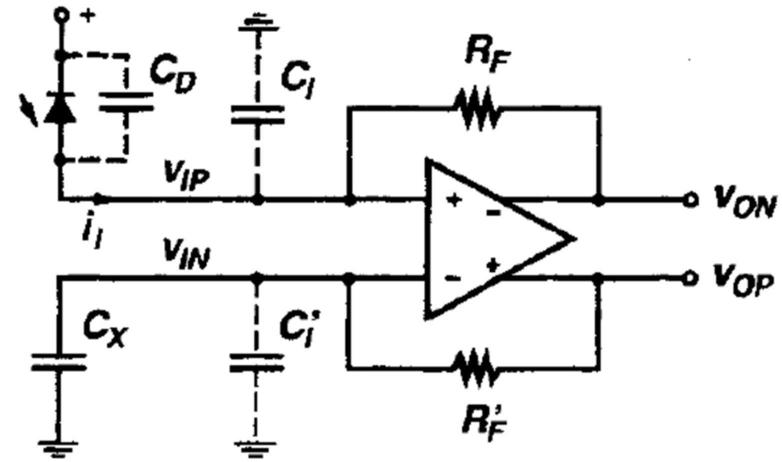


Balanced TIA

- A balanced TIA design attempts to match the capacitance of the two differential inputs

$$C_X \approx C_D$$

- This provides the best power supply/substrate noise immunity, as the noise transfer functions are similar
- Due to double the circuitry, the input-referred rms noise current is increased by sqrt(2)



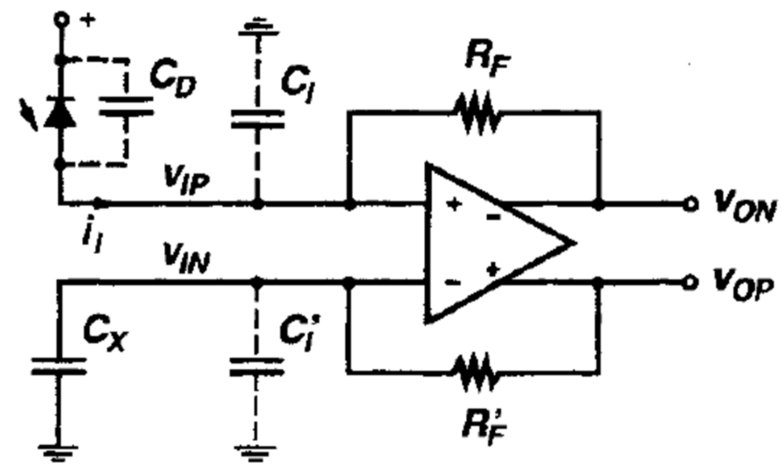
Assuming an high BW amplifier and $C_T = C_D + C_I$

$$Z_T(s) = \frac{v_{OP} - v_{ON}}{i_i} = \frac{\left(\frac{A}{A+1}\right) R_F}{1 + \frac{s C_T R_F}{A+1}}$$

Same transfer function as the single - ended design

Pseudo-Differential TIA

- A pseudo-differential TIA design uses a very large capacitor at the negative input, such that it can be approximated as an AC ground $C_X \to \infty$



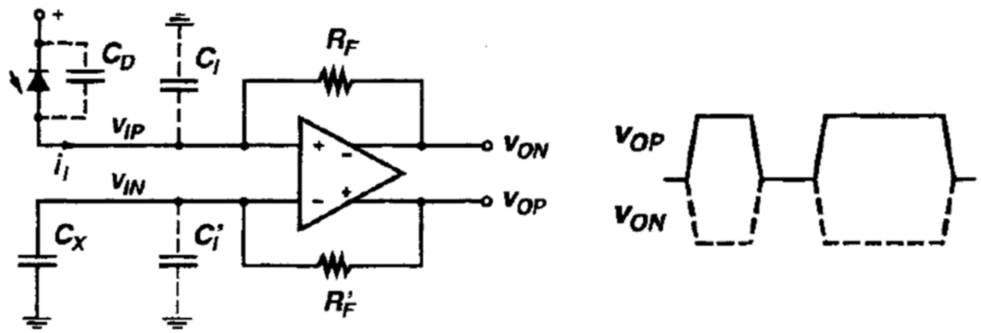
Assuming an high BW amplifier and $C_T = C_D + C_I$

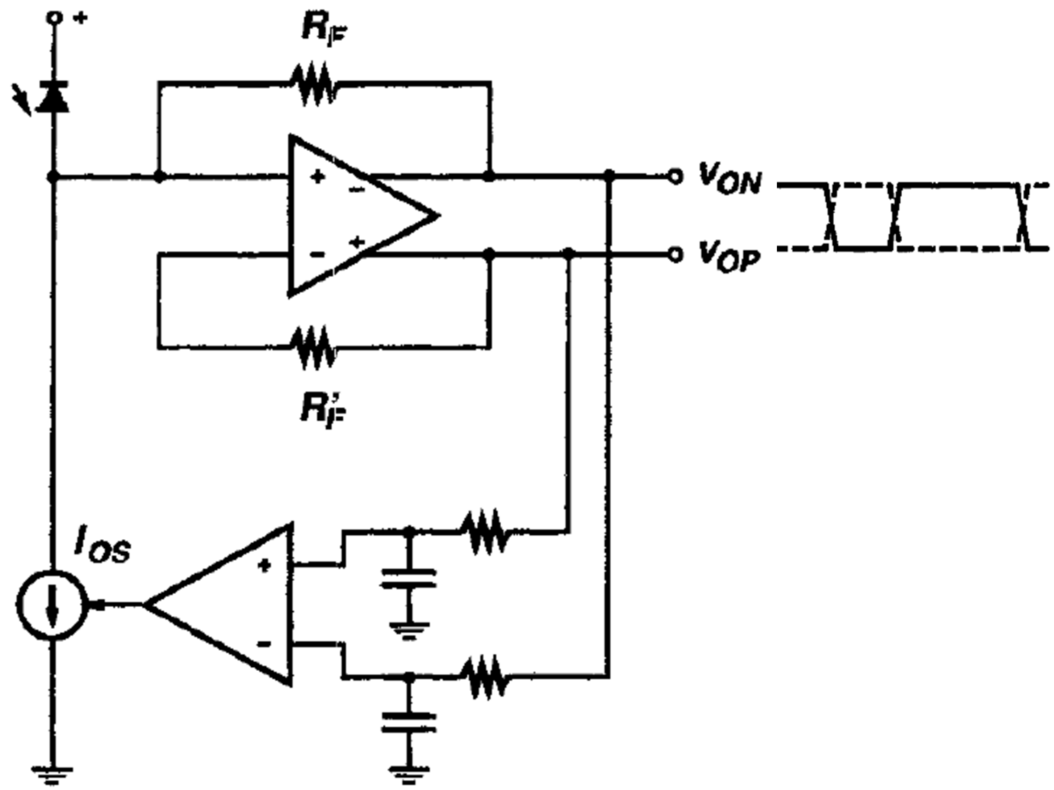
- While not good to reject power supply/substrate noise, it does provide significant filtering of the R_F' noise
- The differential transimpedance is approximately doubled relative to the single-ended case

$$Z_T(s) = \frac{v_{OP} - v_{ON}}{i_i} = \frac{\left(\frac{2A}{A+2}\right) R_F}{1 + \frac{s C_T R_F}{\frac{A}{2} + 1}}$$

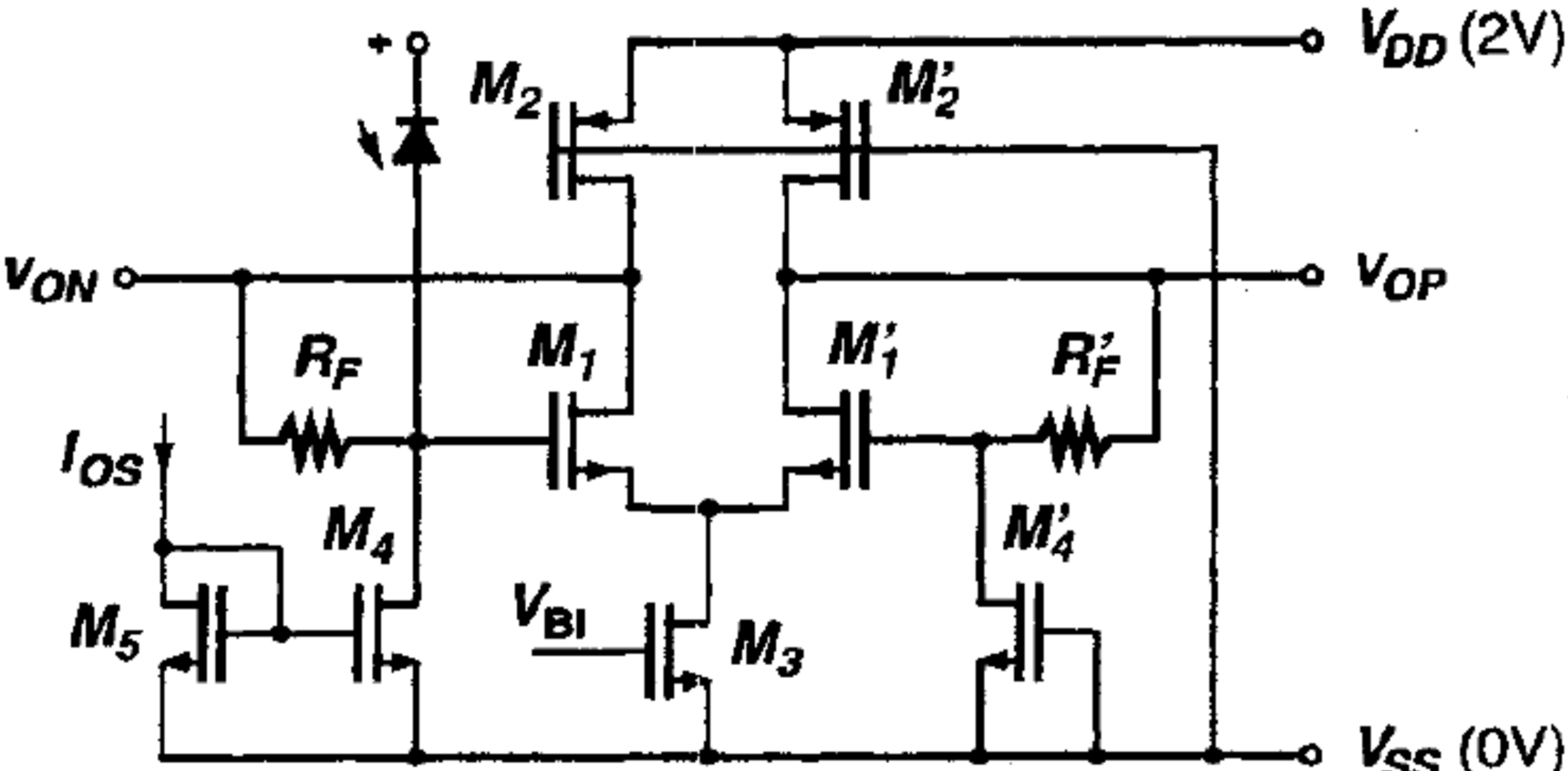
Offset Control

- Due to the single-ended photodetector signal, the differential output signal swings from 0 to V_{ppd}, which can limit the dynamic range
- Adding offset control circuitry can allow for an output swing of $\pm V_{ppd}/2$





Differential Shunt Feedback TIA



Agenda

- Optical Receiver Overview
- Transimpedance Amplifiers
  - Common-Gate TIAs
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Optical RX Scaling Issues

- ☺ Traditionally, TIA has high R_T and low R_{in}

$$R_T = R_F\left(\frac{A}{1+A}\right)$$

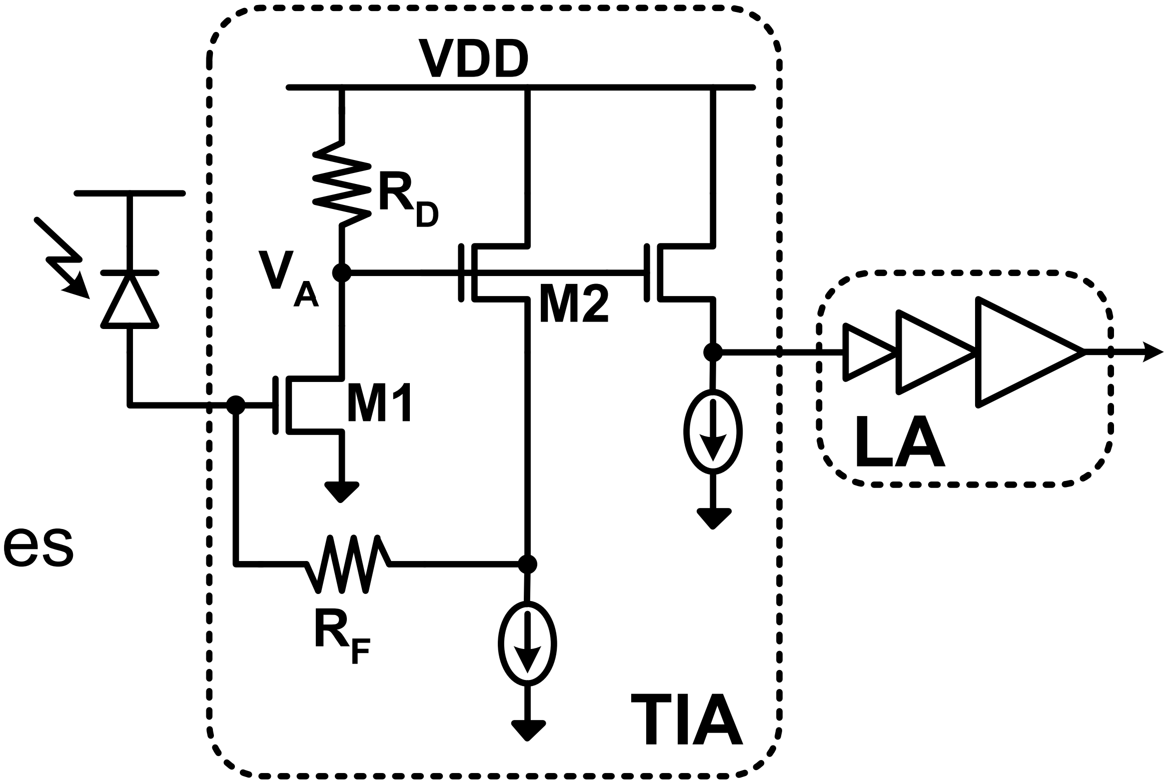
$$\omega_{3dB} \approx \frac{1+A}{R_F C_{IN}}$$

- ☹ Headrooom/Gain issues in 1V CMOS
  - $A \approx 2-3$

- ☹ Power/Area Costs

$$\text{TIA} \;\; I_D \propto \left(R_T C_{IN}\right)^2 f_{3dB}^4$$

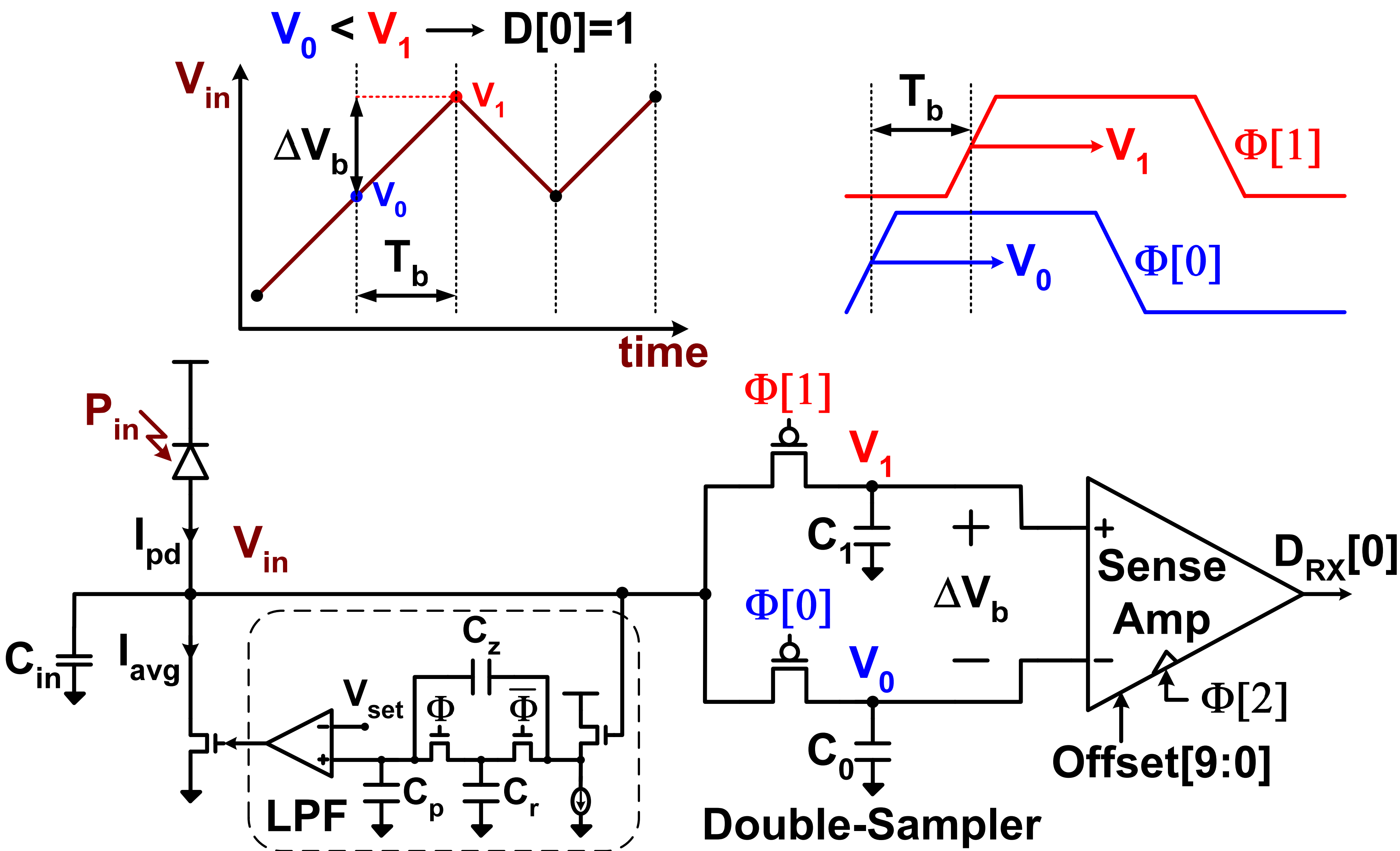
$$\text{LA} \;\; I_D \propto f_{3dB}^2$$



$$V_A = V_{GS1} + V_{GS2} \approx 0.8 * VDD$$

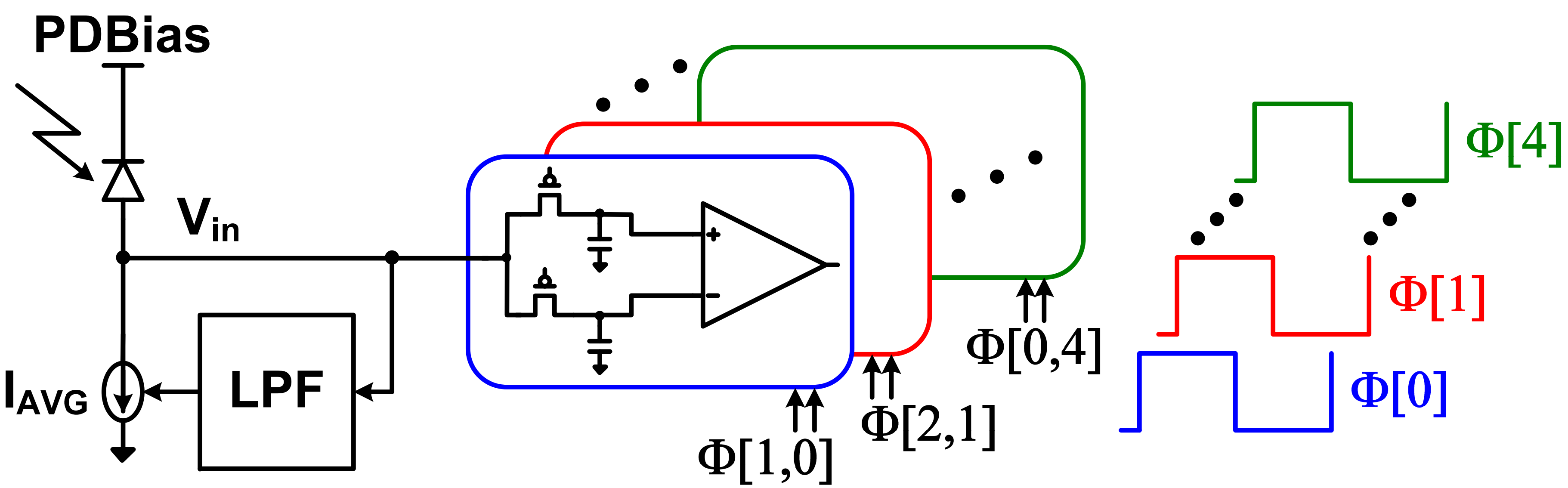
$$A \approx g_{m1} R_D = \frac{\alpha\left(VDD - V_A\right)}{VOD} \approx \frac{\alpha\left(0.2 * VDD\right)}{VOD}$$

Integrating Receiver Block Diagram



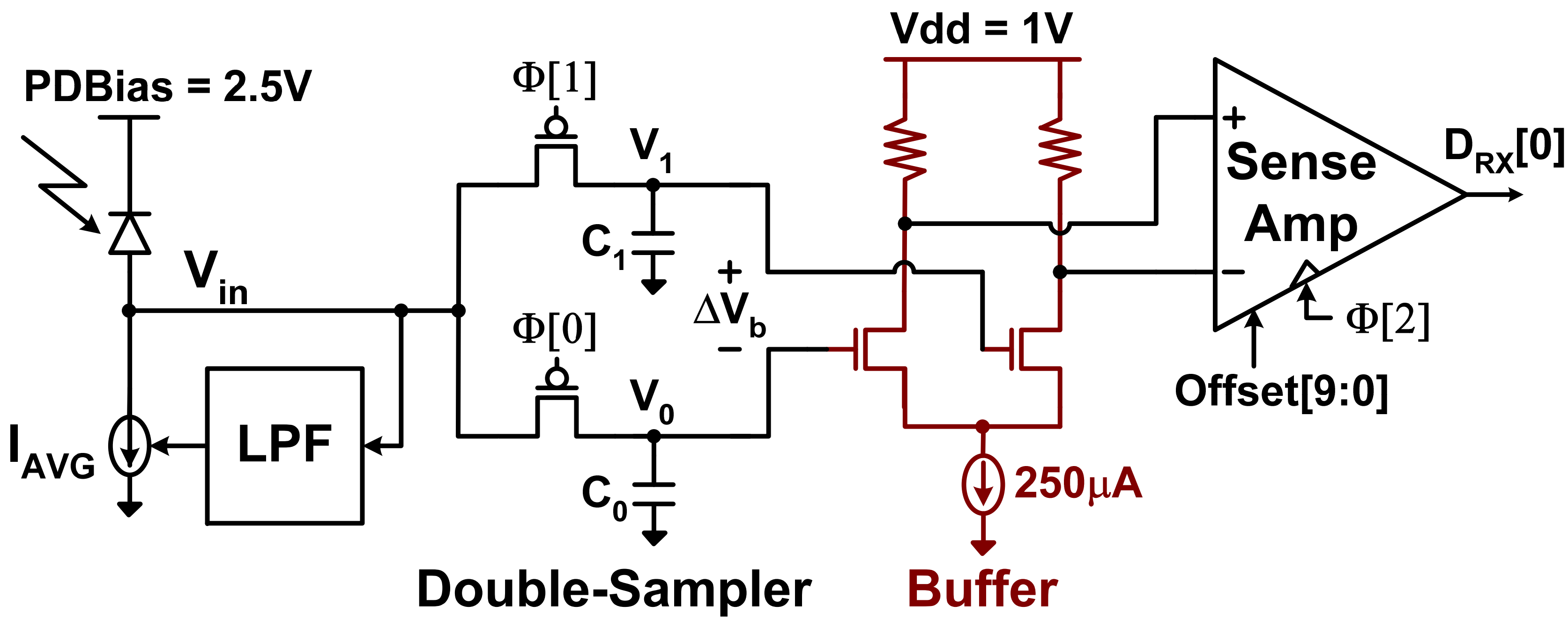
[Emami VLSI 2002]

Demultiplexing Receiver



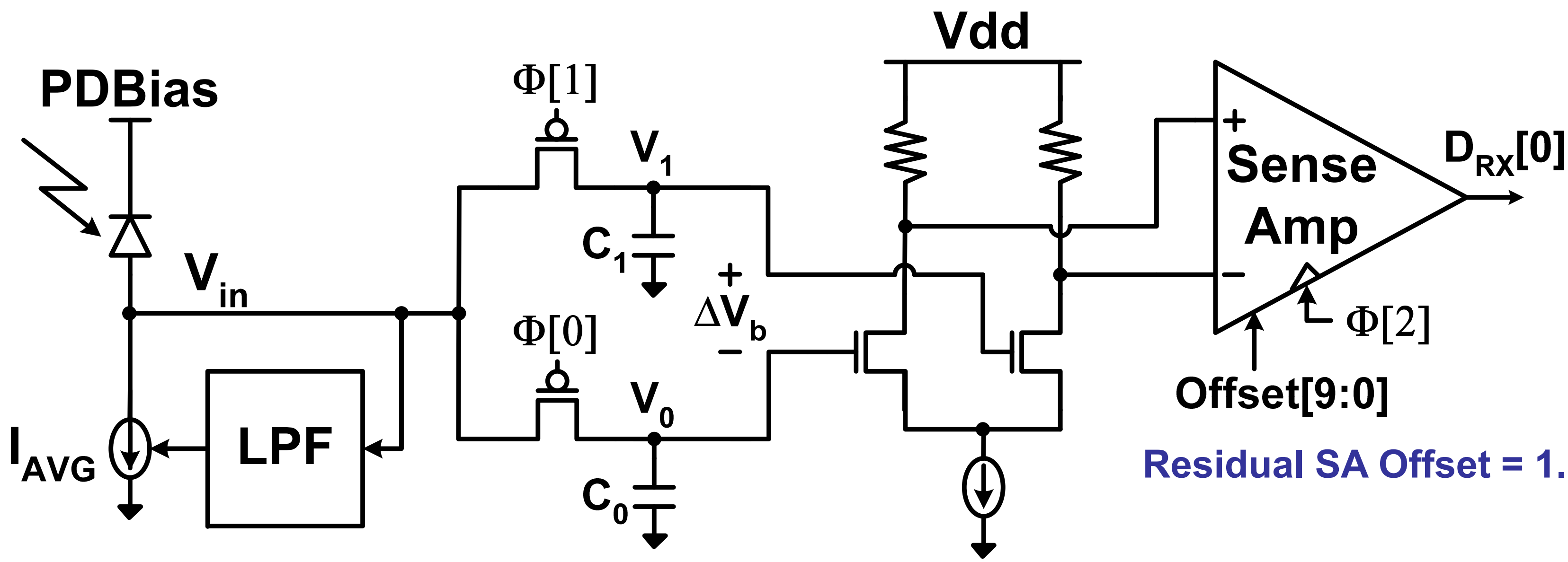
- Demultiplexing with multiple clock phases allows higher data rate
  - Data Rate = #Clock Phases x Clock Frequency
  - Gives sense-amp time to resolve data
  - Allows continuous data resolution

1V Modified Integrating Receiver



- Differential Buffer
  - ☺ Fixes sense-amp common-mode input for improved speed and offset performance
  - ☺ Reduces kickback charge
  - ☹ Cost of extra power and noise
- Input Range = 0.6 – 1.1V

Receiver Sensitivity Analysis



Residual SA Offset = 1.15mV

Max $\Delta V_{in}(\Delta I_{AVG})$ = 0.6mV

$$\sigma_{samp} = \sqrt{\frac{2kT}{C_{samp}}} = 0.92mV \qquad \sigma_{buffer} = 1.03mV \qquad \sigma_{SA} = 0.45mV$$

$$P_{avg} = \frac{\Delta V_b \left(C_{pd} + C_{in}\right)}{\rho T_b}$$

Clock Jitter Noise $\sigma_{clk} = \left(\dfrac{\sigma_j}{T_b}\right)\Delta v_b \approx 0.65mV$ **at 16Gb/s**

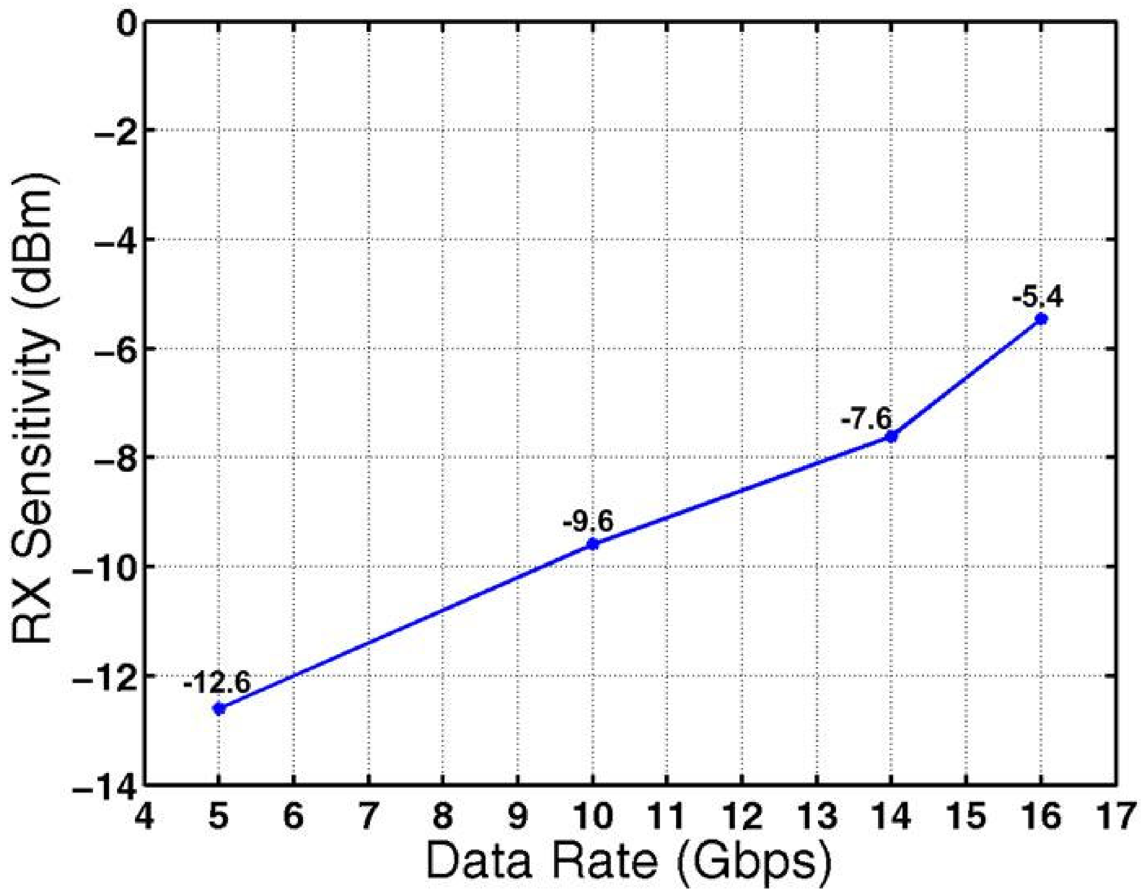
Total Input Noise $\sigma_{tot} = \sqrt{\sigma_{samp}^2 + \sigma_{buffer}^2 + \sigma_{SA}^2 + \sigma_{clk}^2} = 1.59mV$

ΔV_b for BER = 10^{-10} = $6.4\sigma_{tot}$ + Offset = 11.9mV

Gb/s	P_{avg} (dBm)
10	-9.8
16	-7.8

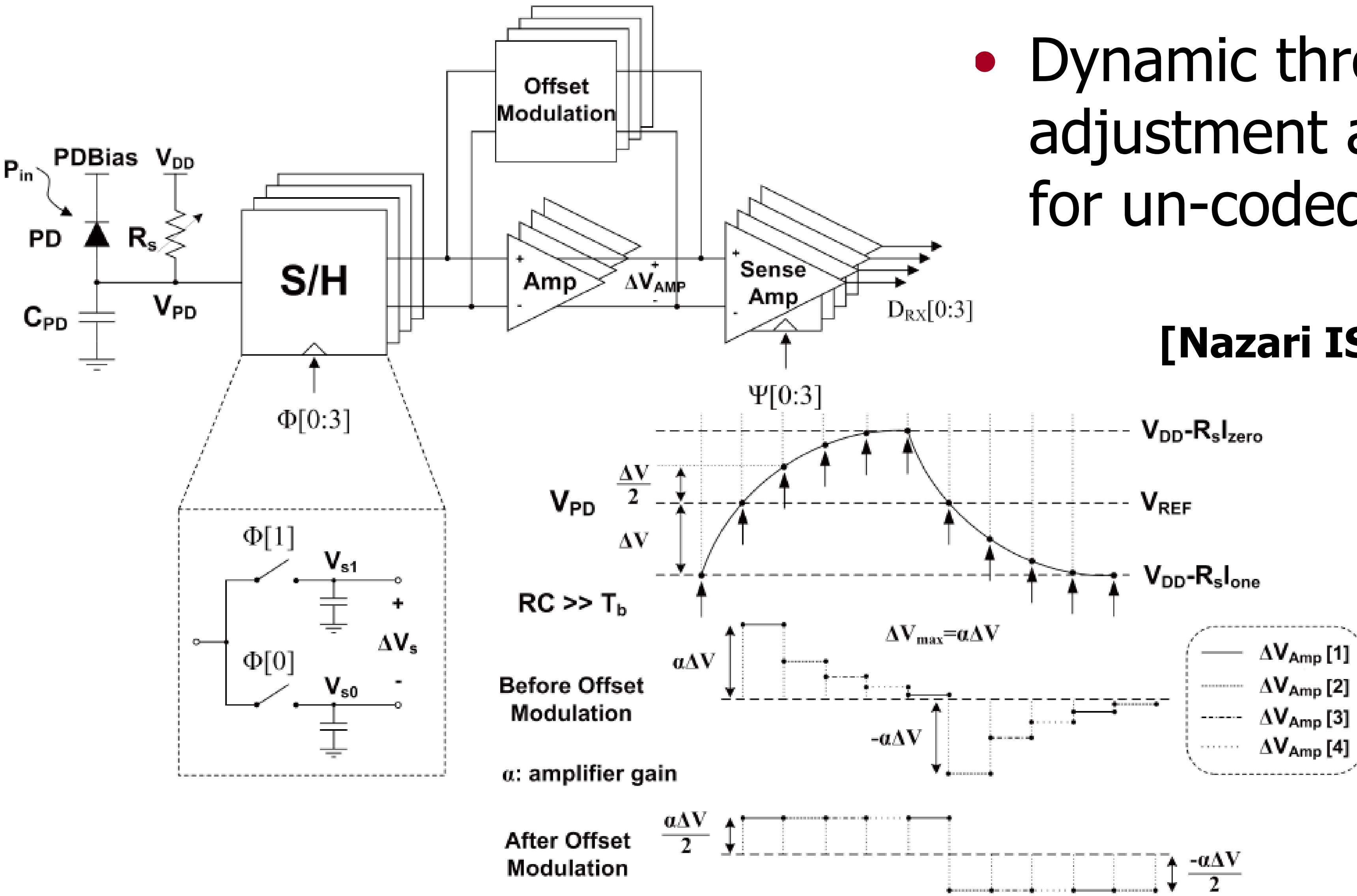
Integrating Receiver Sensitivity

- Test Conditions
  - 8B/10B data patterns (variance of 6 bits)
  - Long runlength data (variance of 10 bits)
- BER < 10^{-10}



[Palermo JSSC 2008]

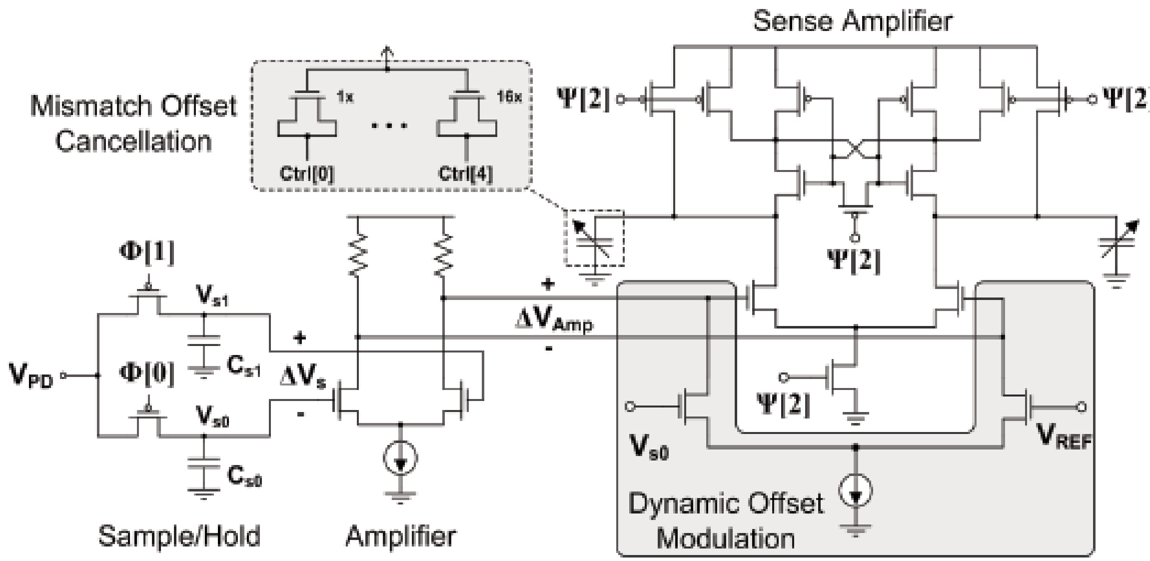
Integrating RX with Dynamic Threshold

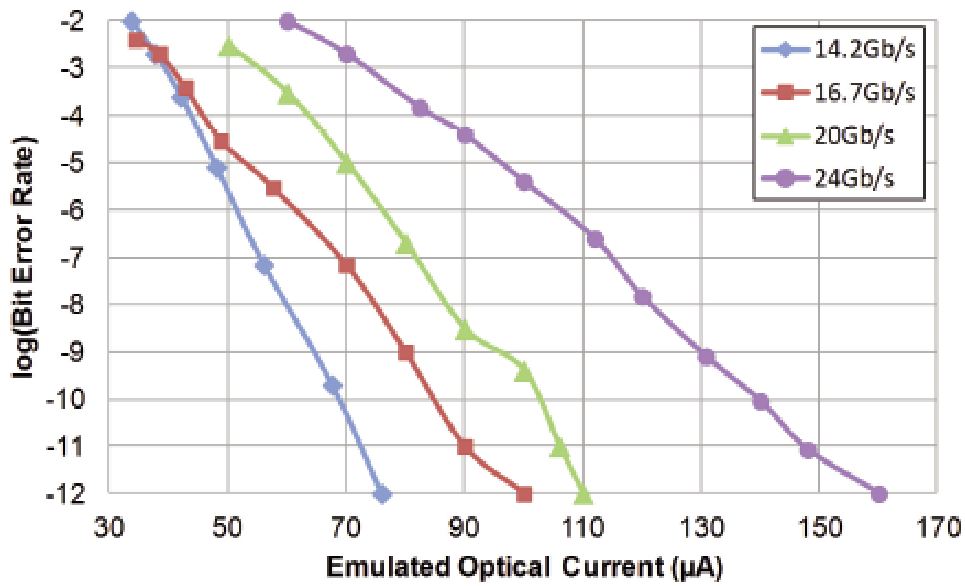


- Dynamic threshold adjustment allows for un-coded data

[Nazari ISSCC 2012]

Integrating RX with Dynamic Threshold





[Nazari ISSCC 2012]

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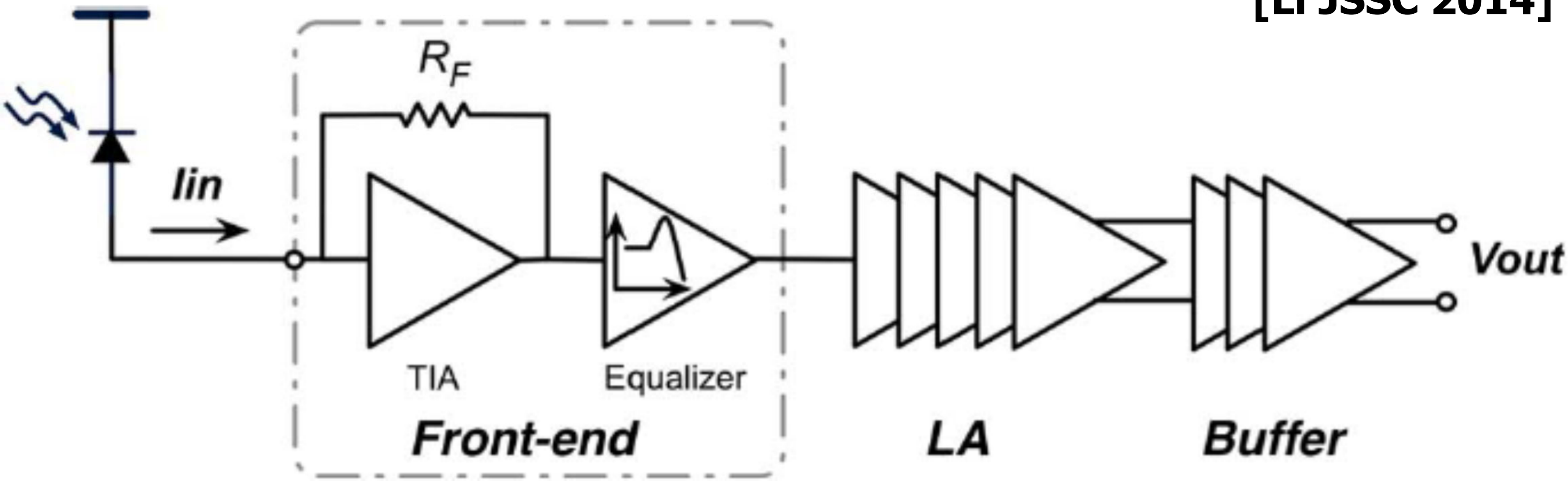
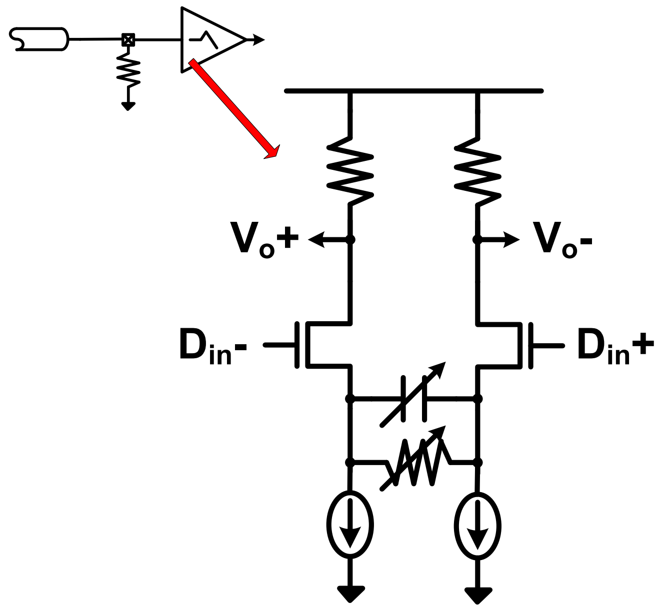
Low-BW TIA & CTLE Front-End

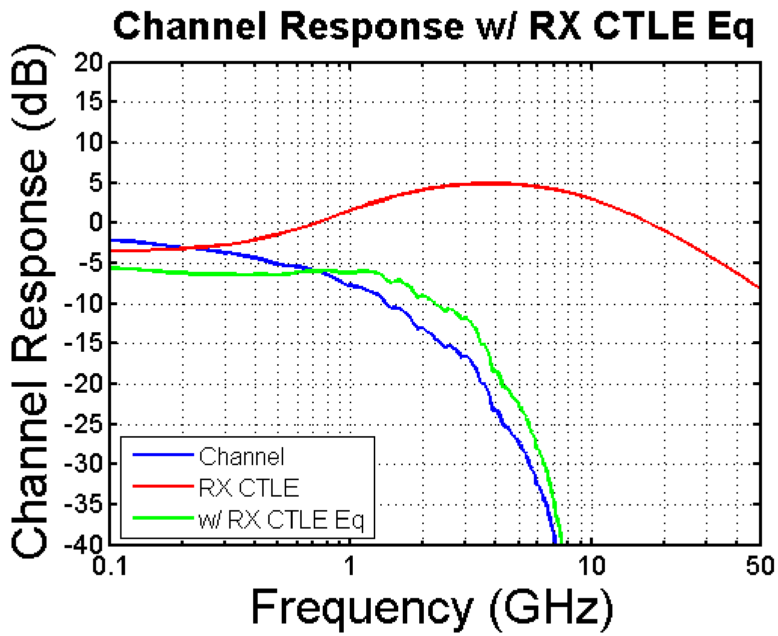
[Li JSSC 2014]

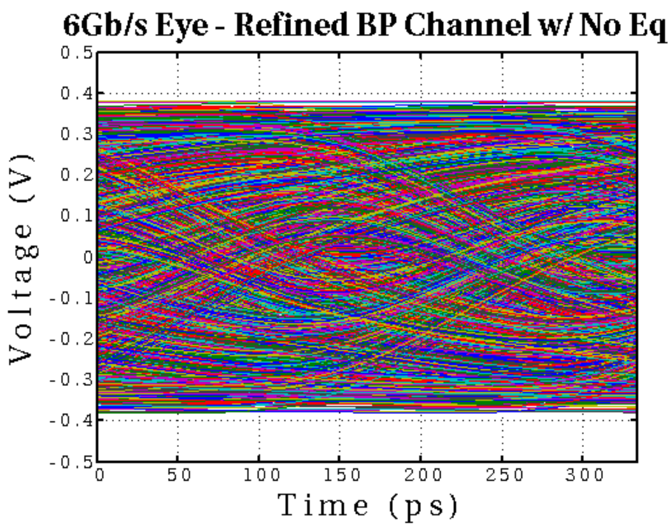


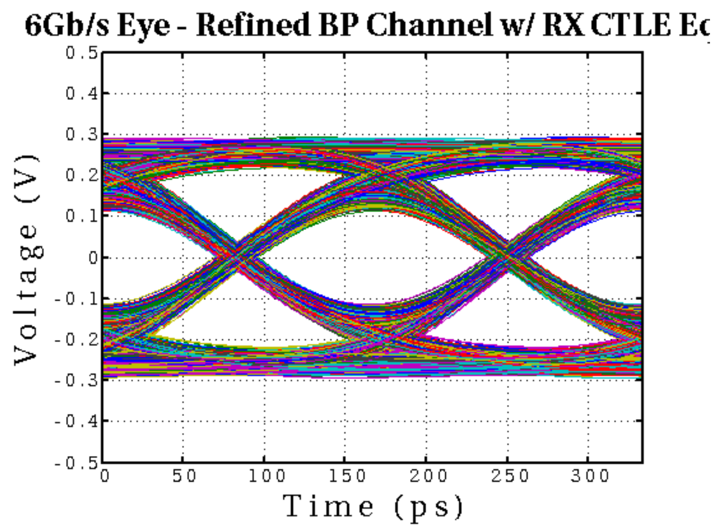
- Improved sensitivity is possible by increasing the first stage feedback resistor, resulting in a high-gain low-bandwidth TIA
- The resultant ISI is cancelled by a subsequent CTLE

Active CTLE Example

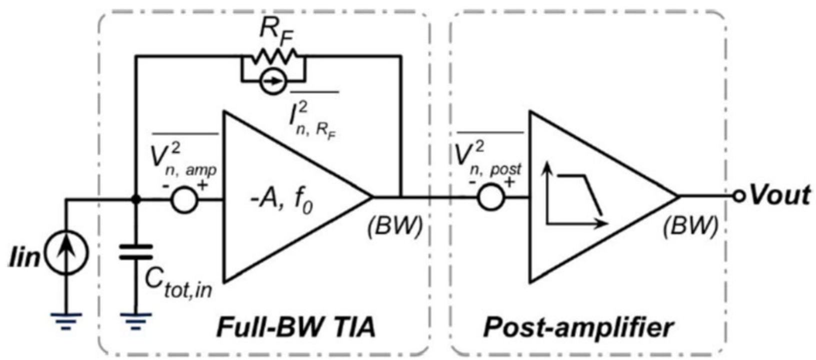


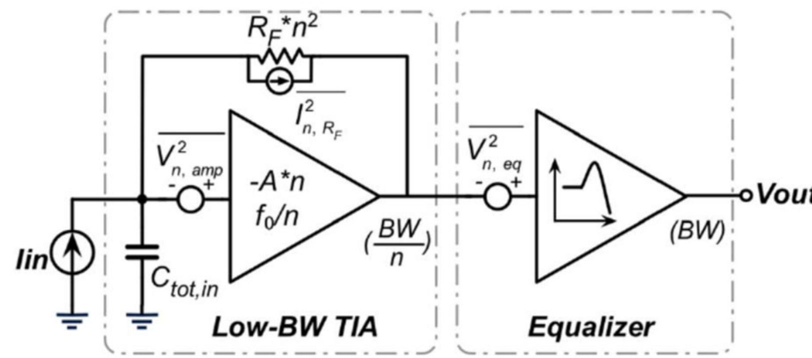






Low-BW TIA & CTLE Front-End

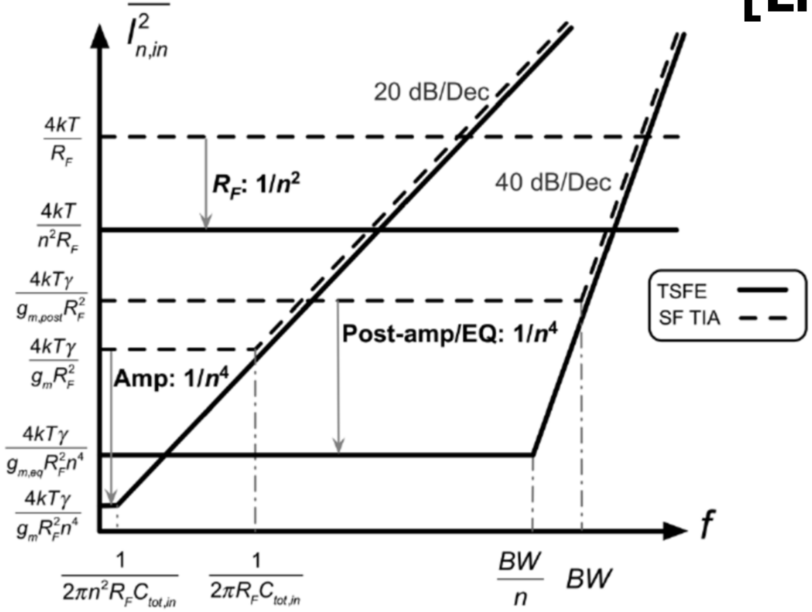




$$\overline{I^2_{n,\mathrm{in,SF}}}(f) = \frac{4kT}{R_F} + \frac{4kT\gamma}{g_m R_F^2} + 4kT\gamma\frac{(2\pi C_{\mathrm{tot,in}})^2}{g_m} f^2 + \frac{4kT\gamma}{g_{m,\mathrm{post}} R_F^2} + \frac{4kT\gamma}{g_{m,\mathrm{post}} R_F^2}\left(\frac{f}{BW}\right)^4$$

$$\begin{aligned}\overline{I^2_{n,\mathrm{in,TSFE}}}(f) &= \frac{4kT}{R_F n^2} + \frac{4kT\gamma}{g_m R_F^2 n^4} + 4kT\gamma\frac{(2\pi R_F n^2 C_{\mathrm{tot,in}})^2}{g_m R_F^2 n^4} f^2 + \frac{4kT\gamma}{g_{m,\mathrm{eq}} R_F^2 n^4} + \frac{4kT\gamma}{g_{m,\mathrm{eq}} R_F^2 n^4}\left(\frac{f}{BW/n}\right)^4 \\ &= \frac{4kT}{R_F n^2} + \frac{4kT\gamma}{g_m R_F^2 n^4} + 4kT\gamma\frac{(2\pi C_{\mathrm{tot,in}})^2}{g_m} f^2 + \frac{4kT\gamma}{g_{m,\mathrm{eq}} R_F^2 n^4} + \frac{4kT\gamma}{g_{m,\mathrm{eq}} R_F^2}\left(\frac{f}{BW}\right)^4 \qquad (5)\end{aligned}$$

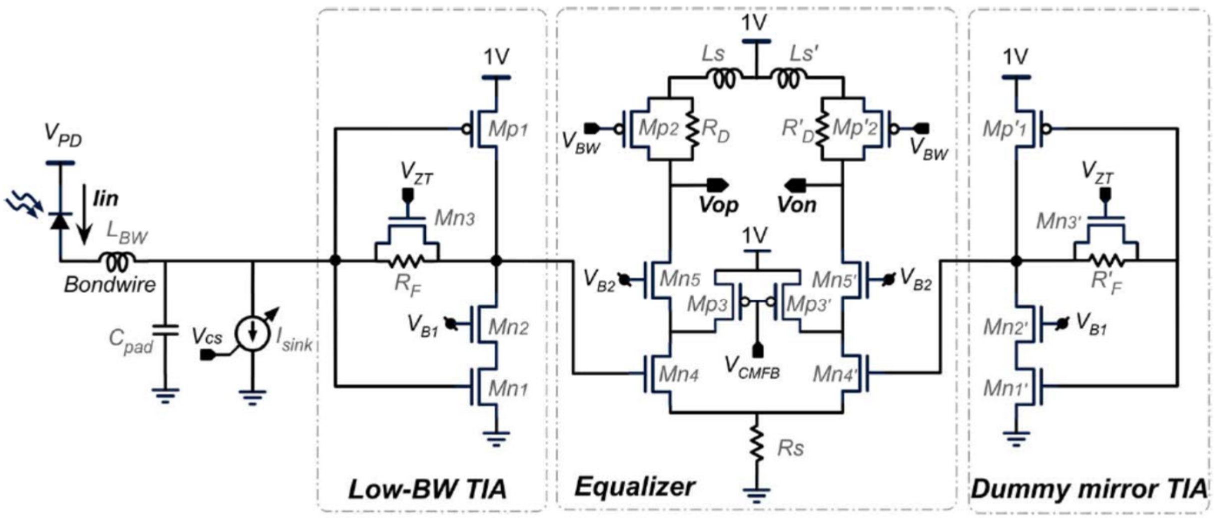
[Li JSSC 2014]

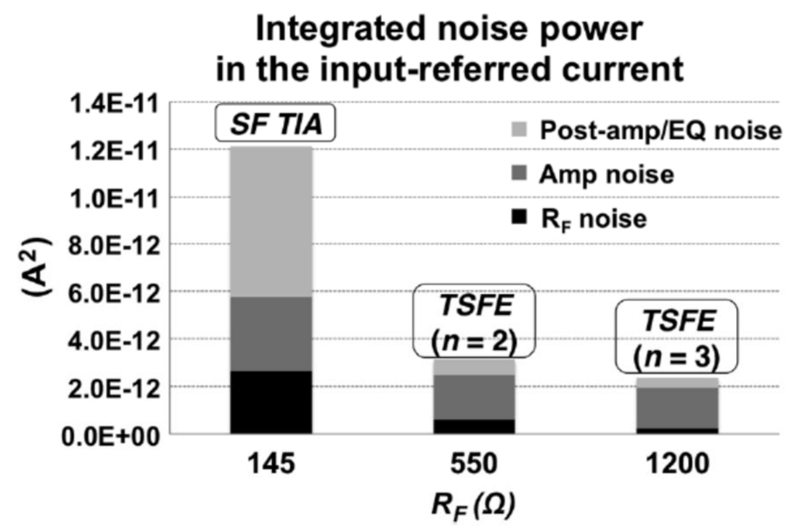


- Significant reduction in feedback resistor noise
- Low-frequency input and post amplifier noise is also reduced

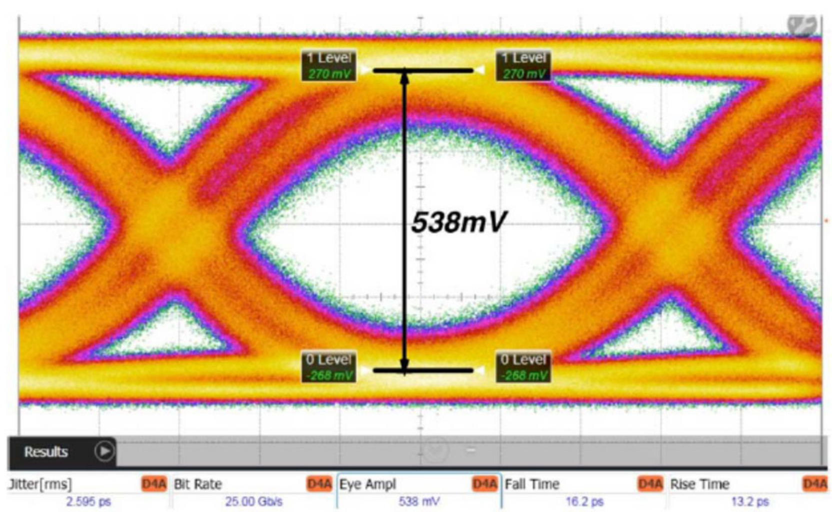
Low-BW TIA & CTLE Front-End

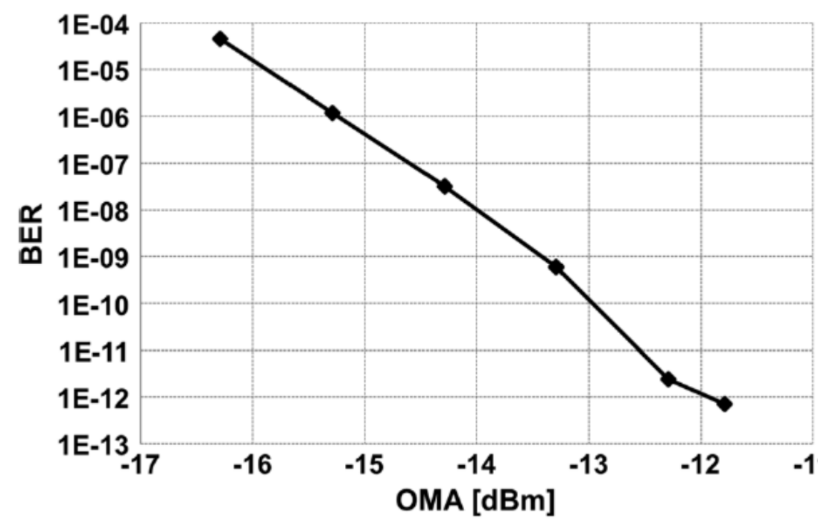
[Li JSSC 2014]





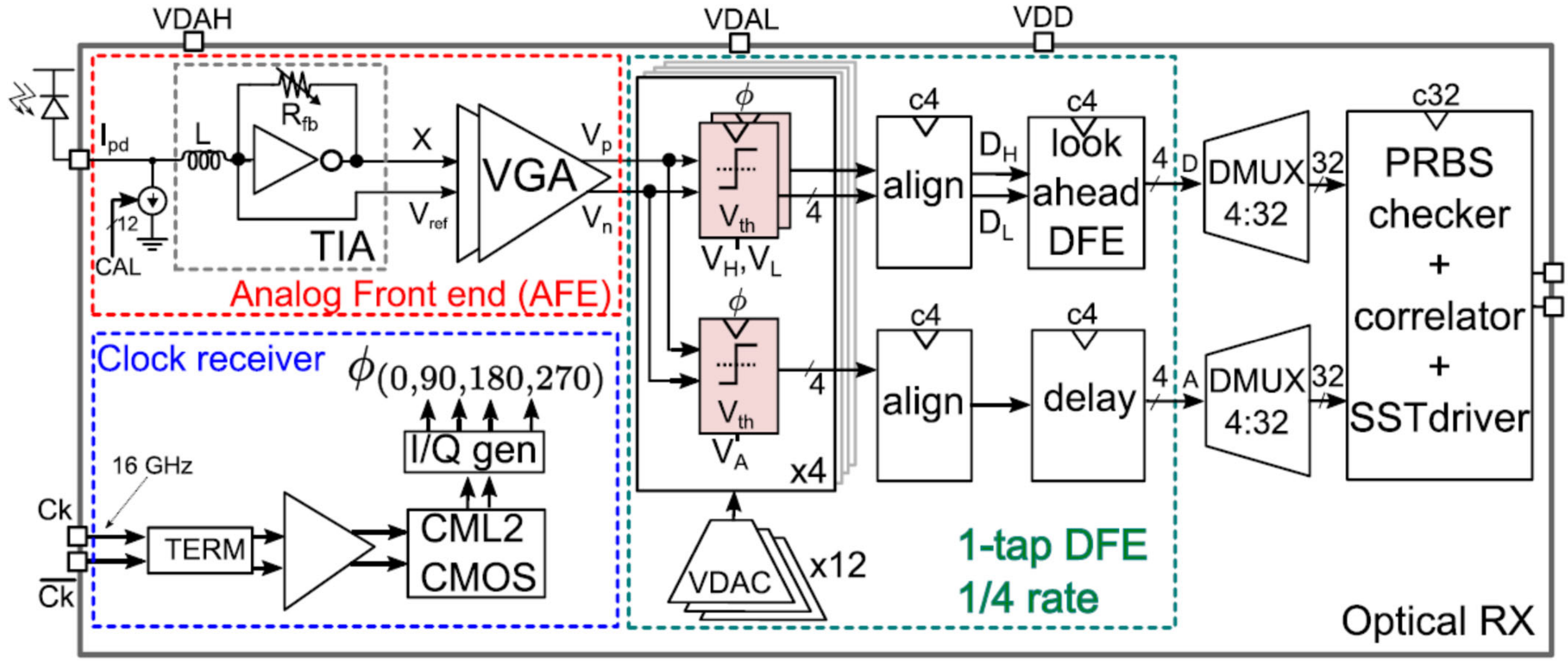
25Gb/s Eye Diagram





Low-BW TIA & DFE RX

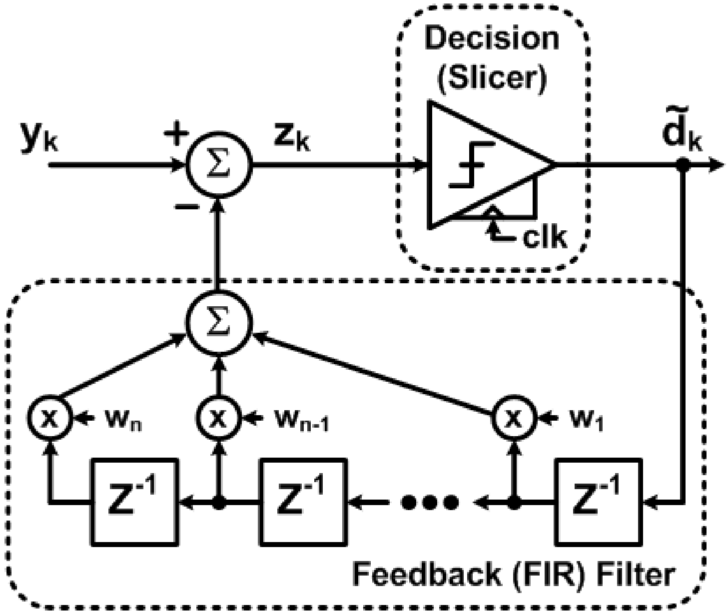
[Ozkaya JSSC 2017]



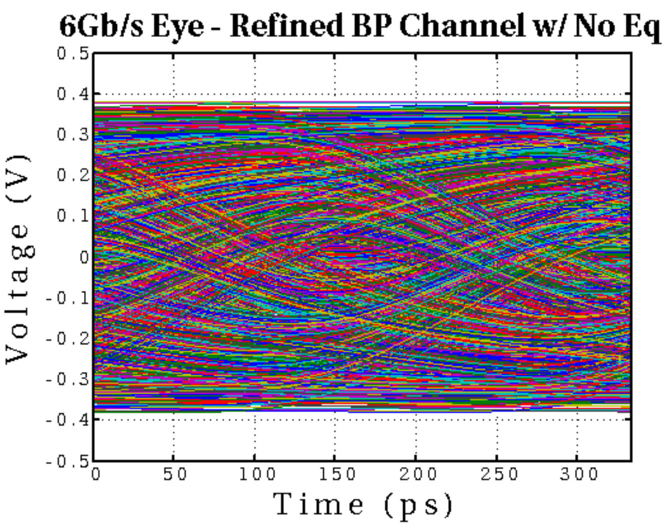
- In a similar manner, a high-gain low-bandwidth TIA is utilized
- The resultant ISI is cancelled by a subsequent 1-tap loop-unrolled DFE

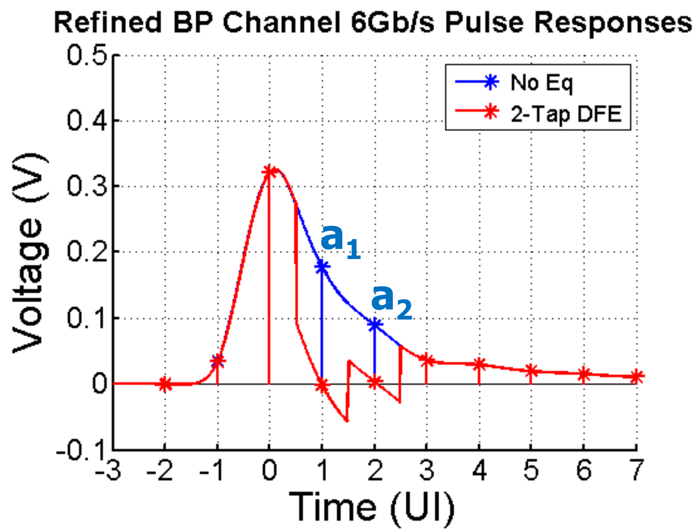
DFE Example

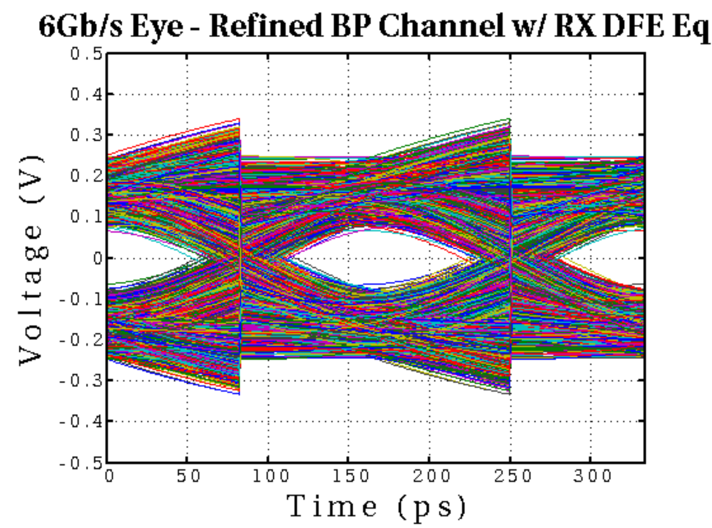
- If only DFE equalization, DFE tap coefficients should equal the unequalized channel pulse response values $[a_1\ a_2\ \ldots\ a_n]$
- With other equalization, DFE tap coefficients should equal the pre-DFE pulse response values
  - DFE provides flexibility in the optimization of other equalizer circuits
  - i.e., you can optimize a TX equalizer without caring about the ISI terms that the DFE will take care of



$[w_1\ w_2]=[a_1\ a_2]$



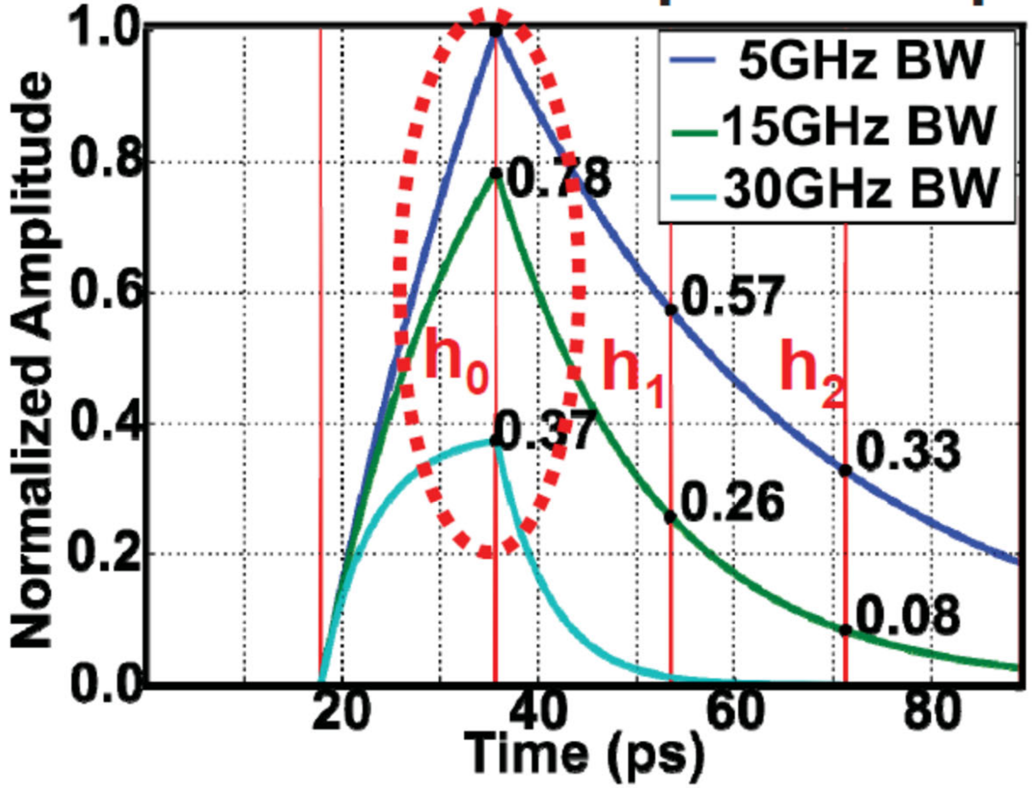


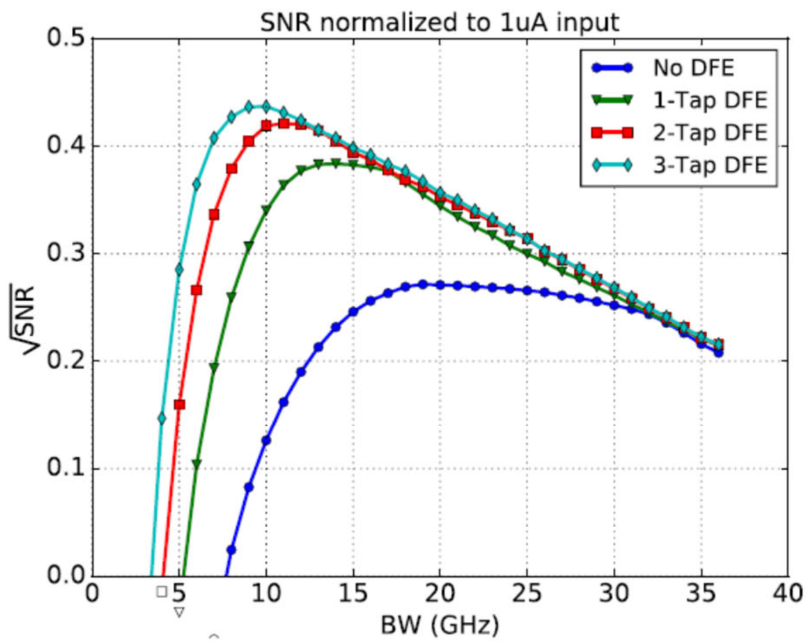


Low-BW TIA & DFE RX

[Ozkaya JSSC 2017]

1st order TIA model pulse response (56Gb/s)

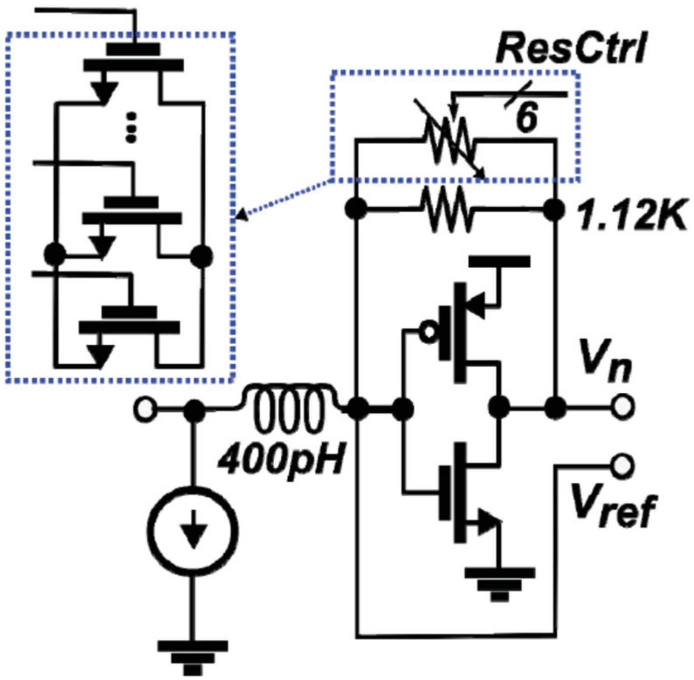




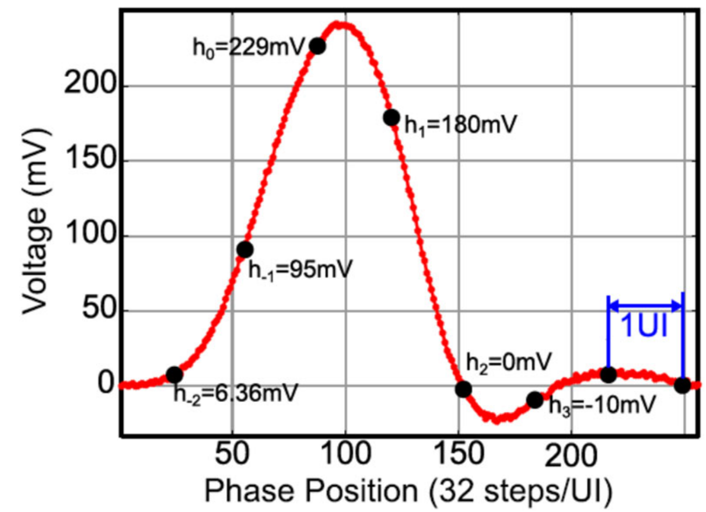
- As RF is increased, the main cursor increases and the SNR improves is ISI is cancelled by a DFE
- Large performance benefit with a low-complexity 1-tap DFE

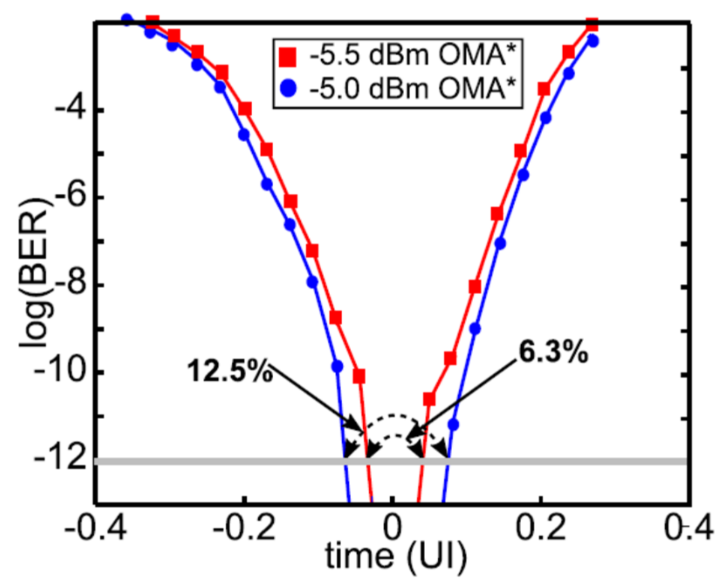
Low-BW TIA & DFE RX

[Ozkaya JSSC 2017]



64Gb/s Pulse Response & Timing Margin





- Self-referenced TIA is used for differential generation
- Actual 64Gb/s pulse response has a significant pre-cursor ISI tap, which requires a 2-tap TX FFE

Next Time

- Main/Limiting Amplifiers