March 5, 2024

ECEN 721: Optical Interconnects

Homework #3

Due: 3-21-2024, 11:59PM

Homeworks will not be received after due.

Instructor: Sam Palermo

This homework requires transistor-level circuit design. You may use any CMOS technology to solve the problem, as long as it is a 90nm or mode advanced technology node (shorter channel length). For students who do not have access to a design kit, instructions on how to access the default 90nm CMOS transistor models are posted on the website in the project section. For this 90nm technology assume a nominal 1.2V supply.

1. **CMOS Technology Characterization**. In order to estimate what level of performance is achievable with a given process technology, it is useful to run some initial characterization simulations. For both NMOS and PMOS transistors with dimensions W=1µm and L=L_{min}, **plot the transition frequency (f_T) versus $|V_{GS}|$ and also versus I_{DS} – 4 plots total (2 per transistor)**. Use the test circuits in Fig. 1. The easiest way to do this is to run a DC sweep with $|V_{GS}|$ varying from 0 to VDD and plot the following equation.

$$f_T = \frac{g_m}{2\pi C_{gg}} \tag{1}$$

Where C_{gg} is the total gate capacitance. Comment on the results. For the f_T plot versus $|V_{GS}|$, use a linear scale for both axes. For the f_T plot versus $|I_{DS}|$, use a log scale for the x-axis (current) and a linear scale for the y-axis (frequency). Discuss how this characterization data impacts the design of high-speed circuits.

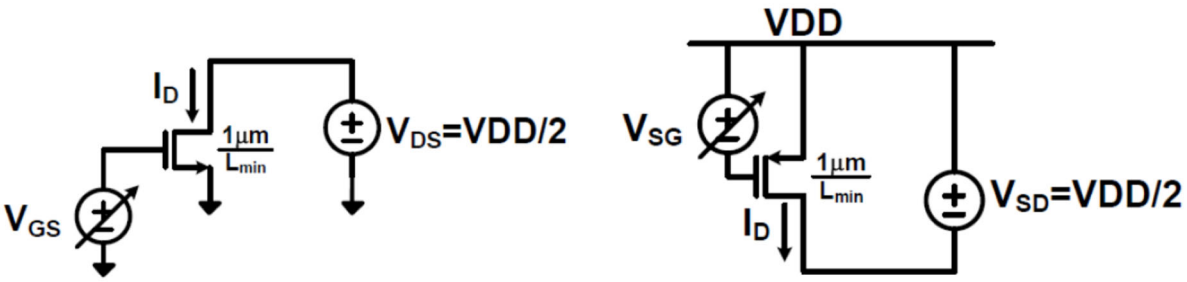


Figure 1 (a) NMOS f_T Test Circuit (b) PMOS f_T Test Circuit

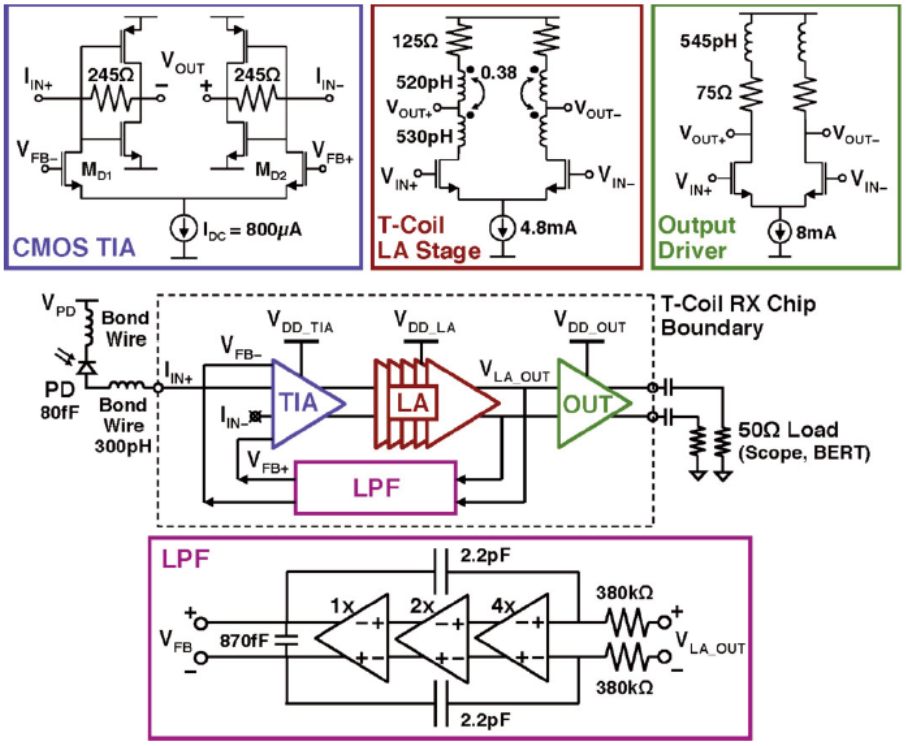
2. **10Gb/s Common-Gate TIA Design**. Design a differential common-gate TIA with mid-band Z_T=1kΩ and 7GHz bandwidth. Assume that the photodetector at the TIA input can be modeled as a simple 40fF capacitor. Also assume that the TIA has to drive a 20fF load. Note, if you can't achieve the Z_T specification with a single TIA stage, you can cascade a voltage amplifier stage(s). Turn in the following for your design.
   a. Schematics with details of transistor sizing and any passive components.
   b. Plot of $Z_T(f)$
   c. Plot of the group delay (f)
   d. Plot of the input-referred current noise density.
   e. Give the input-referred rms noise current i_n^{rms} and the sensitivity for a BER=10^{-12}. Note, to obtain i_n^{rms} it is easier to integrate the output voltage noise power, divide by the mid-band Z_T^2, and take the square-root.
   f. A 10Gb/s eye diagram with i_{in}=20μ$A_{pp.}$ Use a pseudo-random input sequence of 2^7-1 or higher to produce the eye diagram.

3. **10Gb/s Feedback TIA Design**. Design a differential feedback TIA with mid-band Z_T=1kΩ and 7GHz bandwidth. Assume that the photodetector at the TIA input can be modeled as a simple 40fF capacitor. Also assume that the TIA has to drive a 20fF load. It is your choice whether to implement a "balanced" or "pseudo-differential" design. Note, if you can't achieve the Z_T specification with a single TIA stage, you can cascade a voltage amplifier stage(s). Turn in the following for your design.
   a. Schematics with details of transistor sizing and any passive components.
   b. Plot of $Z_T(f)$
   c. Plot of the group delay (f)
   d. Plot of the input-referred current noise density.
   e. Give the input-referred rms noise current i_n^{rms} and the sensitivity for a BER=10^{-12}. Note, to obtain i_n^{rms} it is easier to integrate the output voltage noise power, divide by the mid-band Z_T^2, and take the square-root.
   f. A 10Gb/s eye diagram with i_{in}=20μ$A_{pp.}$ Use a pseudo-random input sequence of 2^7-1 or higher to produce the eye diagram.

4. **10Gb/s Limiting Amplifier Design**. Design a limiting amplifier with 30dB gain and 10GHz total bandwidth. Assume that the limiting amplifier has to drive a 20fF load. While there is no input capacitance specification, in Problem 4 we will cascade the Problem 2 TIA and this limiting amplifier. Turn in the following for your design.
   a. Schematics with details of transistor sizing and any passive components.
   b. Plot of $A_v(f)$
   c. Plot of the group delay (f)
   d. Plot of the input-referred voltage noise density.
   e. Give the input-referred rms noise voltage v_n^{rms} and the sensitivity for a BER=10^{-12}.
   f. A 10Gb/s eye diagram with v_{in}=20m$V_{pp.}$ Use a pseudo-random input sequence of 2^7-1 or higher to produce the eye diagram.

5. **10Gb/s Optical Receiver Simulation**. Now cascade the Problem 3 TIA and Problem 4 LA to drive a 20fF load. If any offset current is required, you can implement that in an ideal open-loop manner to speed-up the simulations. Turn in the following for your design.
   a. Plot of the total receiver gain (f). This should have y-axis units of ohms.
   b. Plot of the total receiver group delay (f)
   c. Plot of the total receiver input-referred current noise density.
   d. Give the input-referred rms noise current i_n^{rms} and the sensitivity for a BER=10^{-12}. A 10Gb/s eye diagram with i_{in}=20$\mu A_{pp.}$ Use a pseudo-random input sequence of 2^7-1 or higher to produce the eye diagram.

In the design of the feedback TIA and limiting amplifier, you are free to use whatever topologies you like. If you would like to follow a reference design, the following reference is a nice low-voltage design.



J. Proesel, C. Schow, and A. Rylyakov, "25Gb/s 3.6pJ/b and 15Gb/s 1.37pJ/b VCSEL-Based Optical Links in 90nm CMOS," *International Solid-State Circuits Conference*, Feb. 2012.