March 31, 2022

# ECEN 689: Optical Interconnects

Final Project

Instructor: Sam Palermo

Project teams can consist of 1-3 students.

## Project Topics

### Project #1 – 10Gb/s PAM2 1km Optical Link Design

This project investigates the design of a 10Gb/s PAM2 1km optical link for a target BER=$10^{-12}$. A complete link budget should be constructed considering the chosen optical source, channel losses, optical channel, and receiver sensitivity. The optical source can either be a directly modulated VCSEL or an externally modulated CW laser with either a MZM, EAM, or ring resonator modulator (carrier-injection or carrier depletion). The photodetector can either be p-i-n (waveguide or discrete), APD, or OA/p-i-n. However, preference is given to a p-i-n detector. Key specs for the receiver decision element are: 1m$V_{rms}$ noise, 1mV offset, and 20fF total input capacitance. The driver and receiver front-end circuits should be designed at the transistor level. Note, you don't have to design the decision element. 10Gb/s eye diagrams should be produced with equivalent circuit models for the optical source and photodetectors. Show eye diagrams at both the transmitter output and the final receiver output. A key metric of the link design is the overall power efficiency (mW/Gbps). Note, for an externally-modulated system this should include the CW laser power.

### Project #2 – 112Gb/s PAM4 100m Optical Link Design

This project investigates the design of a 112Gb/s PAM4 100m optical link with a VCSEL-based transmitter for a target BER=$10^{-6}$. A complete link budget should be constructed considering the VCSEL, channel losses, optical channel, and receiver sensitivity. The optical source should be a directly modulated VCSEL and a p-i-n photodetector should be utilized. Key specs for the receiver decision element are: 1m$V_{rms}$ noise, 1mV offset, and 128fF total input capacitance. The driver and receiver front-end circuits should be designed at the transistor level. Note, you don't have to design the decision element. 112Gb/s PAM4 eye diagrams should be produced with equivalent circuit models for the VCSEL and photodetectors. Equalization circuitry will be most likely required due to VCSEL bandwidth limitations. Show eye diagrams at both the transmitter output and the final receiver output. A key metric of the link design is the overall power efficiency (mW/Gbps).

### Project #3 – Topic of Your Choice

I welcome any project suggestions related to optical interconnects circuits and systems.

## Important Dates

- April 19 Preliminary Report. This will be HW4.
- May 3 Final Report Due
- May 10 Project Presentation Due

**Preliminary Report Required Sections**

1. Motivation and Project Overview
2. Literature Survey
3. Proposed Architecture
    a. This can change for the final report
4. Initial Simulation Results
5. Plan of Work
    a. A description of what will be completed for the final report

**Final Report Required Sections**

1. Motivation and Project Overview
2. Literature Survey
3. Architecture
4. Simulation Results
    a. This section must include a Table comparing your design with current references
5. Conclusion

**The Project Presentation should include the same sections as the final report.**