Comparison of On-die Global Clock Distribution Methods for Parallel Serial Links

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***Abstract*— This paper presents a comparative study of clock distribution methods for serial links, including inverter chain, CML chain, transmission line, inductive load and capacitively driven wires in regards to delay, jitter and power consumption. Analysis, simulation and design insights are given for each method for 2.5GHz clock propagation by on-die 5mm wire in a 90nm CMOS process. Simulations show the transmission line achieves least jitter and delay, while capacitively driven wire illustrates the best power-jitter and power-delay product.**

***Index Terms*--- Clock distribution, jitter, serial link**

I. INTRODUCTION

The aggressive trend of increasing data rate in wireline communication has continued into multi-Gb/s range [1]-[3]. This development benefits from the technology scaling down to 90nm, 65nm or even smaller CMOS process. On one hand, the large bandwidth among far-separated function units on the same die is critical so as not to decrease the whole performance. But on the other hand, little overhead in power budget is expected for these on-die links to make the whole system more efficient and low power. Since the supply voltage does not decrease much as technology scales into sub-100nm process, it is hard to meet the power budget at higher and higher date rate if traditional way is still used. These situations are also same for on-die global clock distribution. In fact, it suffers more than data does. First, data may not flip at every period but clock must flip. Second, there is more severe timing requirement for the global clock. Though many methods for data or clock distribution for serial links [2]-[4] are proposed, no systemic performance comparisons are derived.

In this paper, we analyze the five different clock distribution methods: inverter chain, CML chain, transmission line, inductive load and capacitively driven wires (CDW), as shown in Fig. 1. The design details of them are described in Section II. Section III compares the simulation results in a 90nm CMOS process and Section IV draws a conclusion.

II. CIRCUIT ANALYSIS

The five clock distribution methods can be classified into full swing propagation like inverter chain and low swing propagation like CML, transmission line, inductive load and CDW. Dynamic power dissipation of clock distribution at frequency f can be expressed as

$$P_{dyn} = C_L V^2 f \tag{1}$$

where C_L is load capacitance and V is the propagation swing [5]. Low swing methods benefit from lower dynamic power and less aggressive to substrate and other circuits. But they may suffer from large static power consumption like CML. Also, auxiliary circuits such as level shifter are needed at local receiver side to convert to full swing.

A. Inverter Chain

Inverter chain is the most traditional method for clock distribution. As shown in Fig. 1(a), it can be divided into several segments to minimize the propagation delay. For hand calculation, inverter chain is modeled as shown in Fig. 2. By using Elmore delay formula [5], propagation delay of inverter chain can be expressed as

$$t_p = N\left[0.69R_{eq}c_o + \left(0.69R_{eq} + 0.38\frac{R_w L}{N}\right)\frac{C_w L}{N} + 0.69\left(R_{eq} + \frac{R_w L}{N}\right)c_i\right]$$

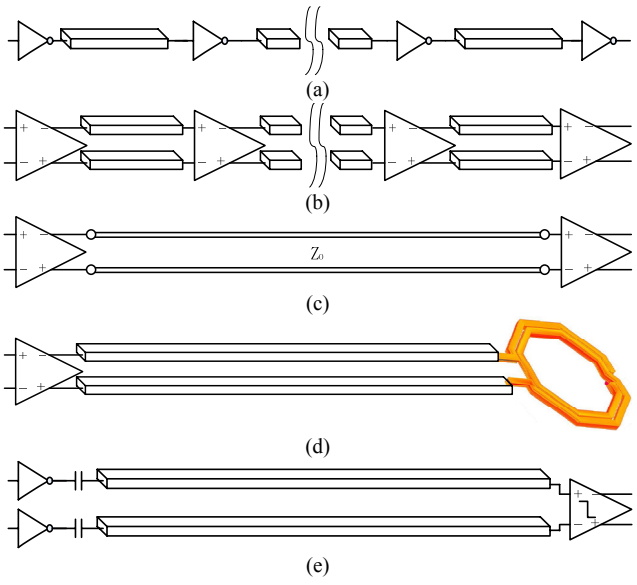

Figure 1. Structures for clock distribution (a) Inverter chain (b) CML chain (c) Transmition line (d) Inductive load and (e) CDW

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$$= N\left[0.69\frac{R_{equ}}{m}mc_{ou} + \left(0.69\frac{R_{equ}}{m} + 0.38\frac{R_wL}{N}\right)\frac{C_wL}{N} + 0.69\left(\frac{R_{equ}}{m} + \frac{R_wL}{N}\right)mc_{iu}\right]$$

$$= 0.69NR_{equ}\left(c_{ou} + c_{iu}\right) + 0.38\frac{R_wC_wL^2}{N} + 0.69\frac{R_{equ}C_wL}{m} + 0.69mR_wLc_{iu} \quad (2)$$

where N is the number of segments. C_i, C_o, R_{eq} are the input, output capacitance and equivalent resistance of the inverter. R_w, C_w are the unit resistance and capacitance of the metal wire. L is the total length of the metal wire. C_{iu}, C_{ou}, R_{equ} are the input, output capacitance and equivalent resistance of a unit strength inverter. Usually a unit strength inverter is defined, so that other inverters are m multiples of the unit inverter. When

$$N = 0.742L\sqrt{\frac{R_wC_w}{R_{equ}\left(c_{ou} + c_{iu}\right)}} \text{ and } m = \sqrt{\frac{R_{equ}C_w}{R_wc_{iu}}} \quad (3)$$

the inverter chain can get minimum propagation delay.

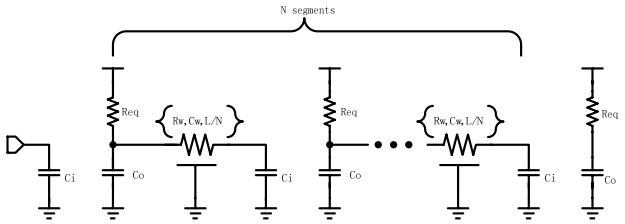
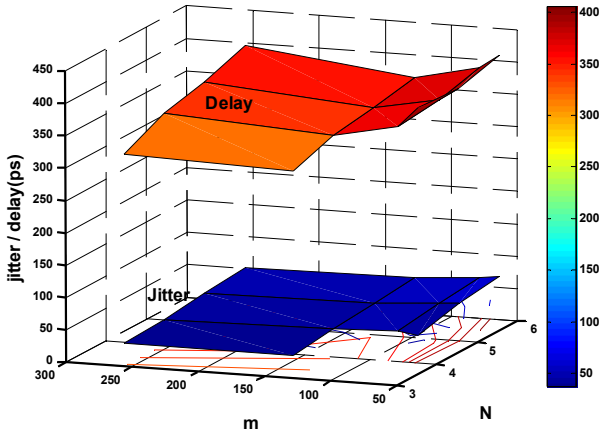


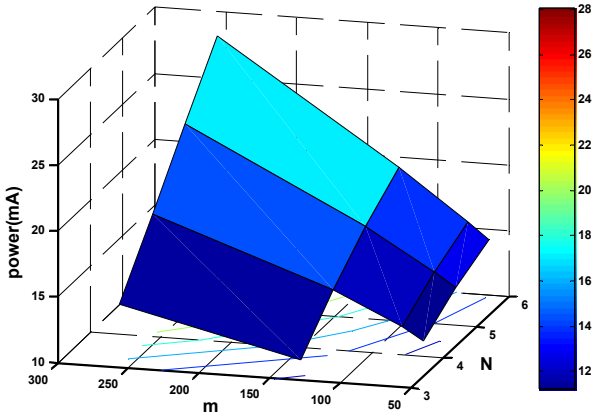
Figure 2. Modeling of chain. N is the no. of segments. C_i, C_o, R_{eq} are the input, output capacitance and equivalent resistance of the inverter or CML. Rw, Cw is the unit resistance and capacitance of the metal wire. L is the total length of the metal wire.

In the specific process we used, the sheet resistance and unit capacitance of the top thick metal 8 are R□=47mΩ, C□=0.25fF/um^2, and its minimum pitch is 560nm. It's not necessary to use minimum width for clock distribution. If 2x wider metal is chosen, then R_w=0.083Ω/um, C_w=0.134fF/um. And it is assumed the metal wire is 5mm long. A unit strength inverter is designed as W/L of NMOS: 0.4u/0.1u, W/L of PMOS: 1u/0.1u. Simulated C_{iu} and C_{ou} are 1.3fF and 1fF respectively. For hand calculation, R_{equ} is estimated by average the on resistance of unit inverter R_{on} at supply and half supply, as $1/2(R_{on}(V_{DD})+R_{on}(V_{DD}/2))\approx 6k\Omega$. So the segment number N and multiple m for optimal delay can be calculated from (3) as N=3.33, round to 3, and m≈86. However, these numbers are not optimal for power and jitter performance. Inverter is sensitive to supply noise because of its low PSRR, so less number of inverters is preferred in regard to jitter performance.

Simulations under the condition of 5mm long wire, 2.5GHz clock and ±5% supply variation are shown in Fig. 3. Minimum jitter ~36ps is achieved when segment N=3, multiple m=256, while minimum delay ~321ps is when N=3, m=128, and minimum power is when N=4, m=64. From the viewpoint of jitter-power product and delay-power product, N=3, m=128 gets the best performance. The case N=3, m=64 is failed, i.e. its eye diagram is almost closed, which is not plotted in Fig. 3.



(a)



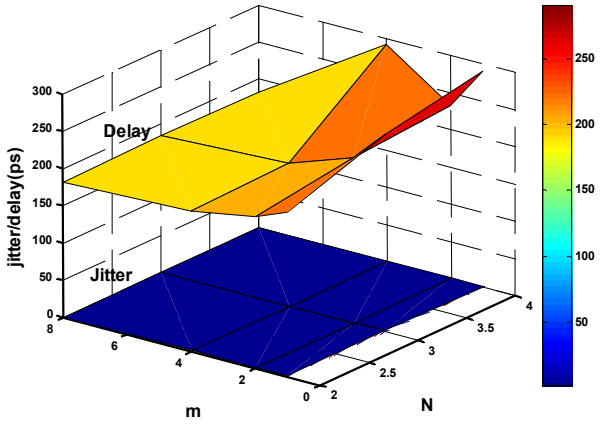
(b)

Figure 3. Simulation result of inverter chain for different segment number N and multiple m in (a) jitter and delay, (b) power

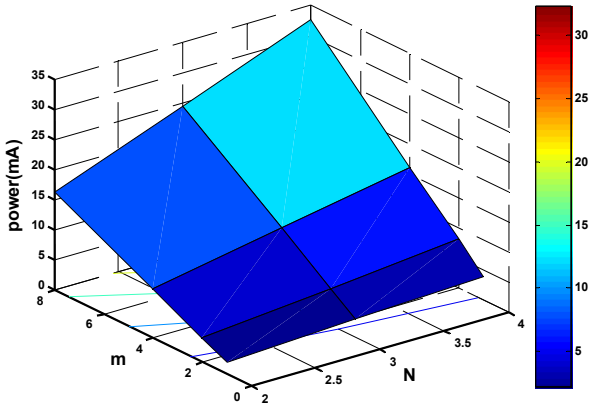
B. *CML Chain*

CML chain, as shown in Fig. 1 (b), can conduct much faster signal due to its current mode nature. It can be analyzed using the same model as Fig. 2. A unit CML is designed with top load resistor 200Ω and 1mA current source. So the output swing is 0.2V and R_{equ} is 200Ω by this choice. W/L of input device pair is 20u/0.1u. Simulated C_{iu} and C_{ou} for CML are 30fF and 6fF respectively. Doing the same analysis as the inverter chain and also assuming 5mm long metal wire, we can get N≈4 and m=3.3 for optimal delay from equation (3). Though PSRR of CML is much better than inverter, it still introduces some noise. CML is also much power hungry due to its static power dissipation, so minimum number of segments is favorable for low power design. However, since the delay of CML is smaller than inverter, it's not necessary to get optimal propagation time to meet the timing requirement.

Fig. 4 presents the simulation results for different N and m. Minimum jitter ~0.5ps is achieved when N=2, m=8, while minimum delay ~182ps is N=4, m=8, and minimum power is N=2, m=1. From the viewpoint of jitter-power product and delay-power product, N=2, m=1 achieves a good tradeoff.



(a)



(b)

Figure 4. Simulation result of CML chain for different segment number N and multiple m in (a) jitter and delay, (b) power

C. *Transmission line*

Transmission line effect takes into effect when total resistance of metal wire is small enough regarding to the characteristic impedance Z_0. Then the distributed inductance of the wire starts to affect the delay behavior. The delay of transmission line is smallest among all the methods due to its speed-of-light propagation velocity. As a passive element, it does not introduce jitter itself, but the driven circuits does.

The on-die transmission line is realized by a coupled differential microstrip in top thick metal 8 with underneath ground shield in metal 6 as shown in Fig. 5. It's not necessary to make exactly standard 100Ω differential characteristic impedance as long as it's matched on-die by its source and load. Actually, Z_0 is preferred to be designed large enough compared with the resistance of metal as mentioned before. And large Z_0 also saves power of the driven CML circuit for the given swing. However, Z_0 is limited by the parasitic capacitance on the die. After several trial and errors, we choose the transmission line with W = 6um, space d=2.5um, ground wire width Ws=4um, and space between signal wire and ground wire s =4um. With this choice, the simulated differential characteristic impedance is 120Ω and DC resistance is 42Ω. It behaves as a lossy transmission line, and the signal amplitude would tamper a little along the line.

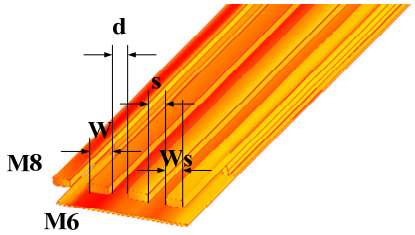


Figure 5. Structure of transmission line

Eye diagrams of data transition at different distance along the transmission line are shown in Fig. 6. The delay is as small as 43ps and with only 0.18ps jitter. However, the driven CML consumes 4mA.

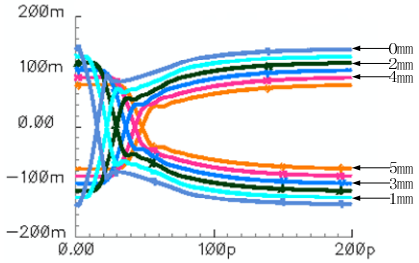
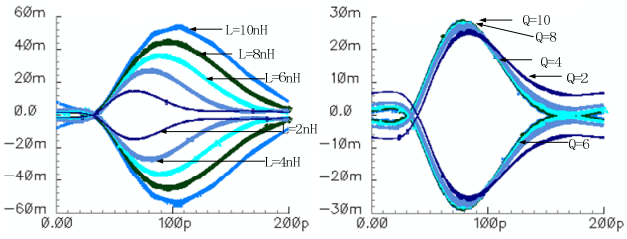


Figure 6. Eye diagram of data transition along the transmission line

D. *Inductive load*

Other than taking advantage of distributed inductance as transmission line, a lumped on-die inductor can be employed to boost both the propagation time and voltage swing, as shown in Fig. 1 (d) [2]. An estimation of inductance can be made by resonant frequency and total capacitance of the metal wire. Assume the same 5mm wire as inverter chain, C_{total}= Cw· L=670fF, so the inductance to cancel this capacitance at 2.5G is about $1/C_{total}\omega^2$=6nH. Larger inductance can push the zero introduced by inductor to lower frequency band, thus causing more boost at desired frequency. However, this may cost more area on the chip. Since the area of inductor is directly related to its inductance and quality factor, careful choice is necessary to achieve these within reasonable area.



(a) (b)

Figure 7. Eye diagram of data transition for inductive load
(a) Q=4 with different L (b) L=4nH with different Q

Fig. 7 presents the results for inductive load. Die area for inductor can be saved by low inductance and low quality factor Q. As Fig. 7 (b) shows quality factor Q of the on-die inductor does not affect much on eye diagram, that's because the long metal wire resistance has dominated loaded Q. In all the cases, jitter is smaller than 1ps. Like transmission line, its swing also gets smaller along the wire.

E. *Capacitively driven wires(CDW)*

Fig. 1 (e) shows the capacitively driven method [4]. The capacitance seen by the inverter is significantly reduced due to the capacitor in series, so the power consumption is reduced too. The propagation time can be estimated as the model in Fig. 8.

$$t_p = 0.69R_{eq}\left(c_o + c_{p1} + c_c\right) + 0.19R_wC_wL^2 \qquad (4)$$

where C_i, C_o, R_{eq} are the input, output capacitance and equivalent resistance of the driven inverter, R_w, C_w are the unit resistance and capacitance of the metal wire. L is the total length. Although minimum series capacitor Cc will reduce the delay and power, it also reduces the swing because of the capacitance divider. So its minimum value should be limited by the sensitivity of comparator at receiver side with some margin. Although Cc blocks the DC, many methods can be implemented to control the DC bias [4].

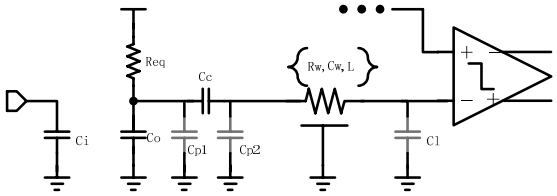


Figure 8. Modeling of CDW

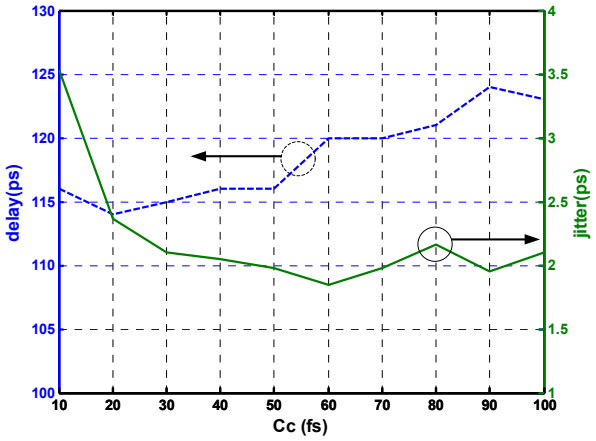
Fig. 9 depicts the delay, jitter, swing and power of CDW with different values of series Cc. This method gives the minimum power dissipation in all five methods.

III. DISCUSSION

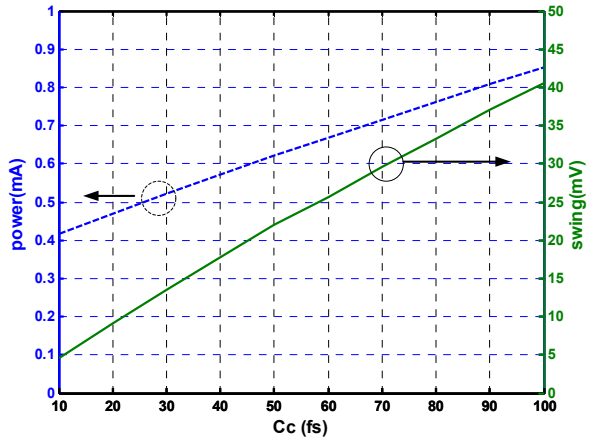
Simulations of these five clock distribution methods have been presented in a 1.2V 8M 90nm CMOS process, all under the condition of 5mm long wire, 2.5GHz clock and ±5% supply variation. Although all the repeaterless low-swing propagation methods suffered from unequal swing along the metal wire due to its lossy resistance, local buffers can be employed to regenerate the signal. A balanced choice among jitter, delay, power, area and robustness is chosen for each method for reasonable comparison. Their performances are summarized in Table I. Transmission line gets the best jitter and delay performance. And CDW gives the minimum jitter-power product and delay-power product.

TABLE I. PERFORMANCE SUMMARY OF FIVE CLOCK DISTRIBUTIONS

Technology	1.2V 90nm CMOS		
Methods (with optimal tradeoff)	**Performance**		
	jitter(ps)	***delay(ps)***	***power(mW)***
Inverter chain (N=3, m=128)	36	321	11.5
CML chain (N=2, m=1)	1	221	2
Transmission line	0.18	43	4
Inductive load (L=6nH, Q=2)	0.42	55	4
CDW (Cc=50f)	1.98	116	0.62



(a)



(b)

Figure 9. CDW simulation results for different Cc

IV. CONCLUSION

A comparison and design analysis regarding five clock distribution methods for serial links are presented. Simulations in a 1.2V 90nm CMOS process have been performed to verify the design tradeoffs and show that transmission line can achieve least jitter and delay, while CDW consumes lowest power with reasonable jitter and delay performance.

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