Characterizing Sampling Aperture of Clocked Comparators

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Abstract

Practical simulation and measurement methods based on impulse sensitivity functions to characterize the sampling aperture of clocked comparators are demonstrated on a 90nm CMOS testchip. The results comparing a StrongARM latch and a CML latch suggest that the StrongARM latch has a narrower aperture of 23ps but its aperture center is more sensitive to supply (65ps/V). The CML latch has a higher sampling gain of 88.8dB but a lower bandwidth of 6.8GHz.
Keywords: comparator, aperture and impulse sensitivity function

Introduction

This paper characterizes the sampling aperture or time resolution of a clocked comparator both in simulation and in measurement. Sampling aperture is a well established concept which was originally analyzed for sampling switches [1]. Although the analysis has been extended in [2] for clocked comparators, it has not been validated through measurement due to the impracticality of previously proposed methods. In this paper, we propose a practical method to characterize sampling apertures suitable for both simulation and measurement and discuss their results for a variant of the StrongARM comparator [3] and a CML-type comparator [4] implemented in 90nm CMOS process. Similar to the results obtained in [2], our results show that 1) the StrongARM comparator has finer time resolution than the CML, 2) the CML has higher sampling gain and input sensitivity at the expense of a lower bandwidth and 3) the CML has higher immunity to supply variations. Because of the last two results, CML latches are often preferred in high-speed I/O interfaces. However, we have also found that the characteristic of the sampling apertures are easily dominated by other components in the system preceding the comparators such as pre-amplifiers, emphasizing the importance of including these preceding circuits when analyzing the effective sampling aperture.

Clocked Comparator Model

Fig. 1 illustrates our assumed model for a clocked comparator. The clocked comparator periodically samples the input voltage $V_{in}(t)$ which is then regeneratively amplified to resolve a digital bit. The sampled and amplified voltage $V_s[n]$ can be expressed as a weighted time-average of the input voltage. The weighting function $ISF(\tau)$ is the impulse sensitivity function (ISF), which describes the sensitivity of the sampled voltage $V_s[n]$ to an impulse arriving at the input at time $nT+\tau$. The final digital output $D_{out}[n]$ can then be determined by the polarity of $V_s[n]$, ignoring hysteresis.

While the ISF was originally defined for oscillators to analyze the phase noise [5], the ISF of a clocked comparator can also reveal many of its important characteristics, as illustrated in Fig 1. For example, the width of the ISF corresponds to the aperture width or the time resolution of the comparator. The area under the ISF is the DC sampling gain. The center of the ISF is the sampling time. And the sampling
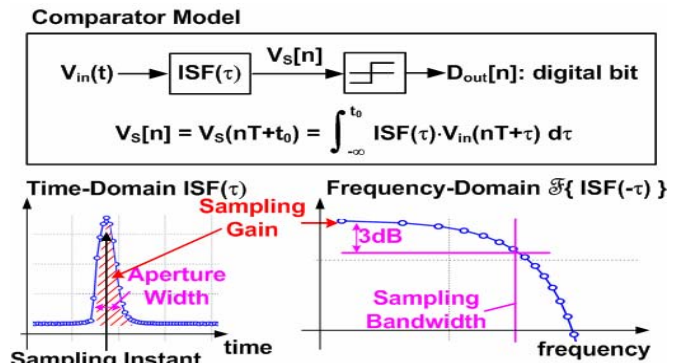

Fig 1: A clocked comparator model based on the ISF

bandwidth is found from the Fourier transform of the ISF.

Characterizing ISF in simulation and measurement

Fig. 2 illustrates how we characterize the ISF of a clocked comparator in simulation. We apply a small step to the comparator input at time τ and servo the offset voltage of the step waveform to a level $V_{MS}(\tau)$ that makes the comparator metastable. We then measure $V_{MS}(\tau)$ for various step arrival times τ to obtain the normalized step sensitivity function $SSF(\tau)$ which represents the size of the $V_{MS}(\tau)$-V_L relative to the step height (V_H-V_L). The equations to derive $SSF(\tau)$ and $ISF(\tau)$ are listed in step 3 of Fig. 2. Our method based on the offset search does not rely on accurate measurements of the output voltages values [1] or the uses of impulses [2], making it more practical to implement in lab and is less prone to errors.

Fig. 3 describes how the proposed method can be applied to measure the ISF in the lab. As in the simulation, a small step whose edge is spaced from the clock edge by τ is applied to the comparator input and the step's offset voltage V_{OS} is swept until the value that makes the comparator metastable is found, i.e. $V_{MS}(\tau)$. The only difference is that the metastable point is found statistically by counting the occurrences of the output bit being 0 or 1 over multiple measurements (e.g. 80). In other words, $V_{MS}(\tau)$ is defined as the step offset V_{OS} that yields the equal probabilities of ones and zeros. Once $V_{MS}(\tau)$ is measured for various time offset τ's, the SSF and ISF can be derived via the same equations as used for simulation results.

Simulation and Measurement Results

We applied our ISF characterization methodology to a comparator testchip implemented in a 90nm CMOS, containing a total of 16 comparators including the StrongARM and CML comparators as shown in Fig. 4. Each comparator is preceded by an identical pre-amplifier to isolate comparator interactions and each output is fed to a 16-bit shift register which can be read out in parallel. Only one comparator is active at any given time during characterization. Due to the limited pin resources available on our testchip, all 16 samplers shared the same input pins, which lowered the input channel bandwidth and widened the measured ISFs.
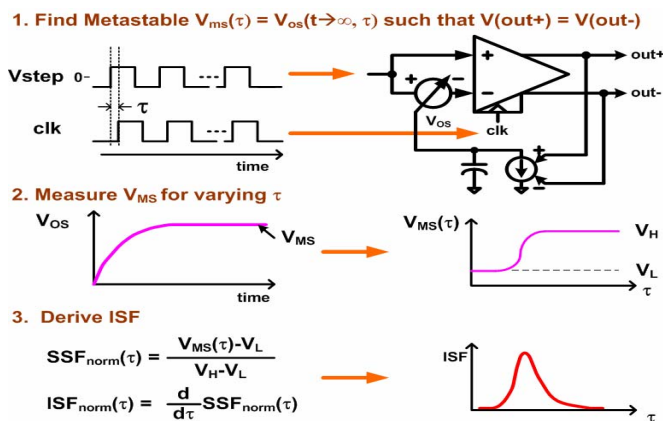
Vstep 0 —
clk

τ
time

out+
out-
V_{OS} clk

2. Measure V_{MS} for varying τ

V_{OS} V_{MS}
time

$V_{MS}(\tau)$ V_H
V_L
τ

3. Derive ISF

$$SSF_{norm}(\tau) = \frac{V_{MS}(\tau) - V_L}{V_H - V_L}$$

$$ISF_{norm}(\tau) = \frac{d}{d\tau} SSF_{norm}(\tau)$$

ISF
τ

Fig. 2: **Characterizing the comparator ISF in simulation**

1. Find Metastable $V_{MS}(\tau) = V_{OS}$ such that Prob(bit m=1) = 0.5

Shift Registers
Vin V_{os}
V_{cm}
bit m
clk
τ

out+
out-
clk
1 1 x 0 0
bit m

2. Measure V_{MS} for varying τ

Prob(bit m = 1)
0.5
Metastable points
V_{os}
$V_{MS}(\tau)$

$V_{MS}(\tau)$ V_H
V_L
τ

3. Derive ISF

$$SSF_{norm}(\tau) = \frac{V_{MS}(\tau) - V_L}{V_H - V_L}$$

$$ISF_{norm}(\tau) = \frac{d}{d\tau} SSF_{norm}(\tau)$$

ISF
τ

Fig. 3: Characterizing the comparator ISF in measurement

To alleviate this problem, we measured the input channel response with a VNA and used a step generator with equalization capability to try to equalize the input channel response and thus deliver the best possible step waveform to the comparator input. Nonetheless, there still remained a residual channel response with -3dB bandwidth of 1.6GHz.

Fig. 5 compares the simulated ISF including the residual channel response and the measured ISF with the setup described above. The results of both the StrongARM and CML comparators demonstrate good agreements between the two ISFs. The simulated ISFs of the comparators themselves are also plotted and the estimated aperture times, sampling bandwidths and gains are listed in the tables in Fig. 5. The difference between the ISF of just the comparator and the ISF including the pre-amplifier and residual channel response emphasizes the importance of including the preceding circuits when analyzing the effective sampling aperture.

Comparator Design Trade-offs

The simulation results in Fig. 6 highlight key design trade-offs in the StrongARM and CML comparators. Fig. 6(a) and (b) show that increasing the input device size can improve the sampling gain and bandwidth for the StrongARM comparator, while it degrades those of the CML, because increasing its input devices increases the output load. Fig. 6(c) and (d) show that the sampling time of the StrongARM varies with the supply voltage, while that of the CML does not. Fig. 6(e) and (f) show that as the clock rise time increases for the StrongARM comparator, the gain improves but the bandwidth degrades, as previously analyzed in [6]. However, it is noteworthy that it is not always better to have a narrow aperture, especially when noise is present in the system.

References

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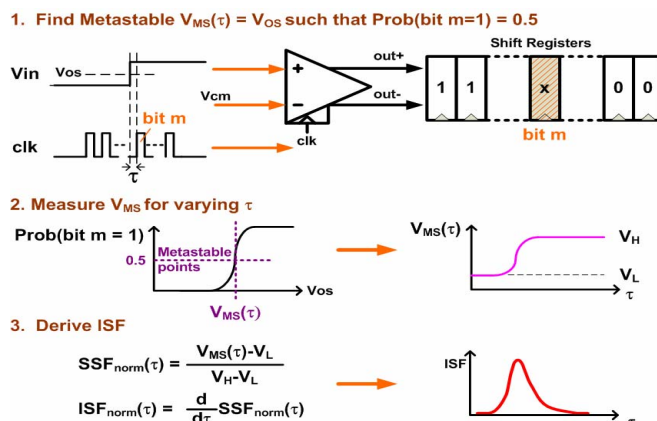
Sampler Quad

4 comparators in each quad

Vin+/- Amp Strong-Arm Latch SR Latch 16-bit Shift Reg

Clk+/- Amp CML Latch ECL To CMOS 16-bit Shift Reg

To 2 more comparators

Sel
test out

V_{in+} V_{in-}
Quad 1 Quad 2 Quad 3 Quad 4 Pad Drivers
CLK+ CLK-
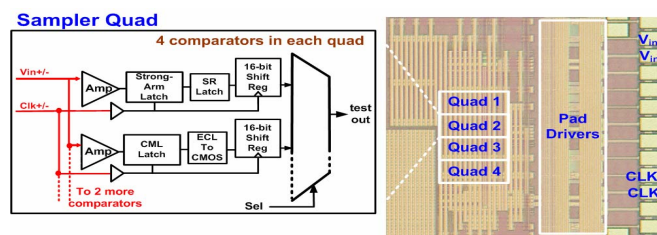
Fig. 4: Die Photograph and testchip block diagram

Effective Channel

EQ
SMA
Package Bond wire and PCB Trace
Pre Amp
Comparator
x16

Normalized StrongArm ISF comparison
Sim w/o input channel
Sim w/ residual channel
Lab measurement
ISF
time [ps]

StrongARM Comparator	Aperture Time [ps]	Sampling BW [GHz]	Sampling Gain [dB]
Sim w/o Channel	23	14.9	67.6
Sim w Channel	300	1.4	56.6
Lab	280	1.4	N/A

CML Comparator	Aperture Time [ps]	Sampling BW [GHz]	Sampling Gain [dB]
Sim w/o Channel	50	6.8	88.8
Sim w Channel	300	1.4	58.0
Lab	280	1.4	N/A

Note: the aperture time is defined as the width that contains 80% of the sensitivity similar to [1]

Normalized CML ISF comparison
Sim w/o input channel
Sim w/ residual channel
Lab measurement
ISF
time [ps]

Fig 5: Simulation and measurement results

Sampling Gain vs Input Size
Sampling Gain [dB]
StrongARM
CML
Input M1 Size [um]
(a)

Sampling BW vs Input Size
Sampling BW [GHz]
StrongARM
CML
Input M1 Size [um]
(b)

VDD effect on StrongARM ISF
Normalized ISF
0.9V
1.00V
1.10V
τ
(c)

VDD effect on CML ISF
Normalized ISF
0.9V
1.00V
1.10V
τ
(d)

Sampling Gain vs clk rise time
Sampling Gain [dB]
StrongARM
clock rise time [% cycle]
(e)

Sampling BW vs clk rise time
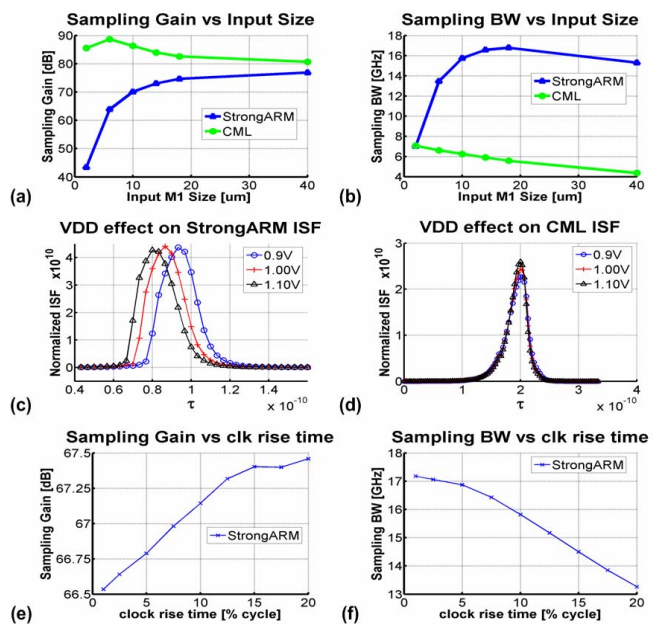Sampling BW [GHz]
StrongARM
clock rise time [% cycle]
(f)

Fig 6: **Design trade-offs in StrongARM and CML comparators**