April 8, 2010

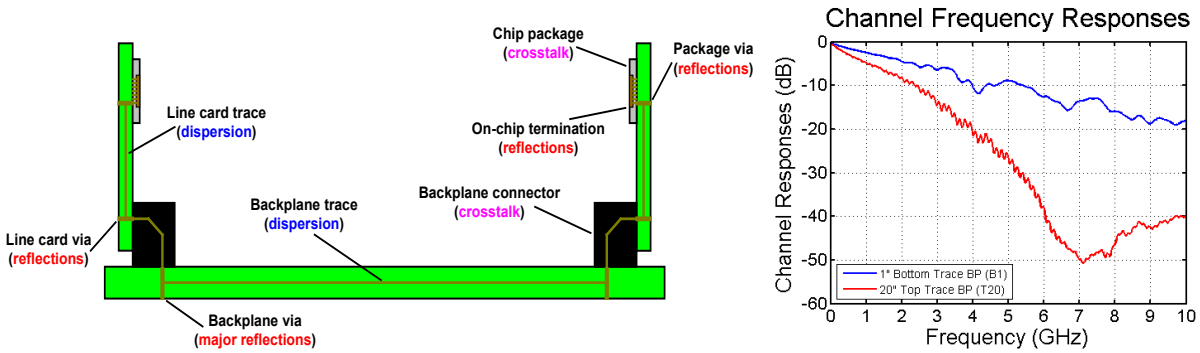
ECEN 689: High-Speed Links

Final Project

Instructor: Sam Palermo

Overview

This project involves the system and circuit design of a 10Gbps high-speed electrical link system for one of two applications (your choice). The project may be done in groups of up to 3 or 4 people.



Option 1 – Ultra-Low Power Link with a Refined Channel

The ultimate performance metric for this option is to obtain the best power efficiency (mW/Gbps) at the target 10Gbps data rate.

- Channel = "B1". This channel is a short 1" backplane with bottom traces plus ~5" of line card traces. While it is a backplane channel, we are using it to emulate a low-loss short refined channel that you may fine in a desktop or portable system.
- Optimize for power efficiency. A reasonable performance target will be <3mW/Gbps (30mW at 10Gbps). This is the power of the serialization (4:1), de-serialization (1:4), driver, receiver front-end, and timing recovery. The power of a global TX PLL and clock distribution may be amortized by a factor of 16 with the assumption of a potential multi-channel system.
- **Extra credit will be given to the group who obtains the best power efficiency**. Note that there needs to be sufficient simulation data to back up your claim.
- Forwarded clock system. This necessitates only a periodic phase adjustment timing recovery system.
- System crosstalk includes 2 FEXT aggressors

Option 2 – High-Performance Link with High-Loss Channel

This channel for this option will necessitate more equalization complexity, but the power consumption targets are relaxed.

- Channel = "T20". This channel is a 20" backplane with top traces (note via stub resonant behavior) plus ~6" of line card traces.

- The channel equalization may be done either in the mixed signal domain, some combination of TX FIR, RX FIR, CTLE, and DFE, **OR** partially digitally if an ADC-based front-end is used at the receiver
- Power efficiency should be <10mW/Gbps. The power total includes similar circuitry as option 1, the power of the serialization (4:1), de-serialization (1:4), driver, receiver front-end, and timing recovery. The power of a global TX PLL and clock distribution may be amortized by a factor of 16 with the assumption of a potential multi-channel system.
- This is an embedded clock plesiochronous system, with a separate clock crystal source on each card. This necessitates a tracking-CDR timing recover system.
- System crosstalk includes 1 NEXT and 1 FEXT aggressors.

Common Performance Specifications and Constraints

- **Min System BER of 10^{-12}.** This is the most critical high-level specification.

TX Performance Specifications and Constraints

- The following TX circuits should be implemented at the transistor level:
  - 4:1 mux. Note this can be implemented in either 1 or 2 stages.
  - All predriver circuitry
  - TX output stage
- TX equalization complexity and resolution should be justified via Stateye and/or Matlab simulations
- TX output impedance must be designed with a tuning range of ±30% from the optimal value.

RX Performance Specifications and Constraints

- The following RX circuits should be implemented at the transistor level:
  - Option 1 & 2(Non-ADC):
    - All mixed-signal equalization, ie RX FIR, CTLE, and/or DFE
    - Clocked comparators
    - Any additional de-multiplexing circuitry to provide a 4-bit 2.5Gb/s parallel received data stream
  - Option 2(ADC)
    - Any linear pre-amplifiers
    - If a time interleaved (TI) architecture is used, one “slice” or “sub-ADC” should be designed
- For clocked RX comparators, assume an input referred noise rms σ=1mV. In order to estimate the random input referred noise sigma, the total input referred noise should be calculated originating from the clocked comparators and input referring through any preceding linear amplification stages whose noise contributions should be included. For any linear amplifier stages that precede the clocked comparators, their input referred noise should be obtained via AC simulations.
- For the RX clocked comparators, and all linear pre-amplifiers that precede them, assume (optimistically) that their input offset is set by the differential pair sizing. The offset to design your system for is $\pm 3\sigma$. Note, this will have an impact on your receiver sensitivity. Offset calibration may be implemented to reduce this offset.

- RX input impedance must be designed with a tuning range of ±30% from the optimal value.
- RX equalization complexity and resolution should be justified via Stateye and/or Matlab simulations
- For option 2(ADC), the digital equalization can be coded via some type of HDL. Assume (very optimistically) that the digital logic can run at the same rate as the ADC output. For example, if you have a 4-way TI architecture, assume the logic can run at 2.5GHz. Note, it's OK if the ADC TI factor is greater than 4.

Clocking Performance Specifications and Constraints

- Option 1 clocking circuitry consists of:
  - TX PLL
  - TX & RX Clock Distribution. Clock distribution length should be sufficient for a 16-channel system.
  - A Potential RX Forwarded-Clock Amplifier
  - Per-channel RX De-skew Circuitry with the following potential architectures:
    - Delay-Locked Loop + Phase Interpolators
    - Injection-Locked Oscillator
- Option 2 clocking circuitry consists of:
  - TX PLL
  - TX Clock Distribution. Clock distribution length should be sufficient for a 16-channel system.
  - Per-channel RX CDR with the following potential architectures:
    - Per-Channel RX PLL-based CDR
    - Global RX PLL, clock distribution, and local per-channel Phase Interpolator (PI) loops
- The following clocking circuits should be implemented at the transistor level:
  - VCO in the TX PLL
  - **One** key RX clocking circuit, examples include
    - Injection-Locked Oscillator
    - Delay-Locked Loop (can be partially macro-modeled)
    - Phase Interpolator
- The remainder of the clocking circuitry can be macro-modeled.
- For PLL reference clocks, assume you have availability of crystal oscillators capable of operation between 1MHz to 300MHz, with 20ppm accuracy. This accuracy is important for option 2 with CDR-based timing, but not an issue we will worry about in option 1.

Tasks

The following items should be addressed for the project:

1. **Signaling convention**: How symbols are encoded into voltage or current and how the channel is driven, terminated, and received.
2. **Timing convention**: Overview of clocking system from global TX PLL, clock distribution, to RX timing recovery.
3. **Specification of Driver, Receiver, and Timing Circuits**: Define the necessary performance parameters that allow the link to achieve a BER=10^{-12}. This should be validated via a combination of Stateye, Matlab, and Circuit simulations.

To validate and evaluate your design you must perform the following analyses on it:

1. **Noise Budget**: Calculate all contributions to noise and interference and compute the differential eye height voltage margin for BER=10^{-12}. This should be validated with Stateye.
2. **Timing Budget**: Calculate all contributions to timing uncertainty and compute the net timing margin. This should be validated with Stateye.
3. **SPICE Simulation of Channel**: Transistor-level simulation from 4:1 mux, through driver, s-parameter channel, RX front-end, and de-mux. The input should be a PRBS source and verified by a PRBS verifier.
4. **Simulations to Confirm Timing Circuits Performance**: A combination of circuit, matlab, and Stateye simulations to validate the parameters that comprise the timing budget.

Important Dates

- April 16 Preliminary Report #1 with initial noise and timing budgets, estimates on equalization complexity, and initial simulations of driver and receiver circuits.
- April 23 Preliminary Report #2 with refined noise and timing budgets, current simulations of driver and receiver circuits, and initial simulations validating the clocking circuitry performance.
- May 4 Final Report Due
- May 10 Project Presentation (8:00-10:00AM). Email Prof. Palermo your presentation before 7AM.

Project Grading*

- Preliminary Report #1 10%
- Preliminary Report #2 10%
- Report and Presentation
  - Completeness of the design 30%
  - Robustness of the design 10%
  - Creativity and elegance of the design 10%
  - Completeness of the analysis 20%
  - Clarity of report and presentation 10%

*Note that all components are necessary to get any credit for the project.

Extra-Credit Opportunities.

A maximum of 20% extra-credit can be obtained on the project if an excellent job is done on the following. Each item is worth approximately 10%.

- Suggest something of your interest
- Best power efficiency for Option #1.
- Implement spread-spectrum clocking
- TX impedance control feedback loop
- ADC with embedded equalization
- ADC automatic gain control
- Resonant clock distribution
- Bandpass filtering of forwarded-clock
- Adaptive supply-scaling techniques for low-power I/O