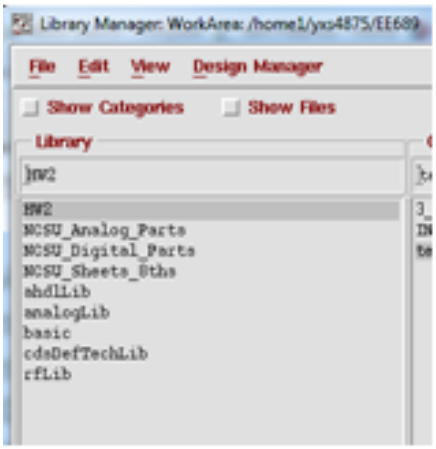
PRBS generation and Return Loss simulation

EE689 High Speed I/O

Dr Samuel Palermo

Library Setting

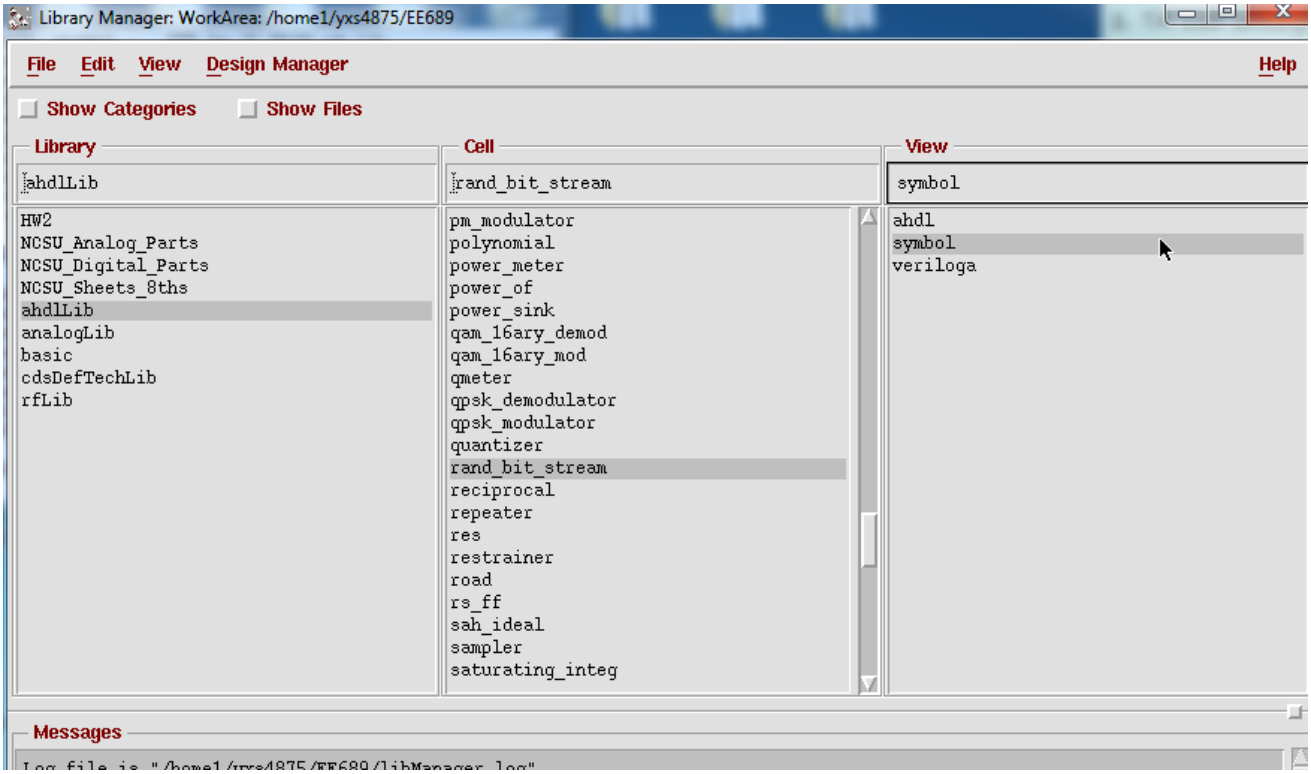
Make Sure you see the ahdlLib and rfLib in library Manager

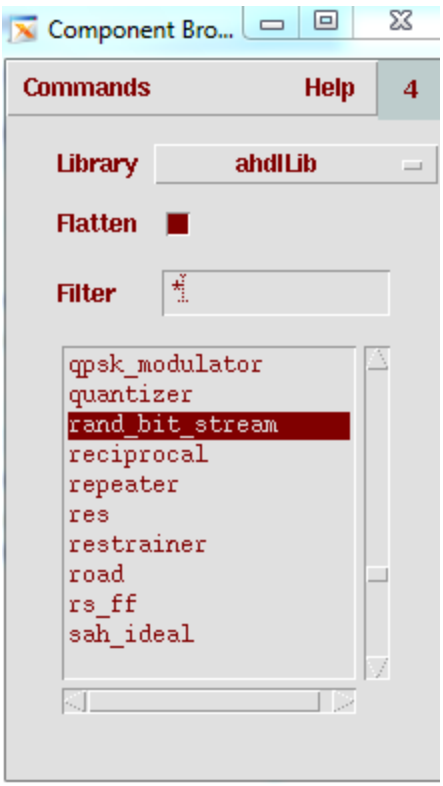


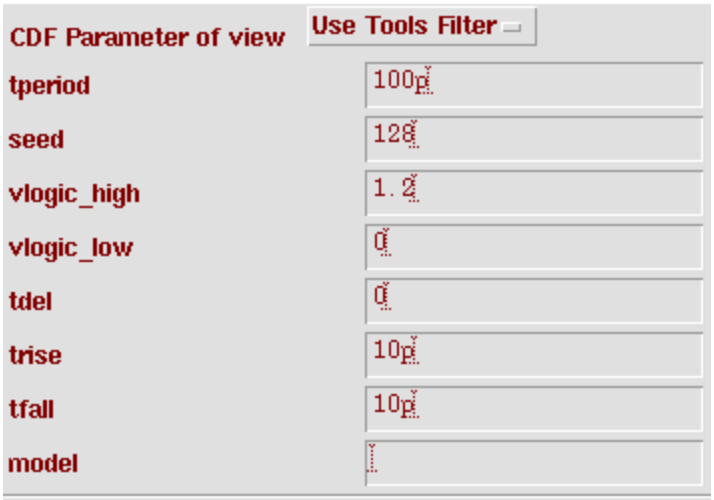

```
eesun1:/home1/yxs4875/EE689>cat cds.lib
INCLUDE /baby/cadence/ic50/local/cdssetup/cds.lib

DEFINE rfLib $CDS_INST_DIR/tools/dfII/samples/artist/rfLib
DEFINE ahdlLib $CDS_INST_DIR/tools/dfII/samples/artist/ahdlLib
DEFINE analogLib $CDS/tools/dfII/etc/cdslib/artist/analogLib
DEFINE HW2 /home1/yxs4875/EE689/HW2
eesun1:/home1/yxs4875/EE689>
```

PRBS Generator

We can find the rand_bit_stream in ahdlLib to generate prbs.
For setting, Tperiod is your 1UI time, and more detail we can see figures.

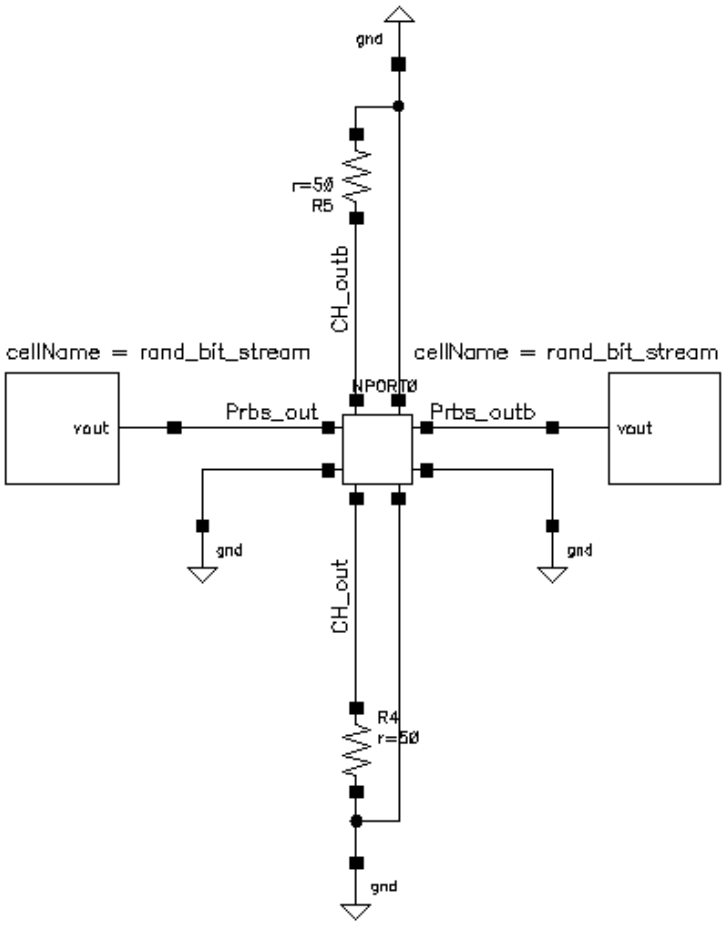


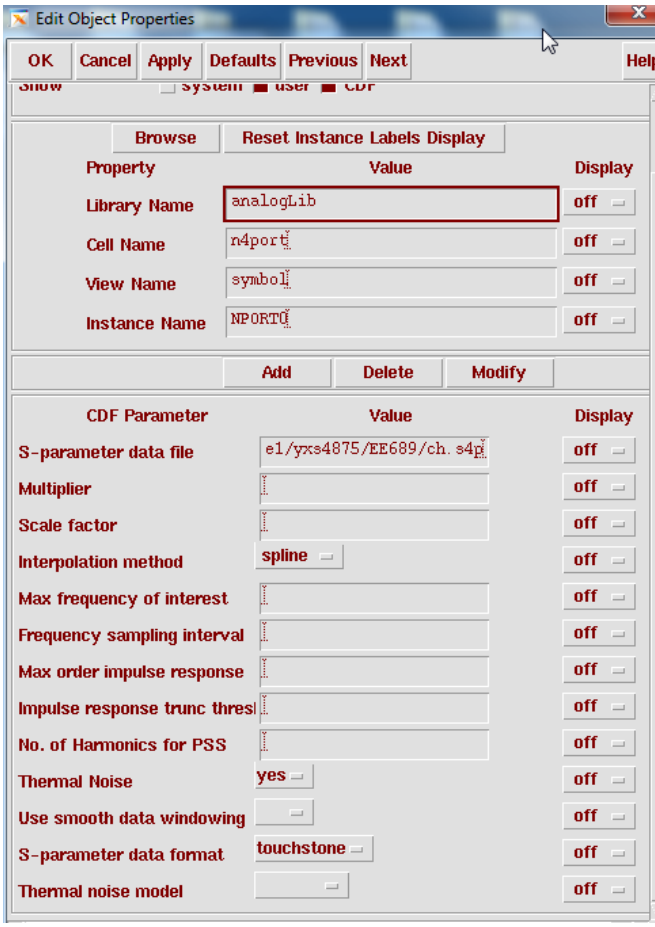




PRBS Generator + Channel

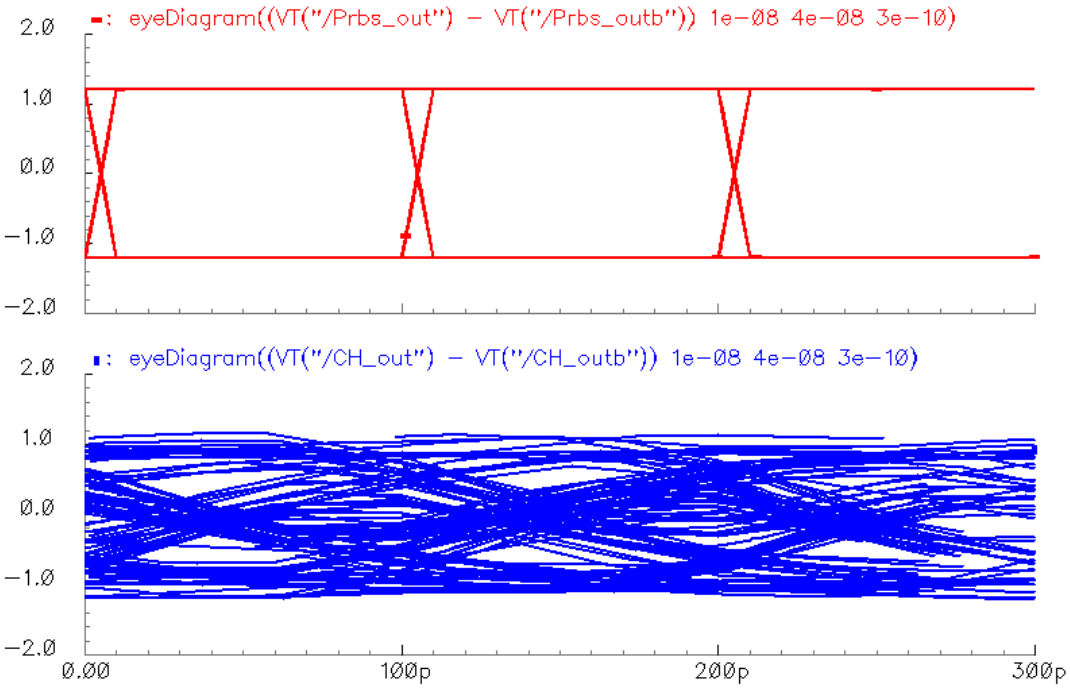
❑ Test bench for Transient Simulation with *.s4p files



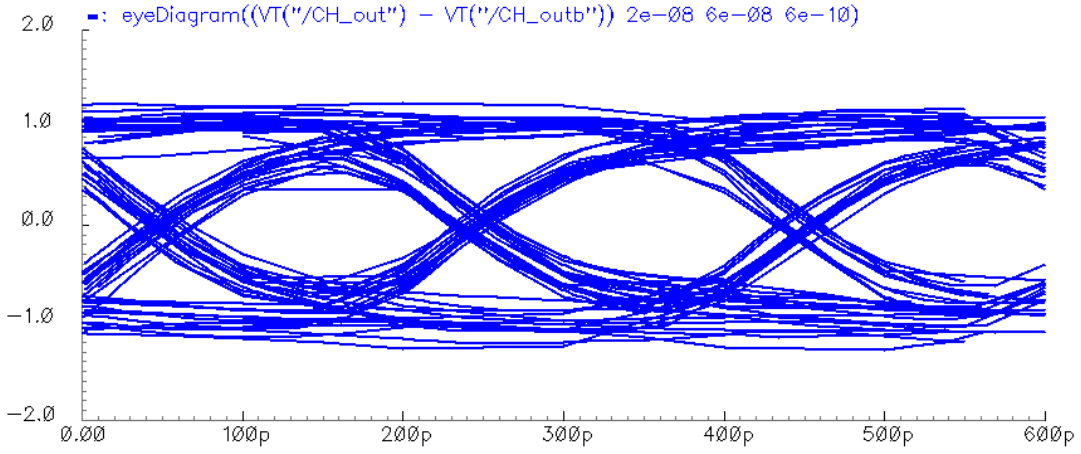


To do transient simulation with touchstone file, we need to n4port model in analogLib.
Actually channel name is peters_01_0605_B14_thru.s4p which you can download in class web site, but I change the name ch.s4p for convenient in here. Port 1 and 3 will be input and port 2 and 4 are output.
We have to terminate with 50 ohms resistor in the output port.

❑ 10Gbs


eyeDiagram((VT("/Prbs_out") – VT("/Prbs_outb")) 1e–08 4e–08 3e–10)
2.0
1.0
0.0
–1.0
–2.0
eyeDiagram((VT("/CH_out") – VT("/CH_outb")) 1e–08 4e–08 3e–10)
2.0
1.0
0.0
–1.0
–2.0
0.00
100p
200p
300p

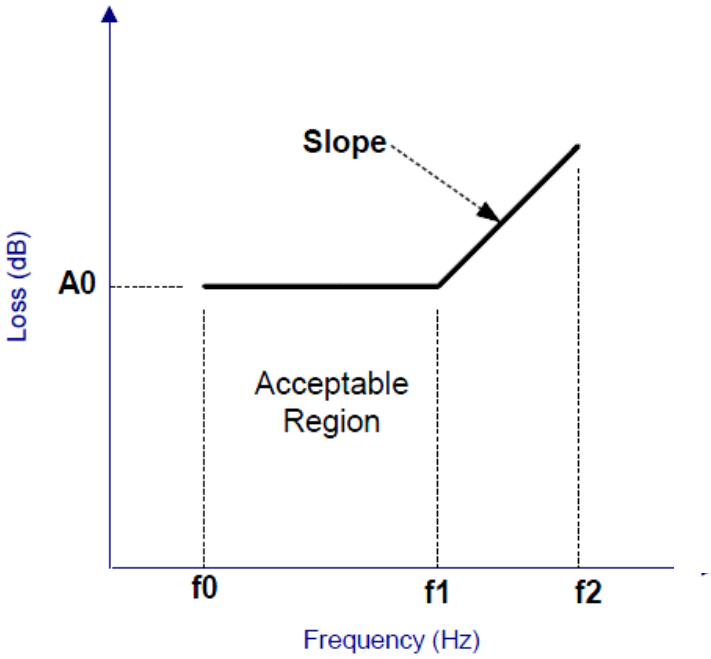
❑ 5Gbs


eyeDiagram((VT("/CH_out") – VT("/CH_outb")) 2e–08 6e–08 6e–10)
2.0
1.0
0.0
–1.0
–2.0
0.00
100p
200p
300p
400p
500p
600p

High Frequency Diff mode Return Loss

- Increased signal integrity
- Some standards require high performance RL Specification

Driver and input differential return loss – CEI – SR short reach interface

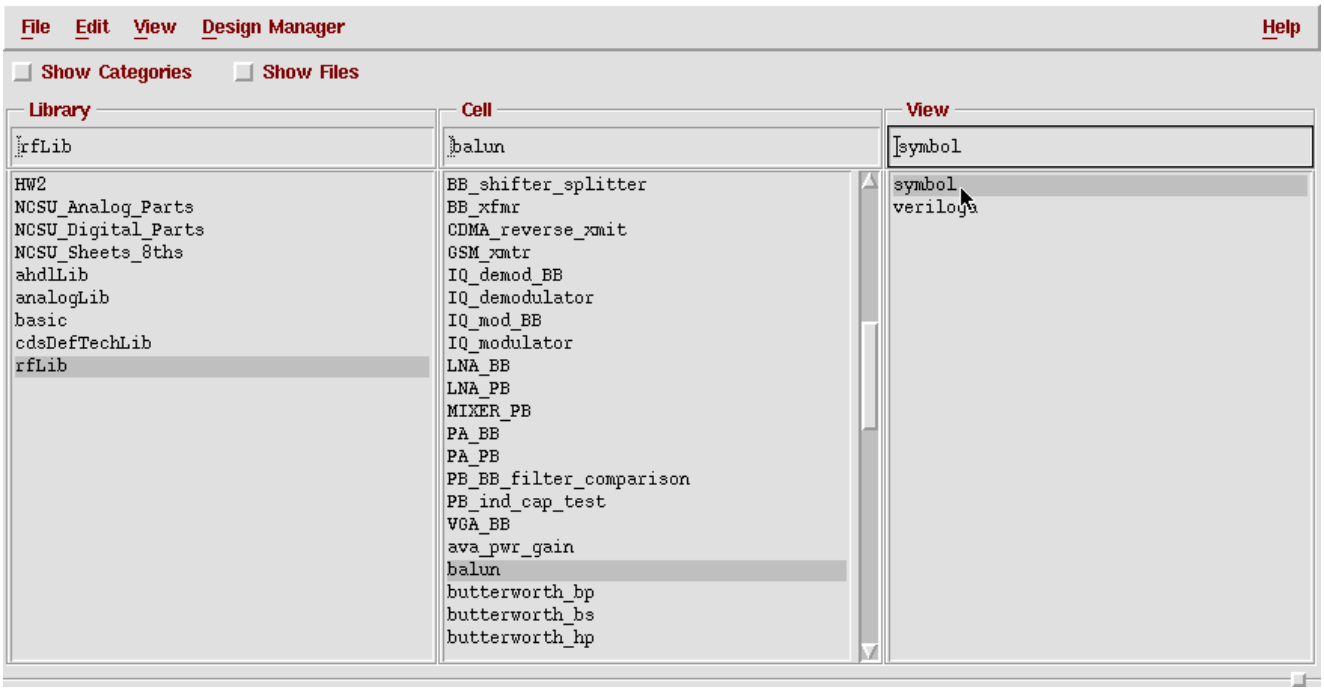


Parameter	Value	Units
A0	-8	dB
f0	100	MHz
f1	$T\_Baud \times \frac{3}{4}$	Hz
f2	$T\_Baud \times \frac{3}{2}$	Hz
Slope	16.6	dB/dec

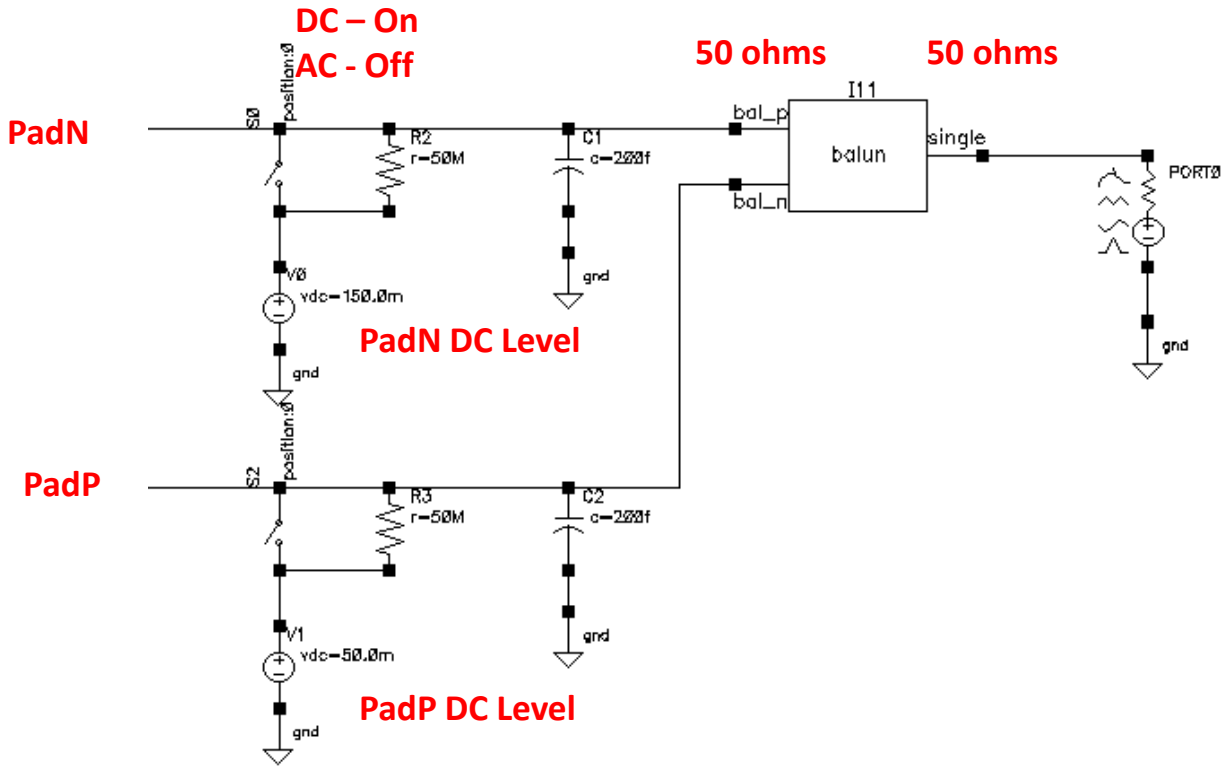
The differential return loss shall be better than A0 from f0 to f1 and better than A0 + Slope*log10(f/f1) where f is the frequency from f1 to f2.

Ref : OIF-CEI-02.0 Stateye www.stateye.org

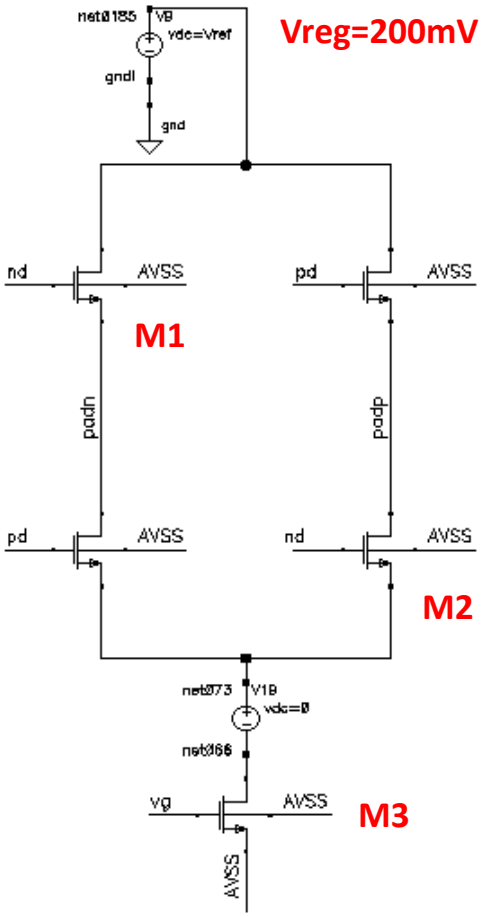
Library for Balun

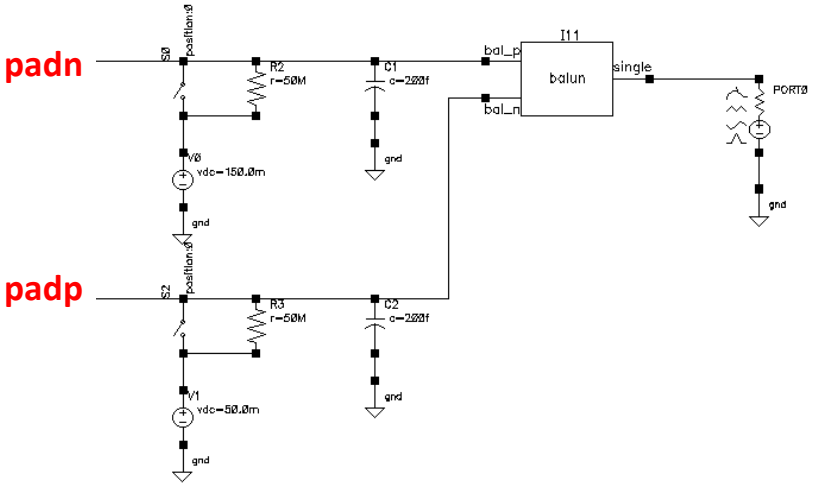


Test bench for RL measurement



Voltage mode RL measurement





When nd is high, TR M1 sets 50ohm termination Resistor, and both M2 and M3 set 50ohm termination Resistor. As we can see, RL performance degrade at high frequency due to pad cap and parasitic cap.