ECEN720: High-Speed Links Circuits and Systems Spring 2025

Lecture 8: RX FIR, CTLE, DFE, & Adaptive Eq.

Sam Palermo
Analog & Mixed-Signal Center
Texas A&M University

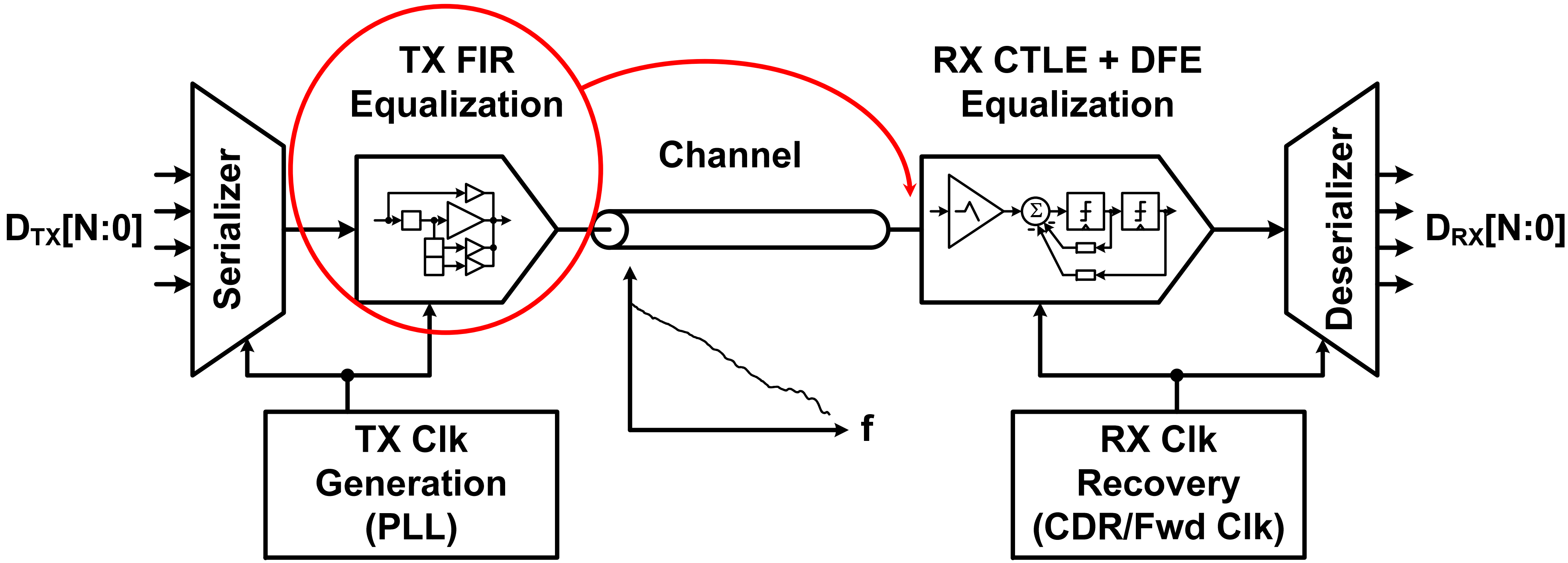
Announcements

- Lab Report 5 and Prelab 6 due Mar 25
- Equalization overview and circuits papers are posted on the website

Agenda

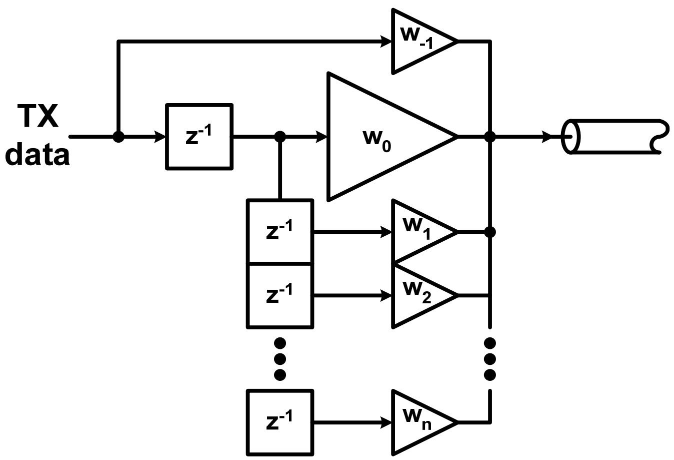
- RX FIR equalization
- RX CTLE equalization
- RX DFE equalization
- Equalization adaptation techniques
- Advanced modulation/other techniques

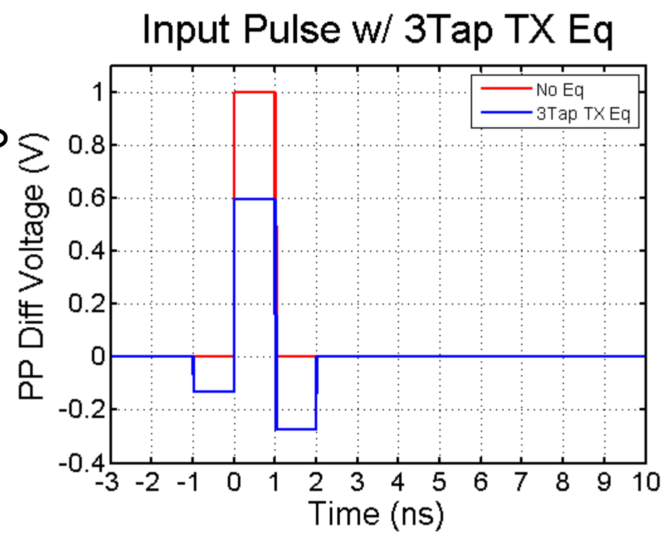
Link with Equalization

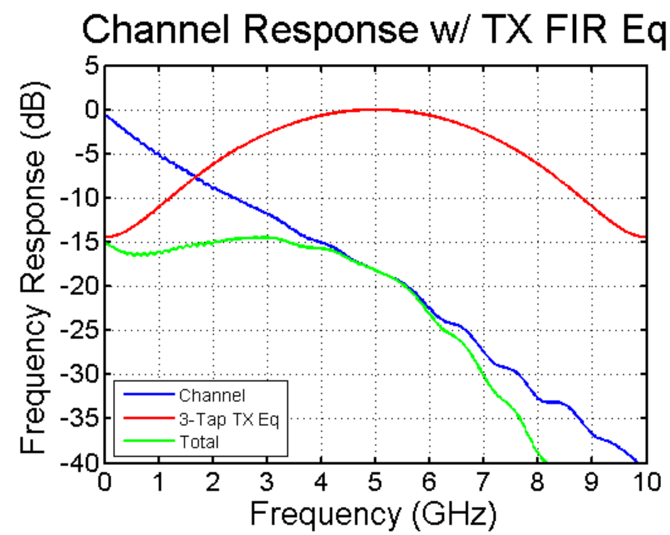


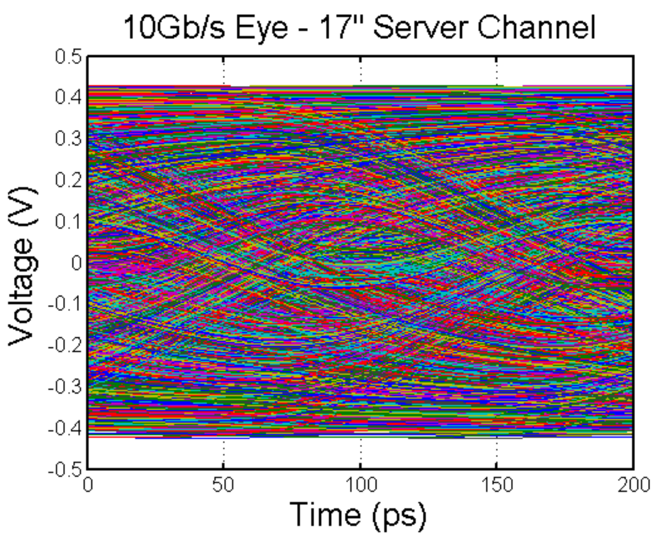
TX FIR Equalization

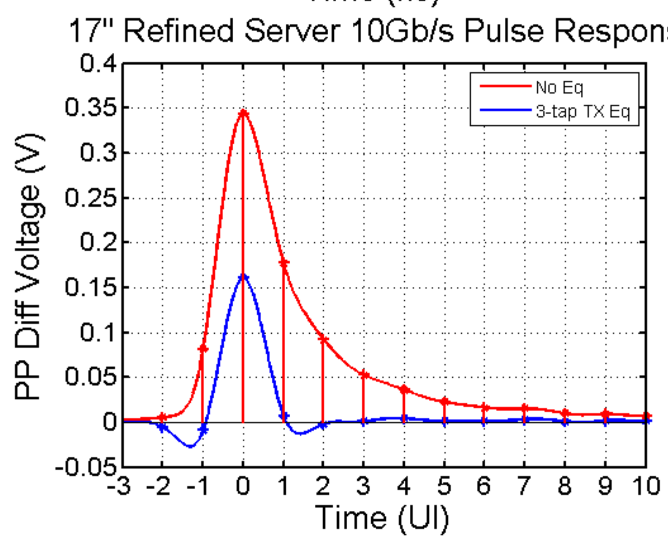
- TX FIR filter pre-distorts transmitted pulse in order to invert channel distortion at the cost of attenuated transmit signal (de-emphasis)

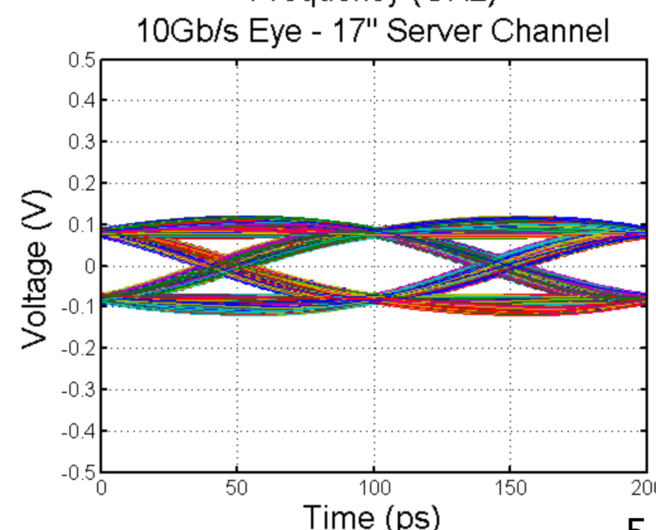






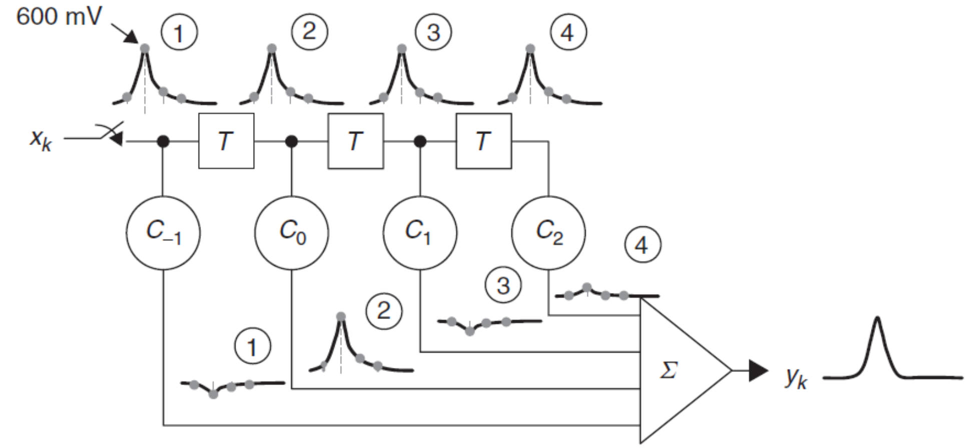


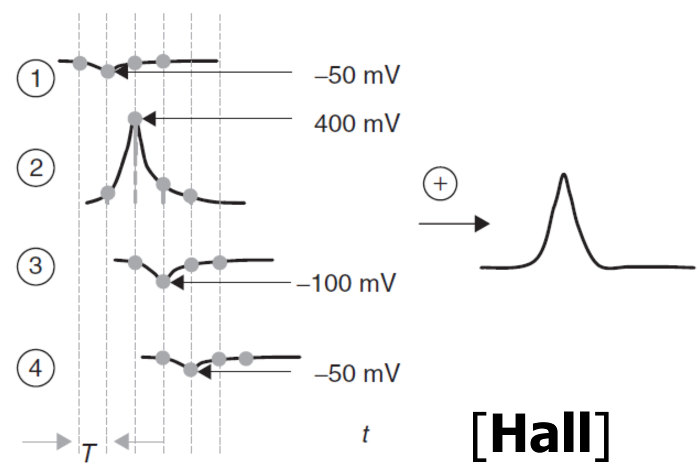




RX FIR Equalization

- Delay analog input signal and multiply by equalization coefficients
- Pros
  - With sufficient dynamic range, can amplify high frequency content (rather than attenuate low frequencies)
  - Can cancel ISI in pre-cursor and beyond filter span
  - Filter tap coefficients can be adaptively tuned without any back-channel
- Cons
  - Amplifies noise/crosstalk
  - Implementation of analog delays
  - Tap precision

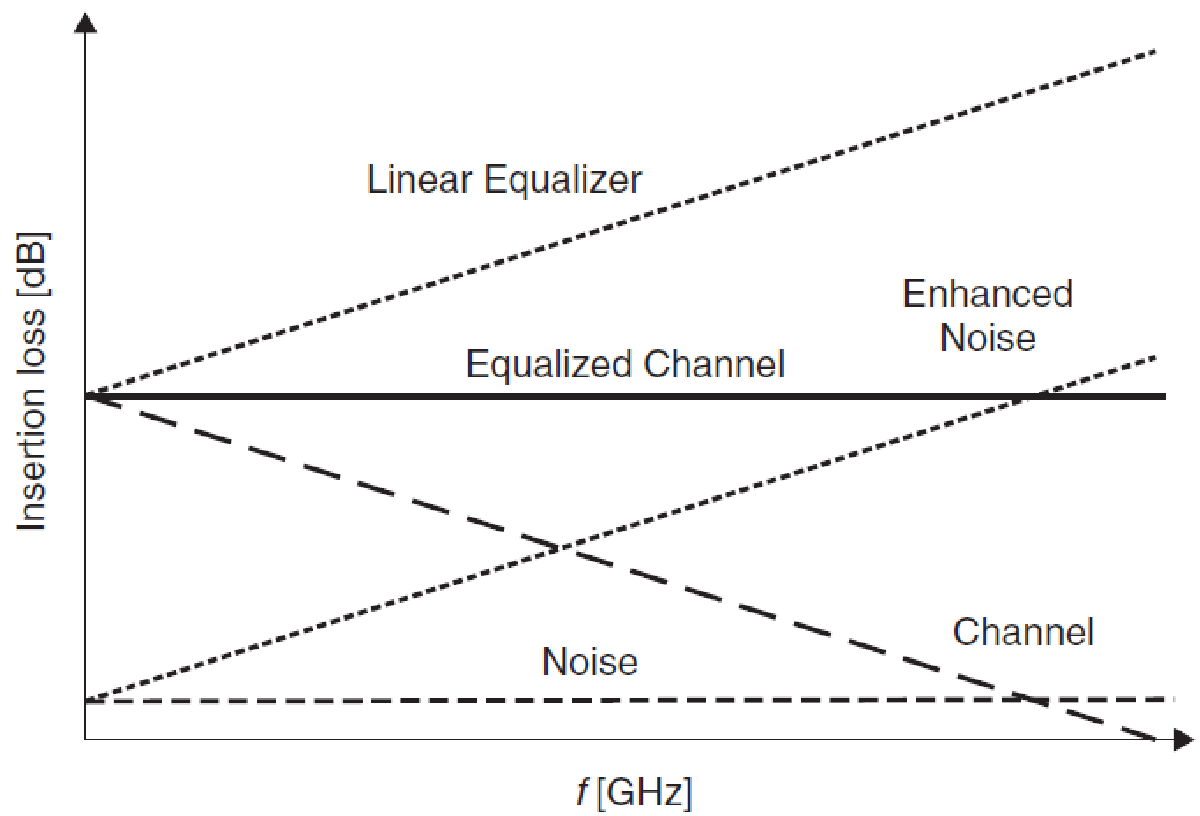




[**Hall**]

RX Equalization Noise Enhancement

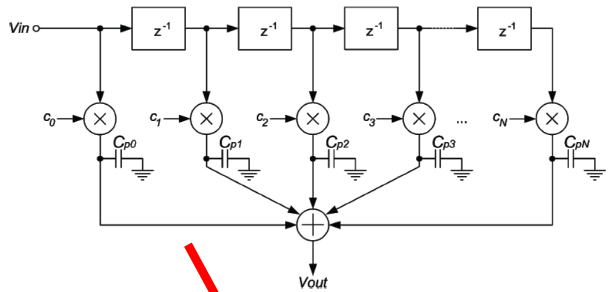
- Linear RX equalizers don't discriminate between signal, noise, and cross-talk
  - While signal-to-distortion (ISI) ratio is improved, SNR remains unchanged

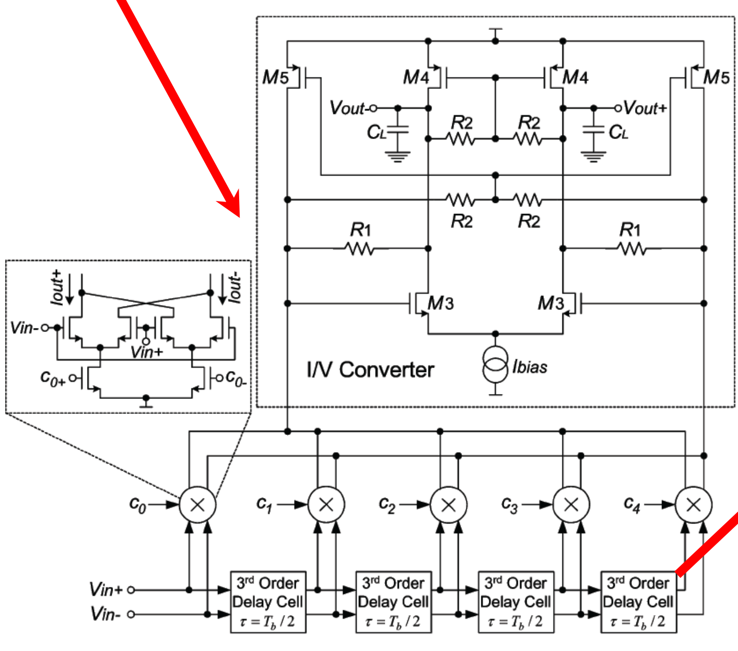


[**Hall**]

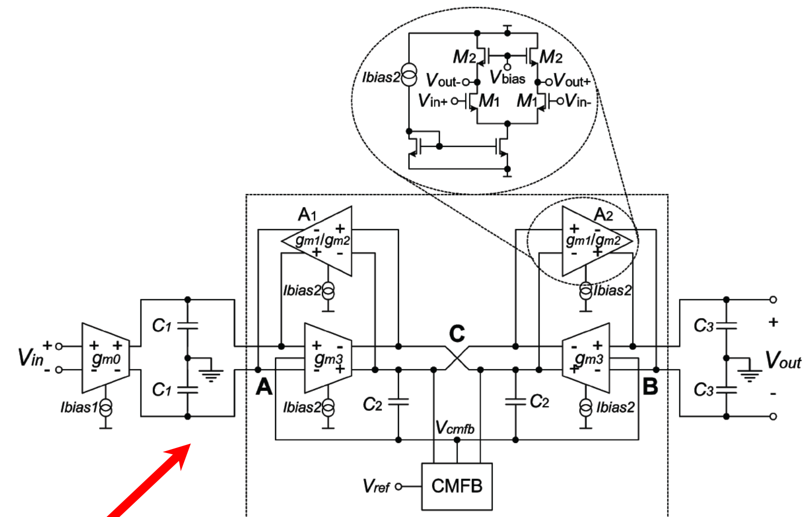
Analog RX FIR Equalization Example

- 5-tap equalizer with tap spacing of $T_b/2$

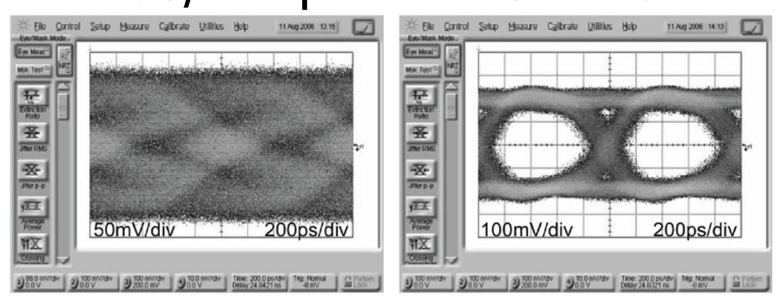




3rd-order delay cell



1Gb/s experimental results

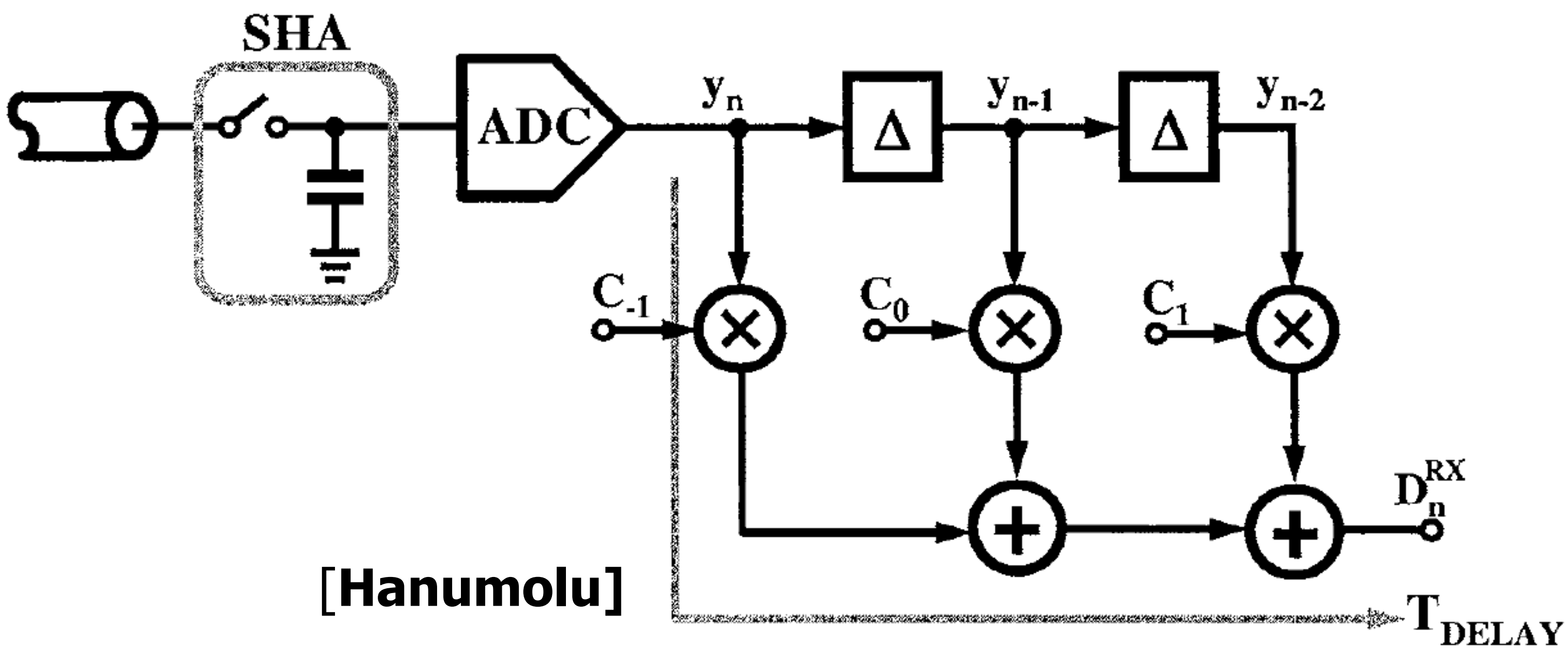


Before Equalizer: 23meters　After Equalizer: 23meters

D. Hernandez-Garduno and J. Silva-Martinez, “A CMOS 1Gb/s 5-Tap Transversal Equalizer based on 3rd-Order Delay Cells," ISSCC, 2007.

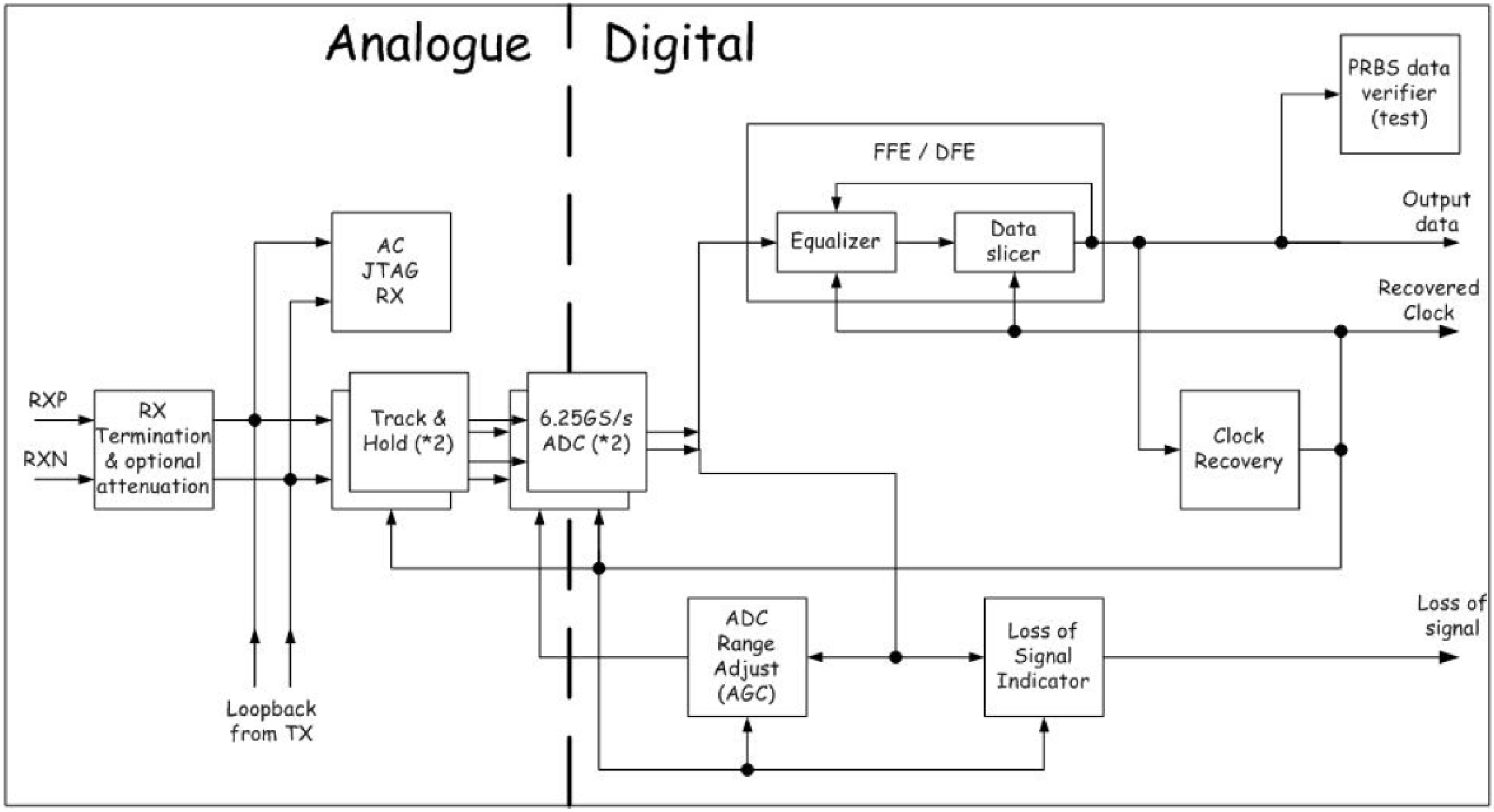
Digital RX FIR Equalization

- Digitize the input signal with high-speed low/medium resolution ADC and perform equalization in digital domain
  - Digital delays, multipliers, adders
  - Limited to ADC resolution
- Power can be high due to very fast ADC and digital filters



[Hanumolu]

Digital RX FIR Equalization Example

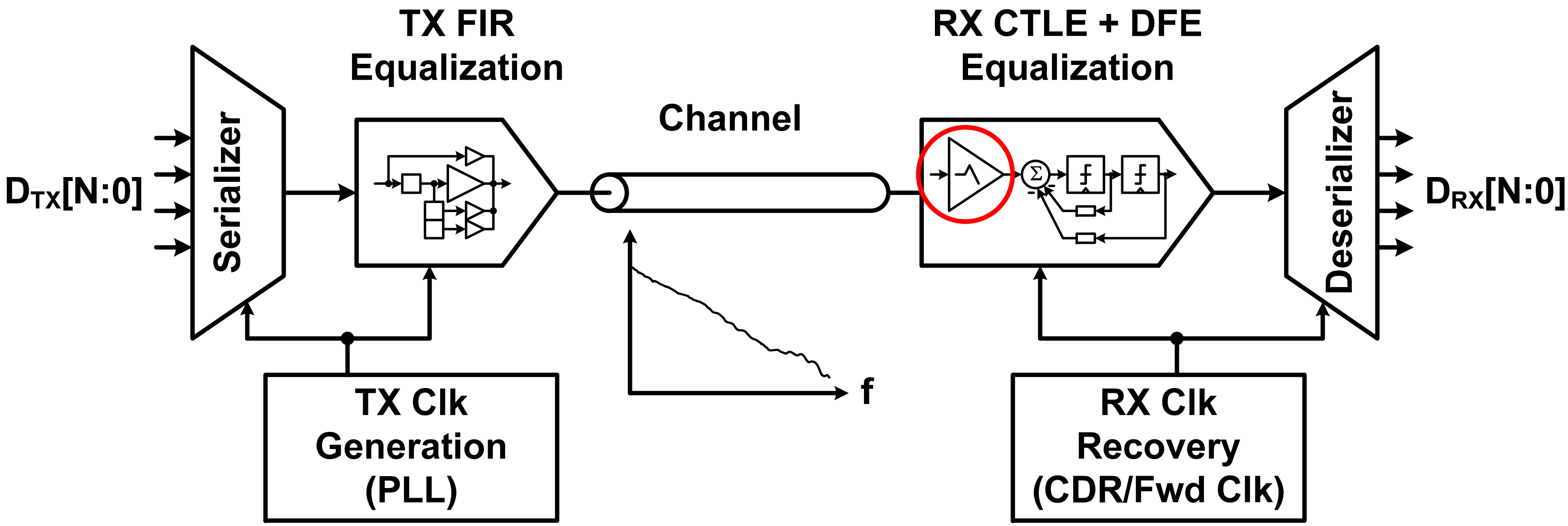


- 12.5GS/s 4.5-bit Flash ADC in 65nm CMOS [**Harwood ISSCC 2007**]
- 2-tap FFE & 5-tap DFE
- XCVR power (inc. TX) = 330mW, Analog = 245mW, Digital = 85mW

Agenda

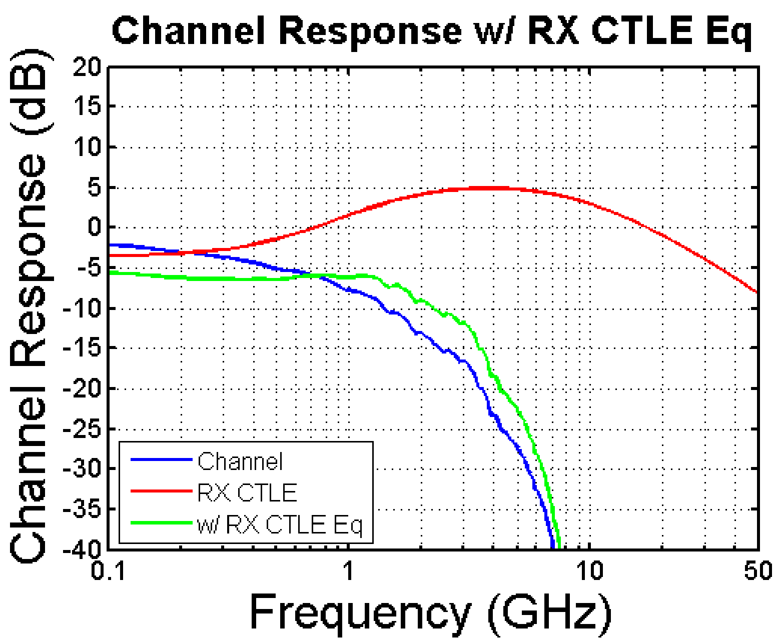
- RX FIR equalization
- RX CTLE equalization
- RX DFE equalization
- Equalization adaptation techniques
- Advanced modulation/other techniques

Link with Equalization

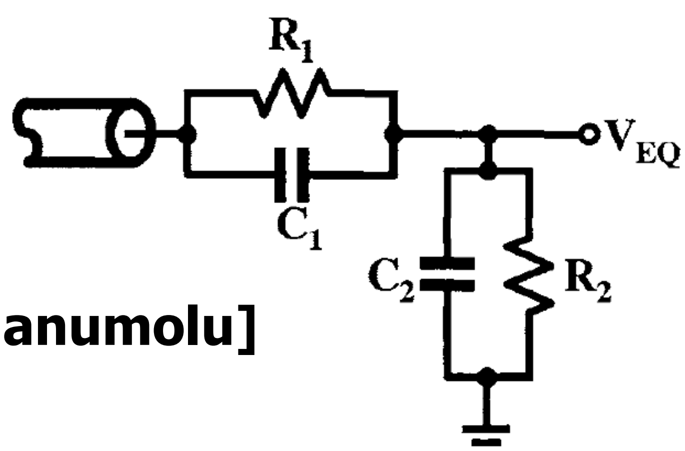


RX Continuous-Time Linear Equalizer (CTLE)

- Passive R-C (or L) can implement high-pass transfer function to compensate for channel loss
- Cancel both precursor and long-tail ISI
- Can be purely passive or combined with an amplifier to provide gain

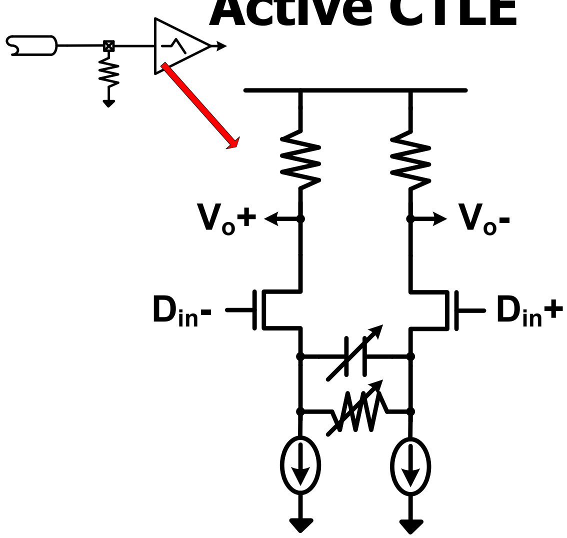


Passive CTLE



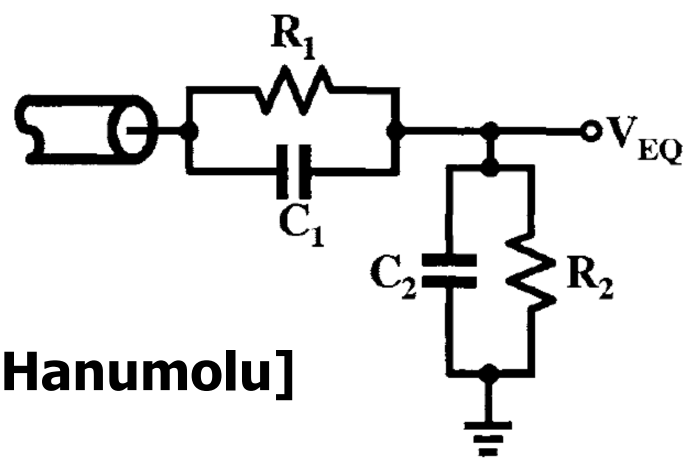
[Hanumolu]

Active CTLE



Passive CTLE

- Passive structures offer excellent linearity, but no gain at Nyquist frequency



[Hanumolu]

$$H(s) = \frac{R_2}{R_1 + R_2} \frac{1 + R_1 C_1 s}{1 + \frac{R_1 R_2}{R_1 + R_2}(C_1 + C_2)s}$$

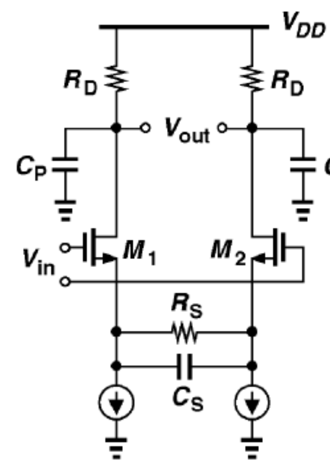
$$\omega_z = \frac{1}{R_1 C_1}, \qquad \omega_p = \frac{1}{\frac{R_1 R_2}{R_1 + R_2}(C_1 + C_2)}$$

$$\textbf{DC gain} = \frac{R_2}{R_1 + R_2}, \quad \textbf{HF gain} = \frac{C_1}{C_1 + C_2}$$

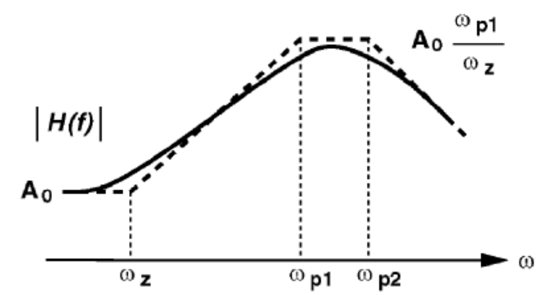
$$\textbf{Peaking} = \frac{\textbf{HF gain}}{\textbf{DC gain}} = \frac{\omega_p}{\omega_z} = \frac{R_1 + R_2}{R_2} \frac{C_1}{C_1 + C_2}$$

Active CTLE

- Input amplifier with RC degeneration can provide frequency peaking with gain at Nyquist frequency
- Potentially limited by gain-bandwidth of amplifier
- Amplifier must be designed for input linear range
  - Often TX eq. provides some low frequency attenuation
- Sensitive to PVT variations and can be hard to tune
- Generally limited to 1st-order compensation



[Gondi JSSC 2007]



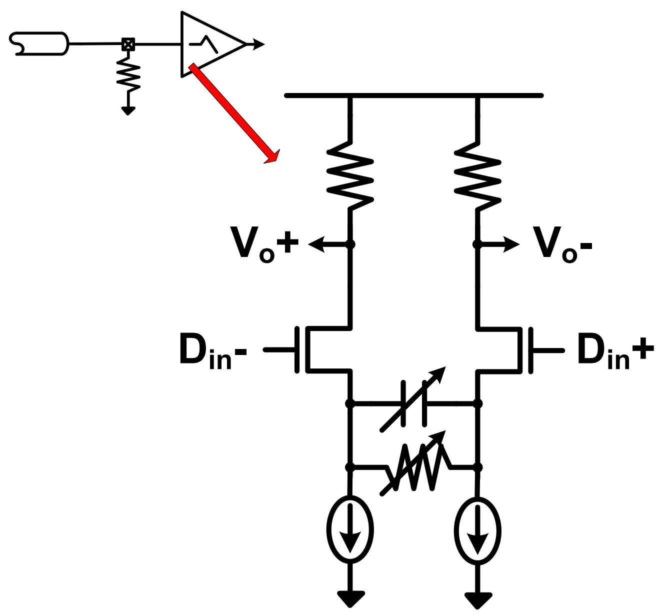
$$H(s) = \frac{g_m}{C_p} \frac{s + \frac{1}{R_S C_S}}{\left(s + \frac{1 + g_m R_S/2}{R_S C_S}\right)\left(s + \frac{1}{R_D C_p}\right)}$$

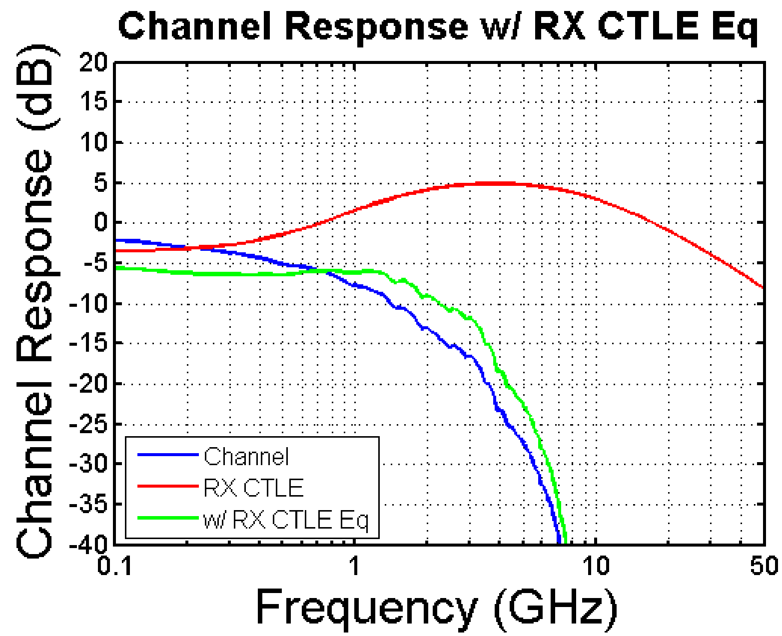
$$\omega_z = \frac{1}{R_S C_S}, \quad \omega_{p1} = \frac{1 + g_m R_S/2}{R_S C_S}, \quad \omega_{p2} = \frac{1}{R_D C_p}$$

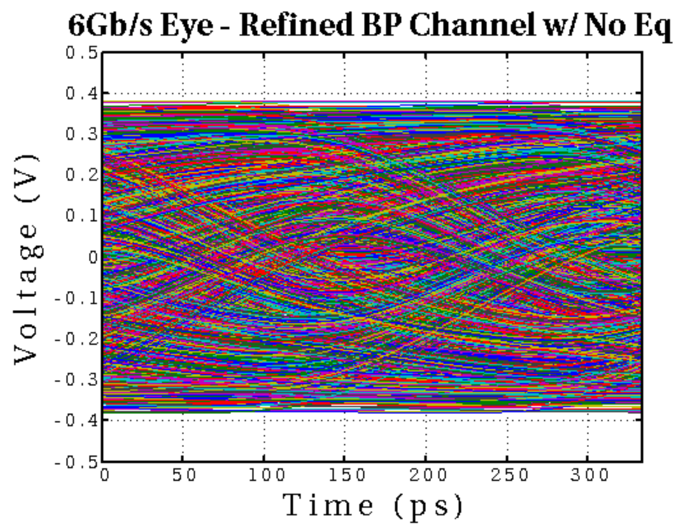
$$\text{DC gain} = \frac{g_m R_D}{1 + g_m R_S/2}, \quad \text{Ideal peak gain} = g_m R_D$$

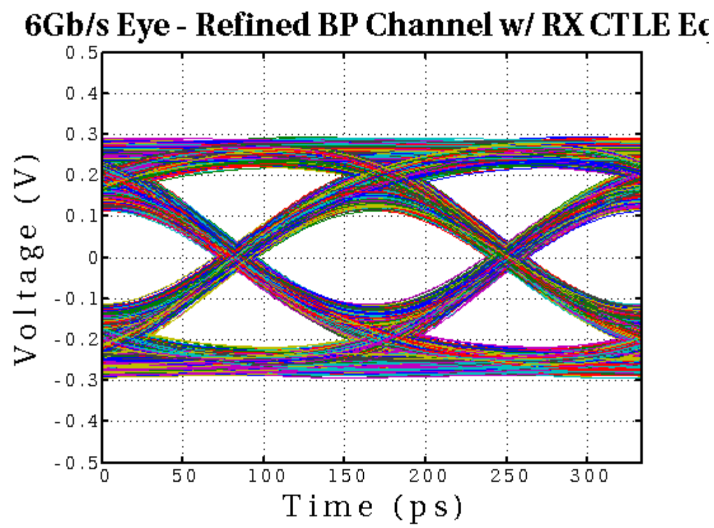
$$\text{Ideal Peaking} = \frac{\text{Ideal peak gain}}{\text{DC gain}} = \frac{\omega_{p1}}{\omega_z} = 1 + g_m R_S/2$$

Active CTLE Example







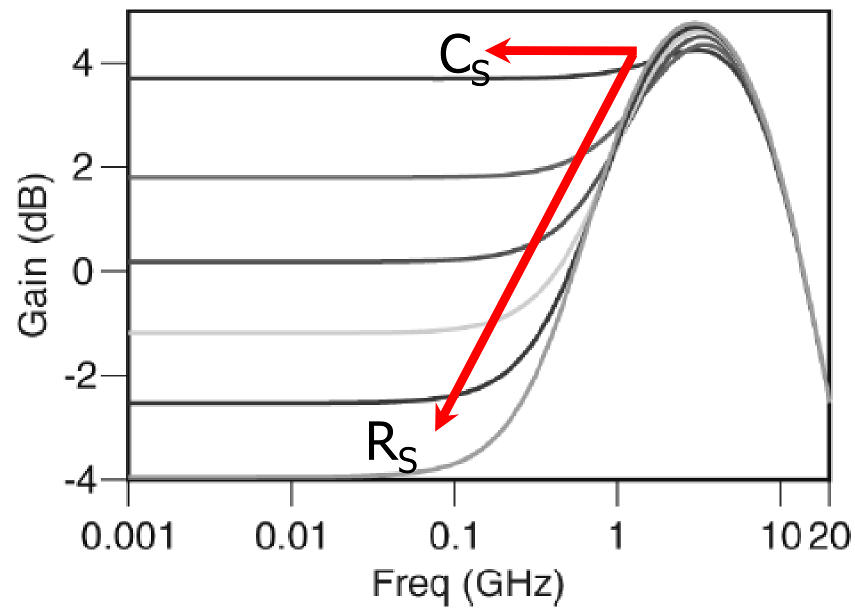


Active CTLE Tuning

- Tune degeneration resistor and capacitor to adjust zero frequency and 1st pole which sets peaking and DC gain

- Increasing C_S moves zero and 1st pole to a lower frequency w/o impacting (ideal) peaking

- Increasing R_S moves zero to lower frequency and increases peaking (lowers DC gain)
    - Minimal impact on 1st pole



$$\omega_z = \frac{1}{R_S C_S}, \quad \omega_{\mathbf{p1}} = \frac{1 + g_m R_S/2}{R_S C_S}$$

Agenda

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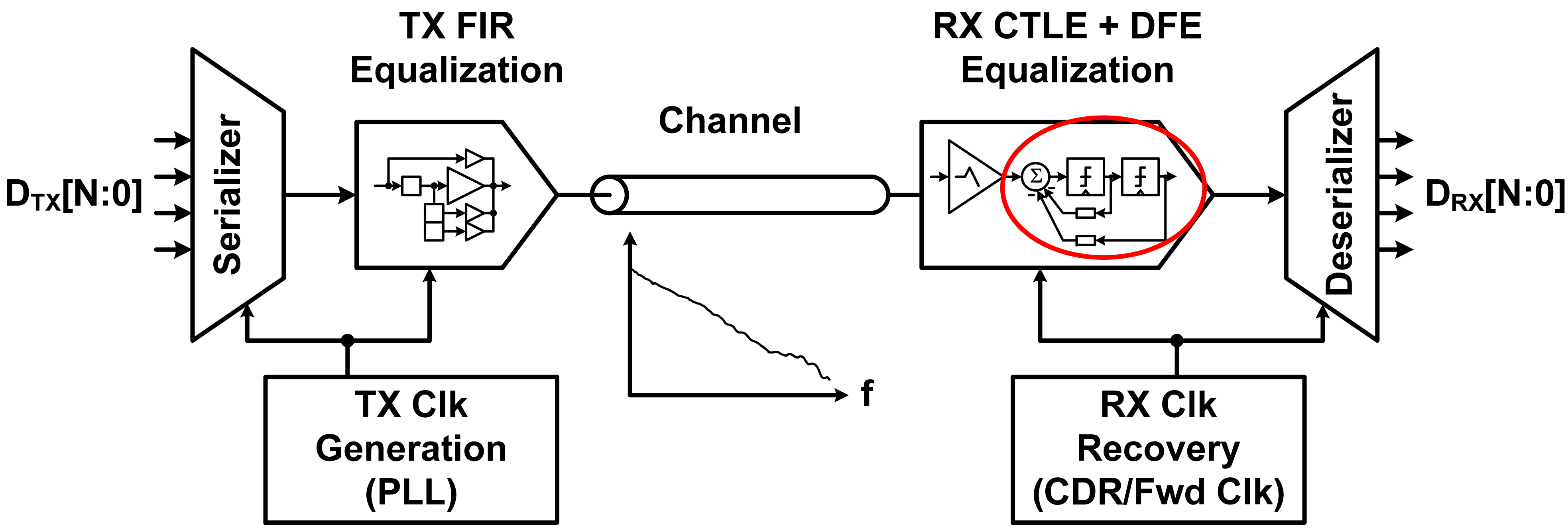
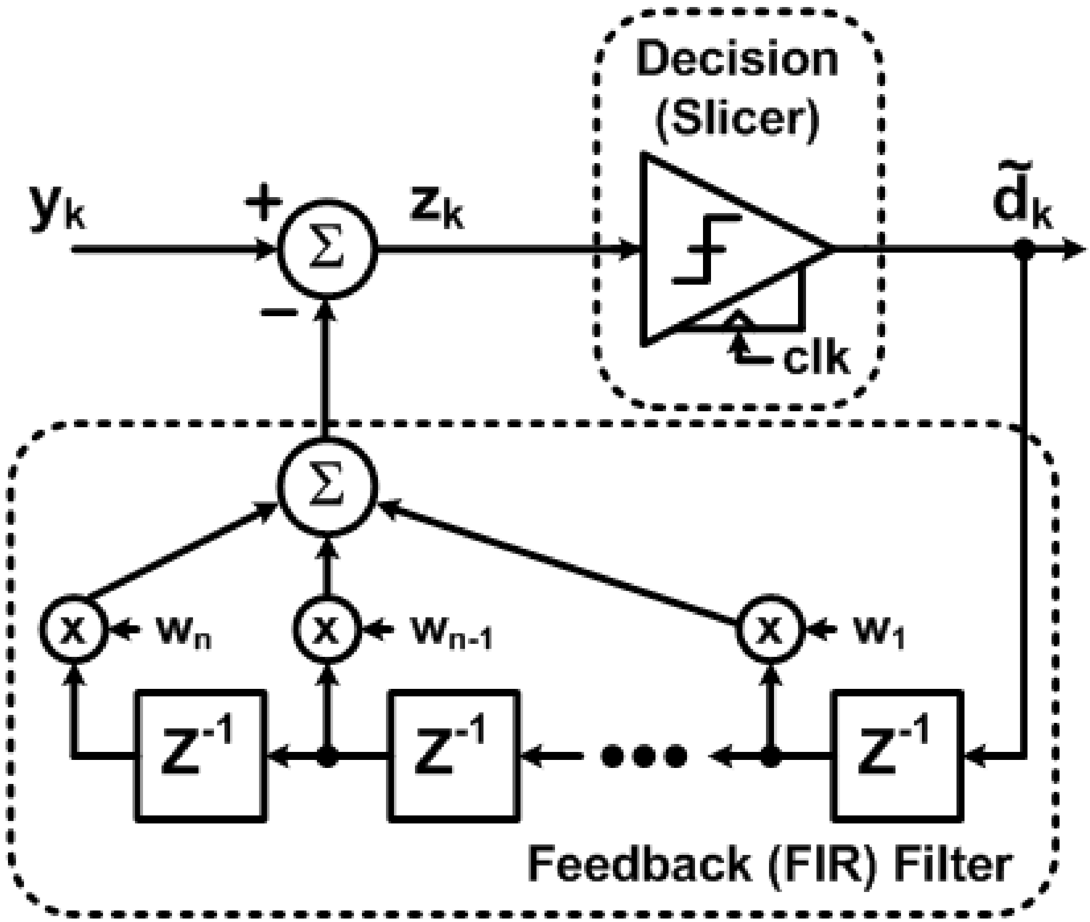
Link with Equalization



RX Decision Feedback Equalization (DFE)

- DFE is a **non-linear** equalizer
- Slicer makes a **symbol decision**, i.e. quantizes input
- ISI is then directly subtracted from the incoming signal via a feedback FIR filter

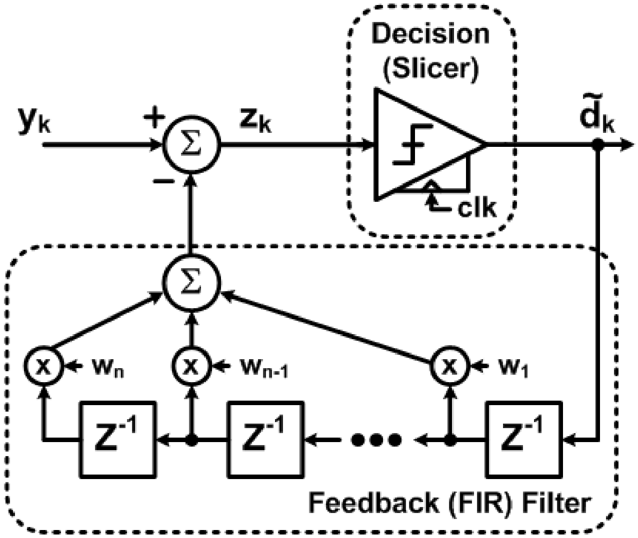
$$z_k = y_k - w_1 \tilde{d}_{k-1} \cdots - w_{n-1} \tilde{d}_{k-(n-1)} - w_n \tilde{d}_{k-n}$$

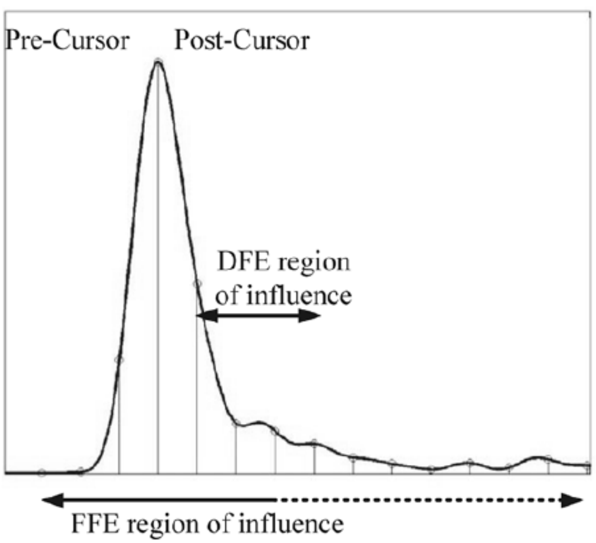


RX Decision Feedback Equalization (DFE)

- Pros
  - Can boost high frequency content without noise and crosstalk amplification
  - Filter tap coefficients can be adaptively tuned without any back-channel
- Cons
  - Cannot cancel pre-cursor ISI
  - Chance for error propagation
    - Low in practical links ($BER=10^{-12}$)
  - Critical feedback timing path
  - Timing of ISI subtraction complicates CDR phase detection

$$z_k = y_k - w_1 \tilde{d}_{k-1} \cdots - w_{n-1} \tilde{d}_{k-(n-1)} - w_n \tilde{d}_{k-n}$$

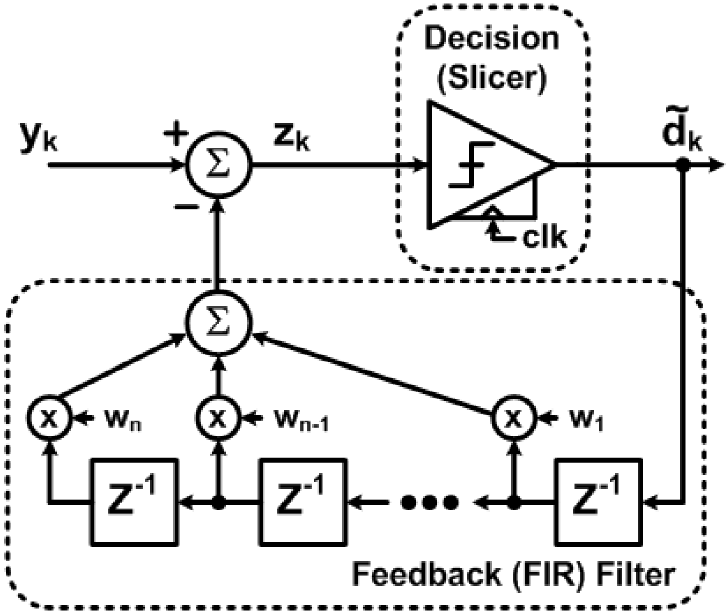




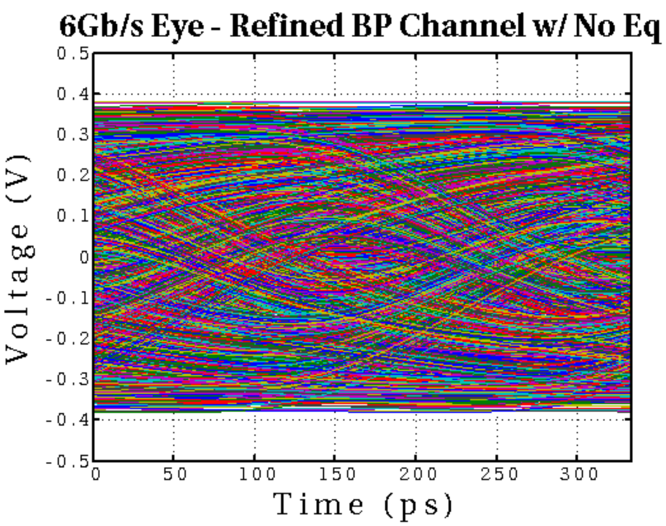
[Payne]

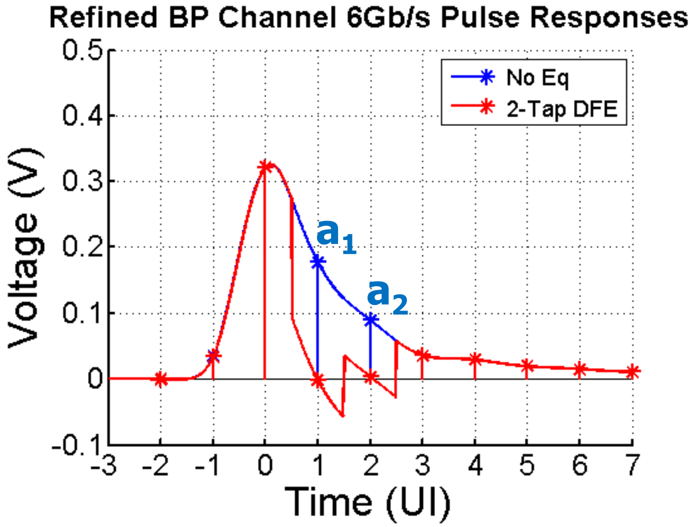
DFE Example

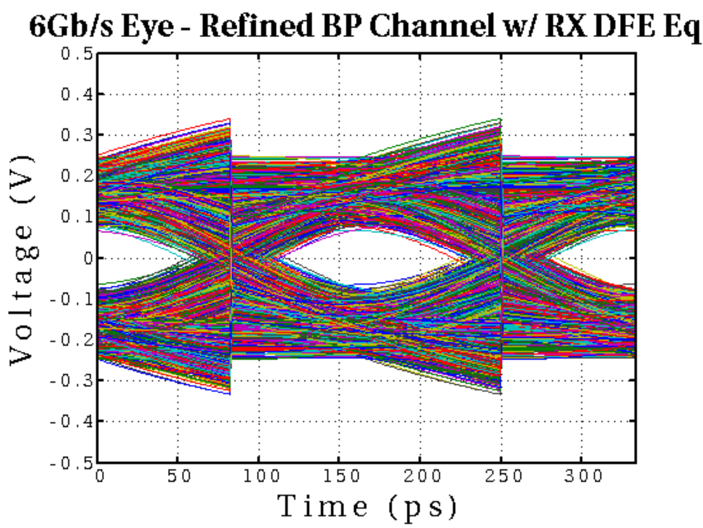
- If only DFE equalization, DFE tap coefficients should equal the unequalized channel pulse response values $[a_1\ a_2\ \ldots\ a_n]$
- With other equalization, DFE tap coefficients should equal the pre-DFE pulse response values
  - DFE provides flexibility in the optimization of other equalizer circuits
  - i.e., you can optimize a TX equalizer without caring about the ISI terms that the DFE will take care of



$[w_1\ w_2]=[a_1\ a_2]$

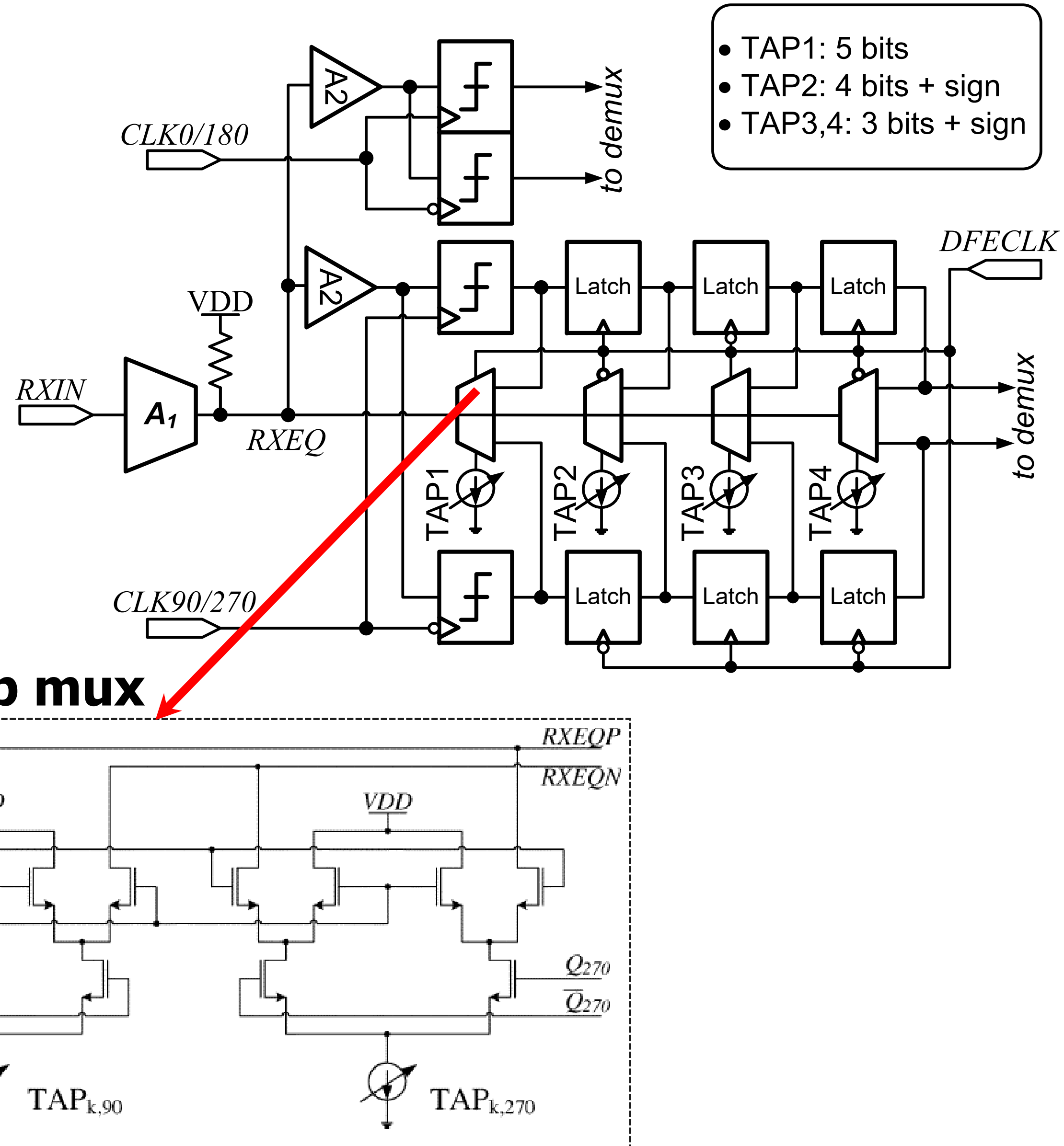






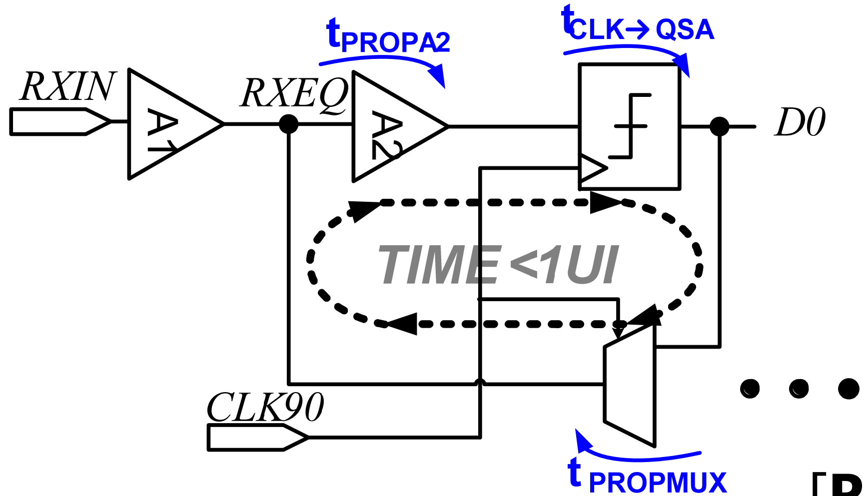
Direct Feedback DFE Example (TI)

- 6.25Gb/s 4-tap DFE
  - ½ rate architecture
  - Adaptive tap algorithm
  - Closes timing on 1st tap in **½ UI** for convergence of both adaptive equalization tap values and CDR

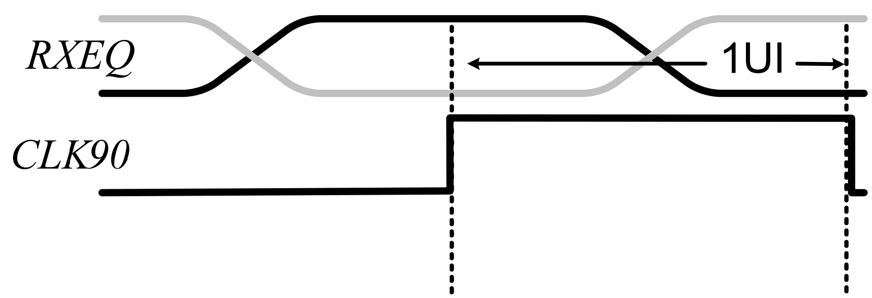


R. Payne *et al*, "A 6.25-Gb/s Binary Transceiver in 0.13-um CMOS for Serial Data Transmission Across High Loss Legacy Backplane Channels," *JSSC*, vol. 40, no. 12, Dec. 2005, pp. 2646-2657

Direct Feedback DFE Critical Path



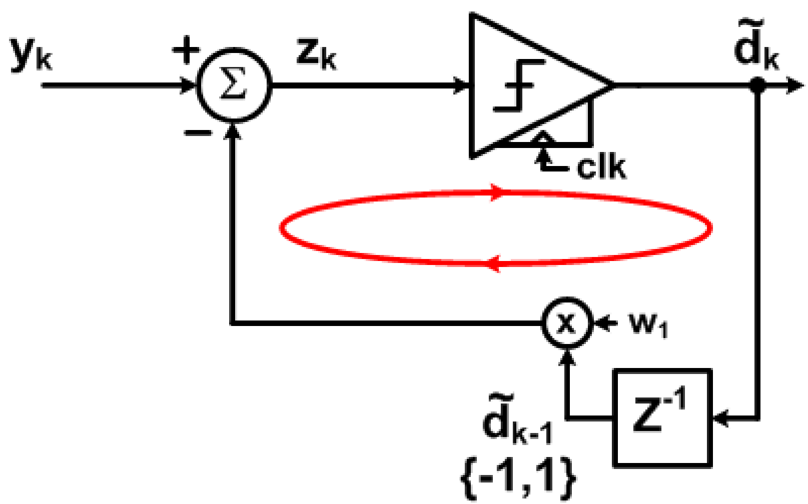
[Payne]

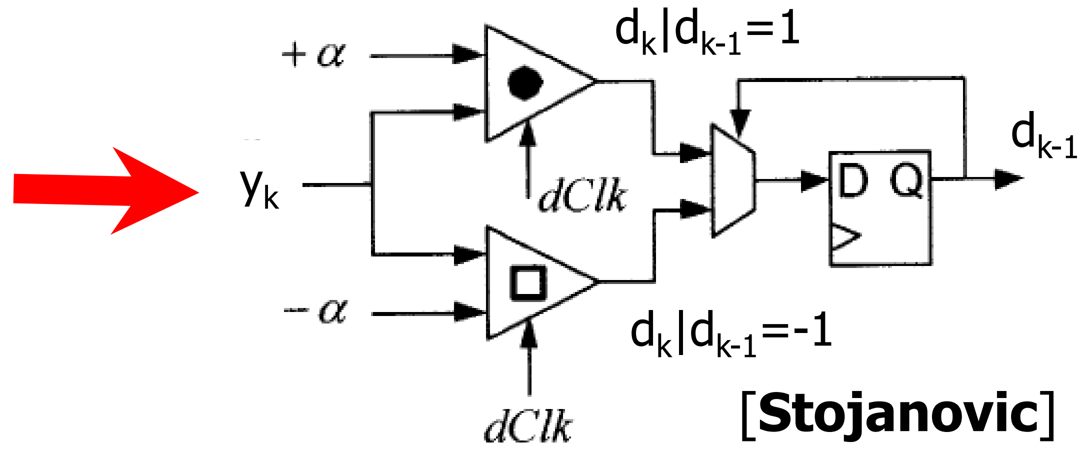


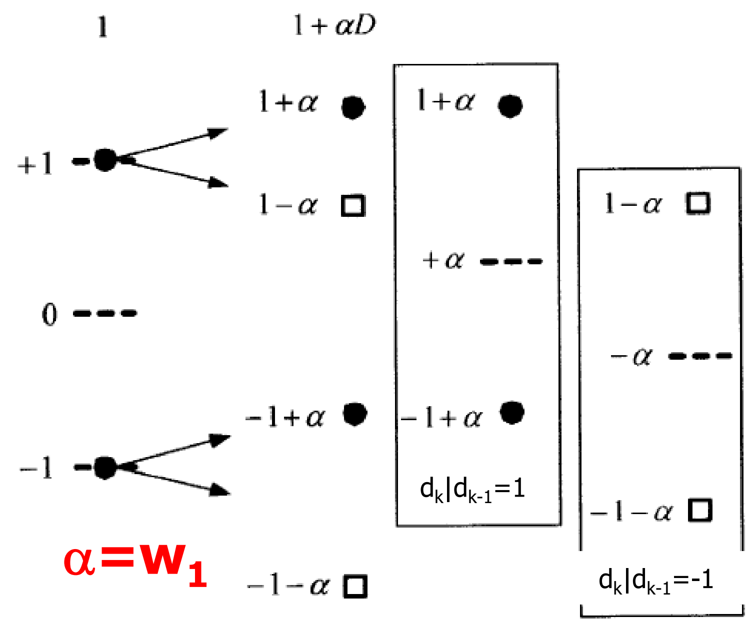
$$t_{CLK \rightarrow QSA} + t_{PROPMUX} + t_{PROPA2} \leq 1UI$$

- Must resolve data and feedback in 1 bit period
  - TI design actually does this in ½UI for CDR

DFE Loop Unrolling



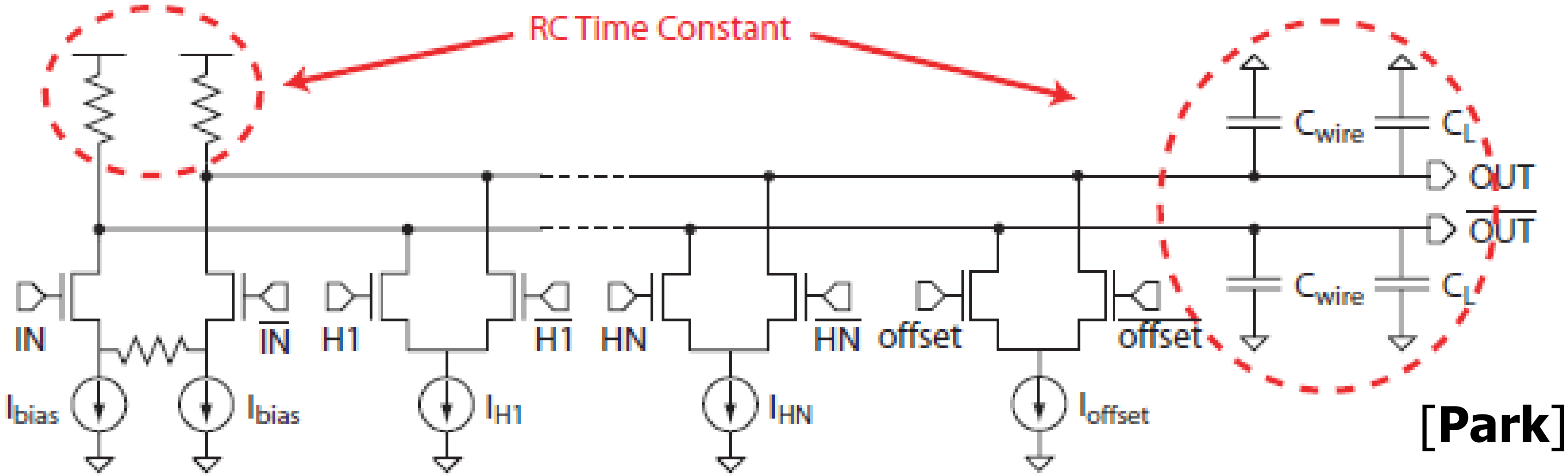




- Instead of feeding back and subtracting ISI in 1UI
- Unroll loop and pre-compute 2 possibilities (1-tap DFE) with adjustable slicer threshold
- With increasing tap number, comparator number grows as $2^{\#taps}$

$$\tilde{d}_k = \begin{cases} \mathrm{sgn}(y_k - w_1) & \text{"if" } \tilde{d}_{k-1} = 1 \\ \mathrm{sgn}(y_k + w_1) & \text{"if" } \tilde{d}_{k-1} = -1 \end{cases}$$

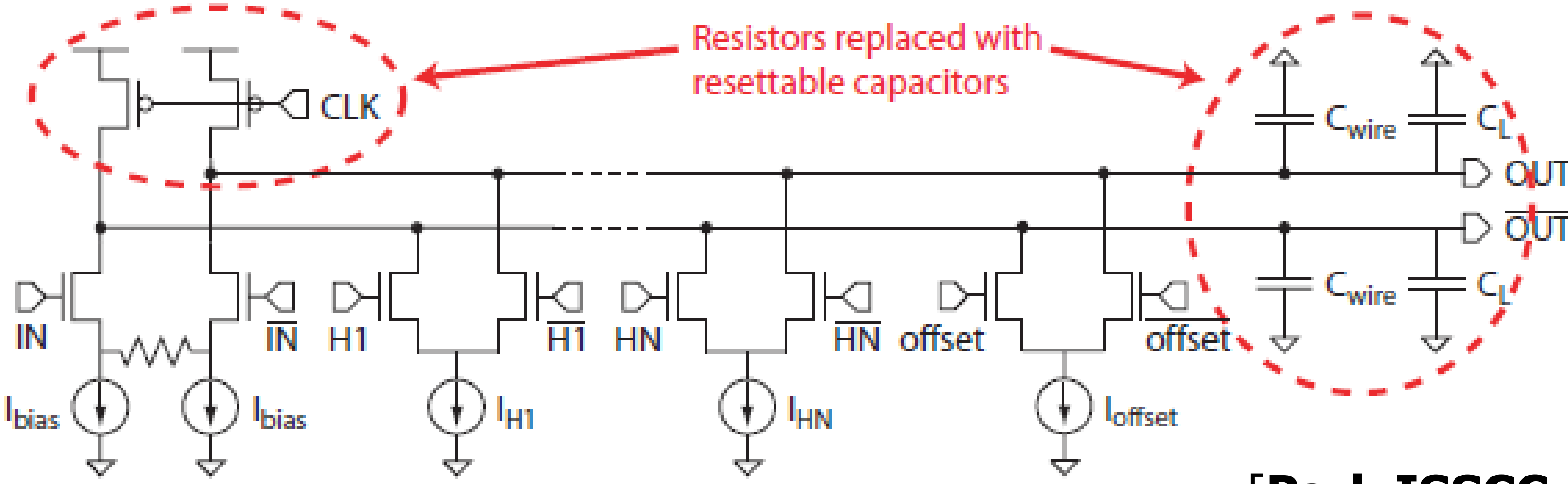
DFE Resistive-Load Summer



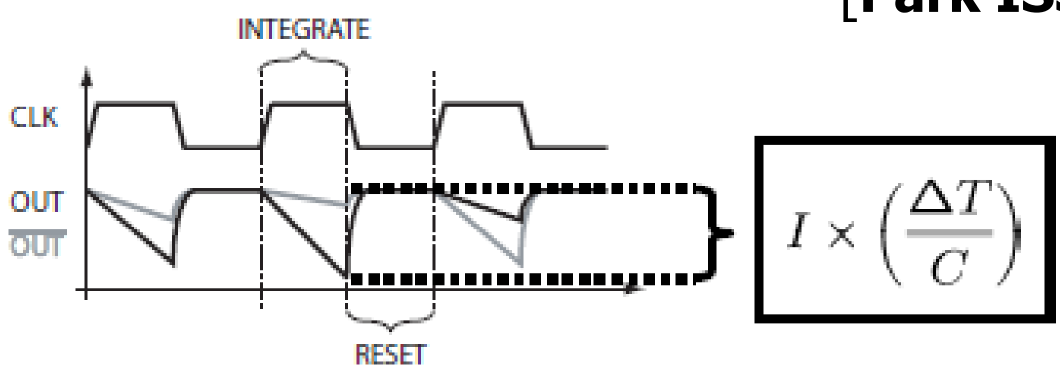
$$\textbf{Summer Swing} = IR, \quad \tau = RC$$

- Summer performance is critical for DFE operation
- Summer must settle within a certain level of accuracy (>95%) for ISI cancellation
- Trade-off between summer output swing and settling time
- Can result in large bias currents for input and taps

DFE Integrating Summer

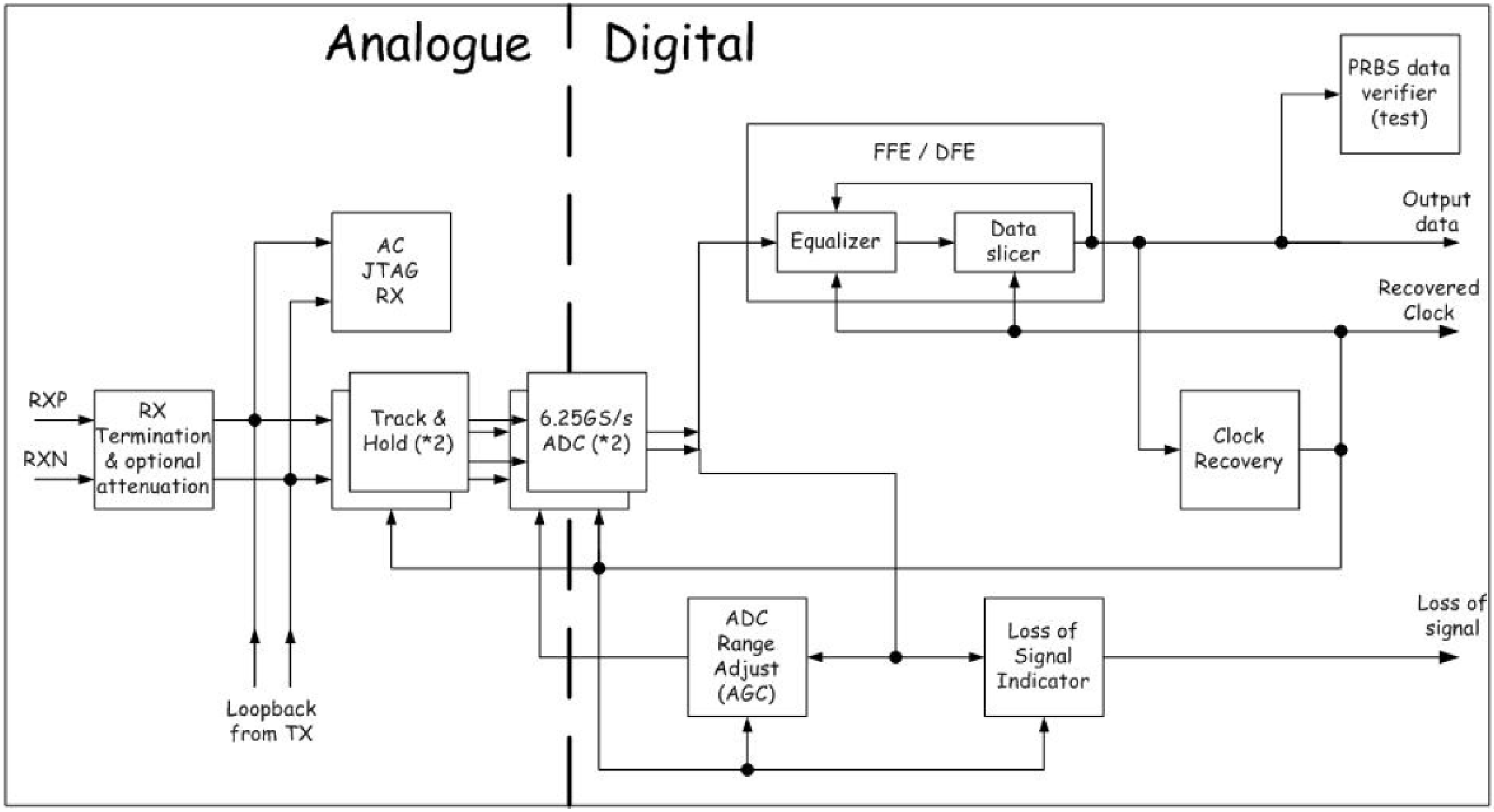


[Park ISSCC 2007]



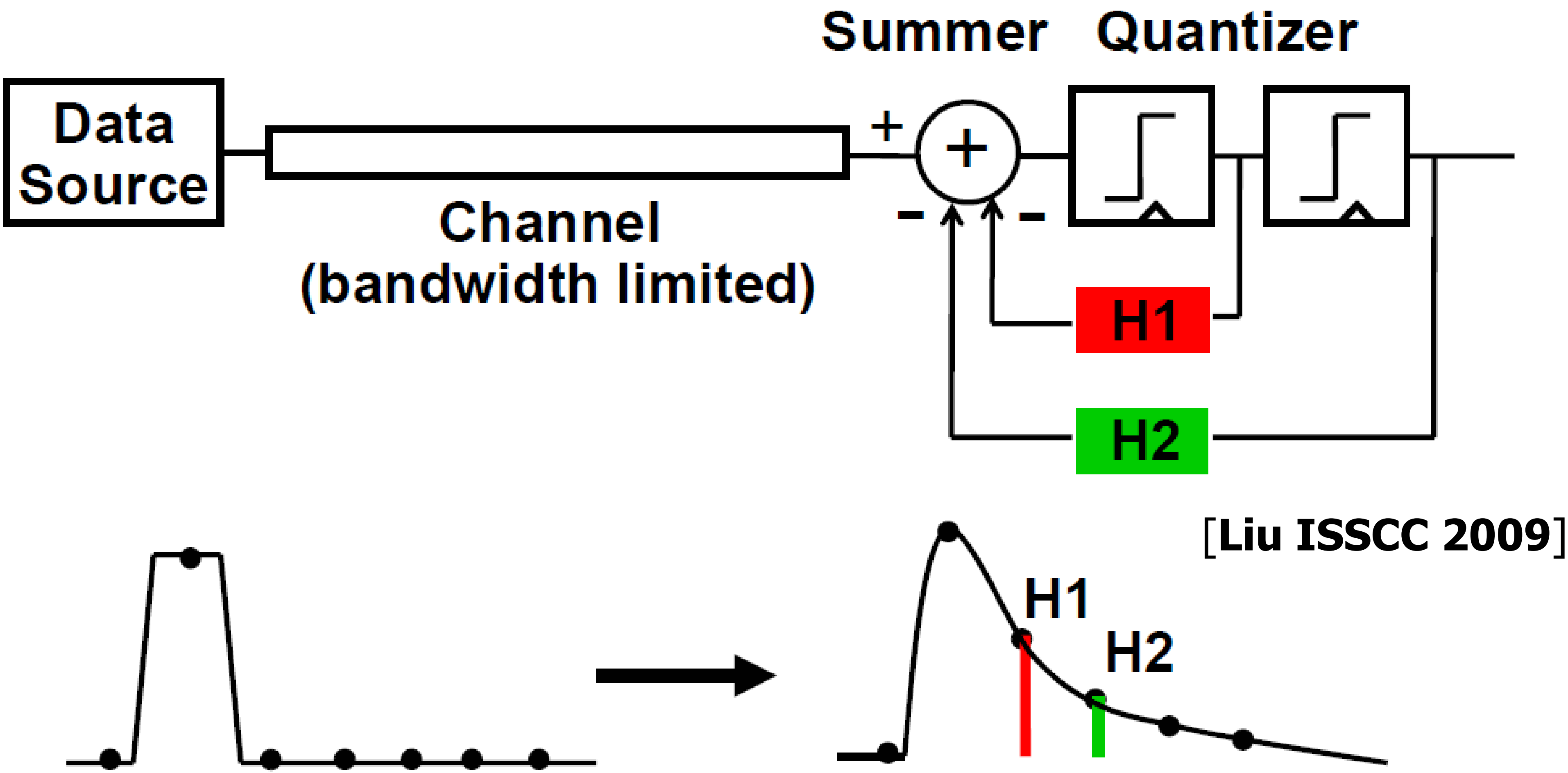
- Integrating current onto load capacitances eliminates RC settling time
- Since ΔT/C > R, bias current can be reduced for a given output swing
  - Typically a 3x bias current reduction

Digital RX FIR & DFE Equalization Example



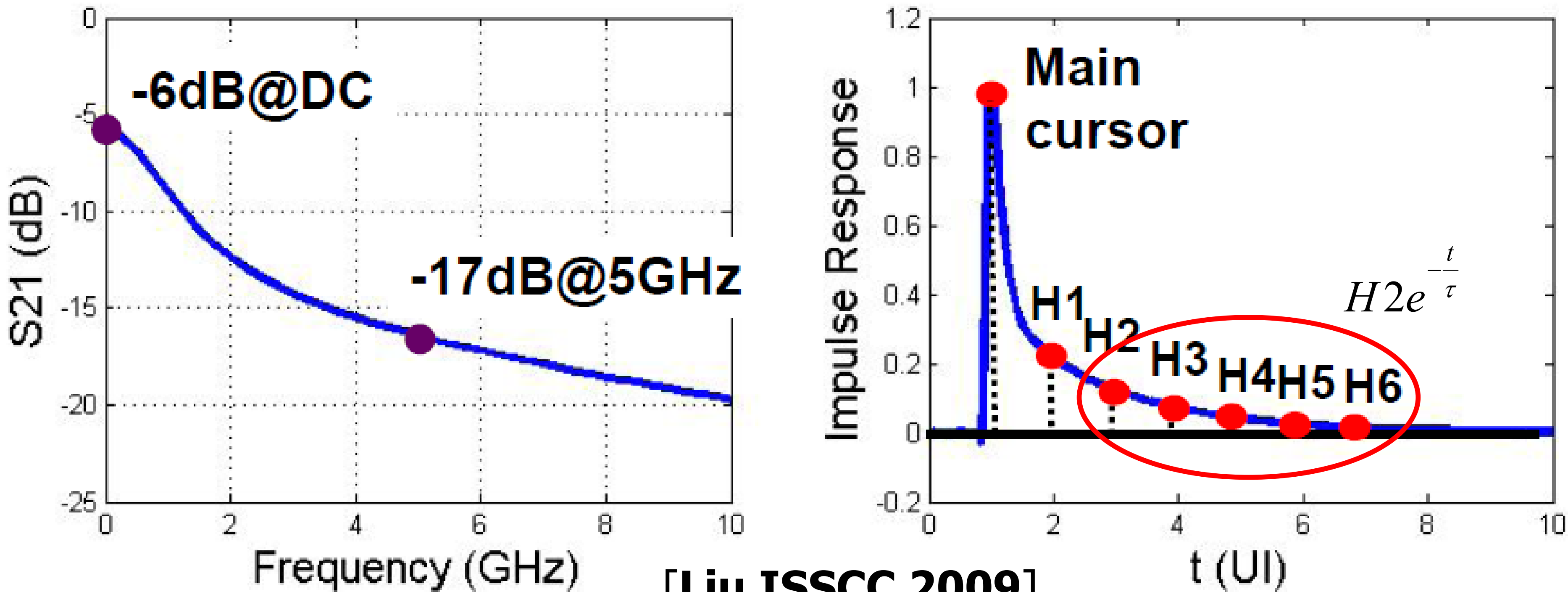
- 12.5GS/s 4.5-bit Flash ADC in 65nm CMOS [**Harwood ISSCC 2007**]
- 2-tap FFE & 5-tap DFE
- XCVR power (inc. TX) = 330mW, Analog = 245mW, Digital = 85mW

DFE with Feedback FIR Filter



- DFE with 2-tap FIR filter in feedback will only cancel ISI of the first two post-cursors

"Smooth" Channel

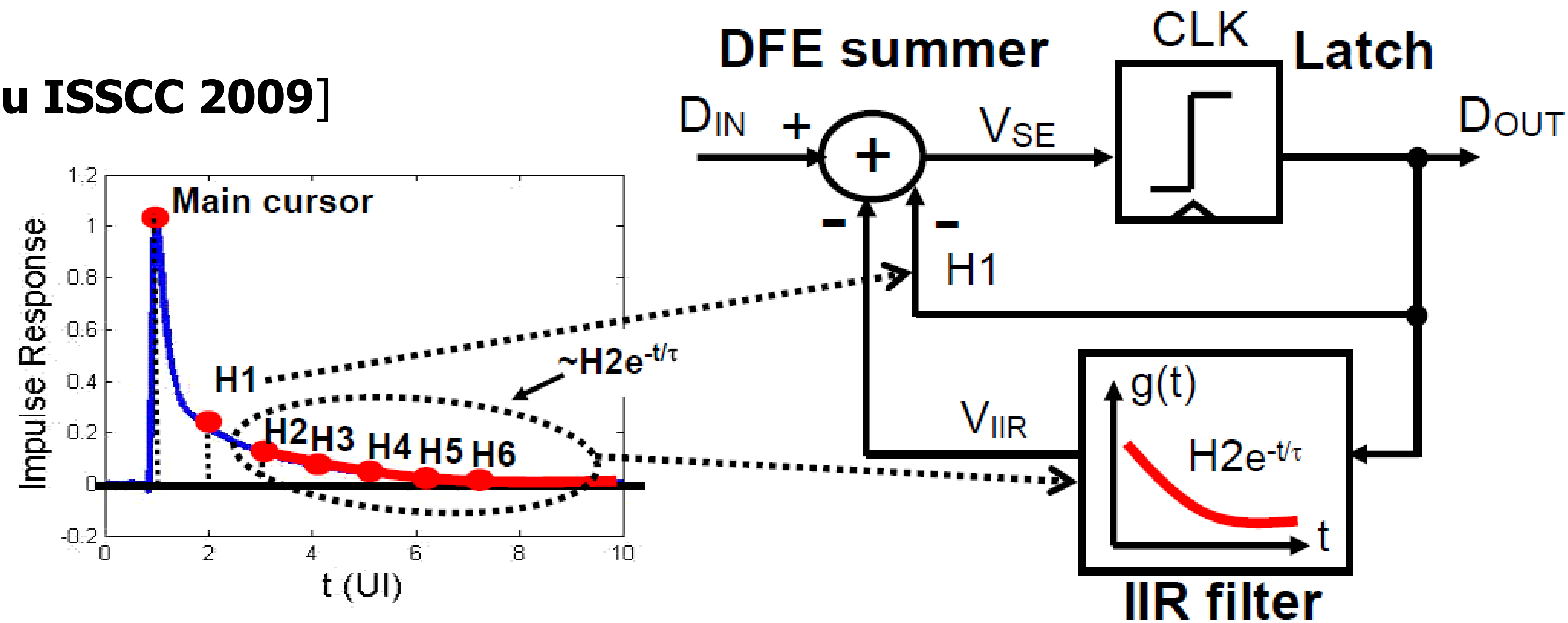


[**Liu ISSCC 2009**]

- A DFE with FIR feedback requires many taps to cancel ISI
- Smooth channel long-tail ISI can be approximated as exponentially decaying
  - Examples include on-chip wires and silicon carrier wires

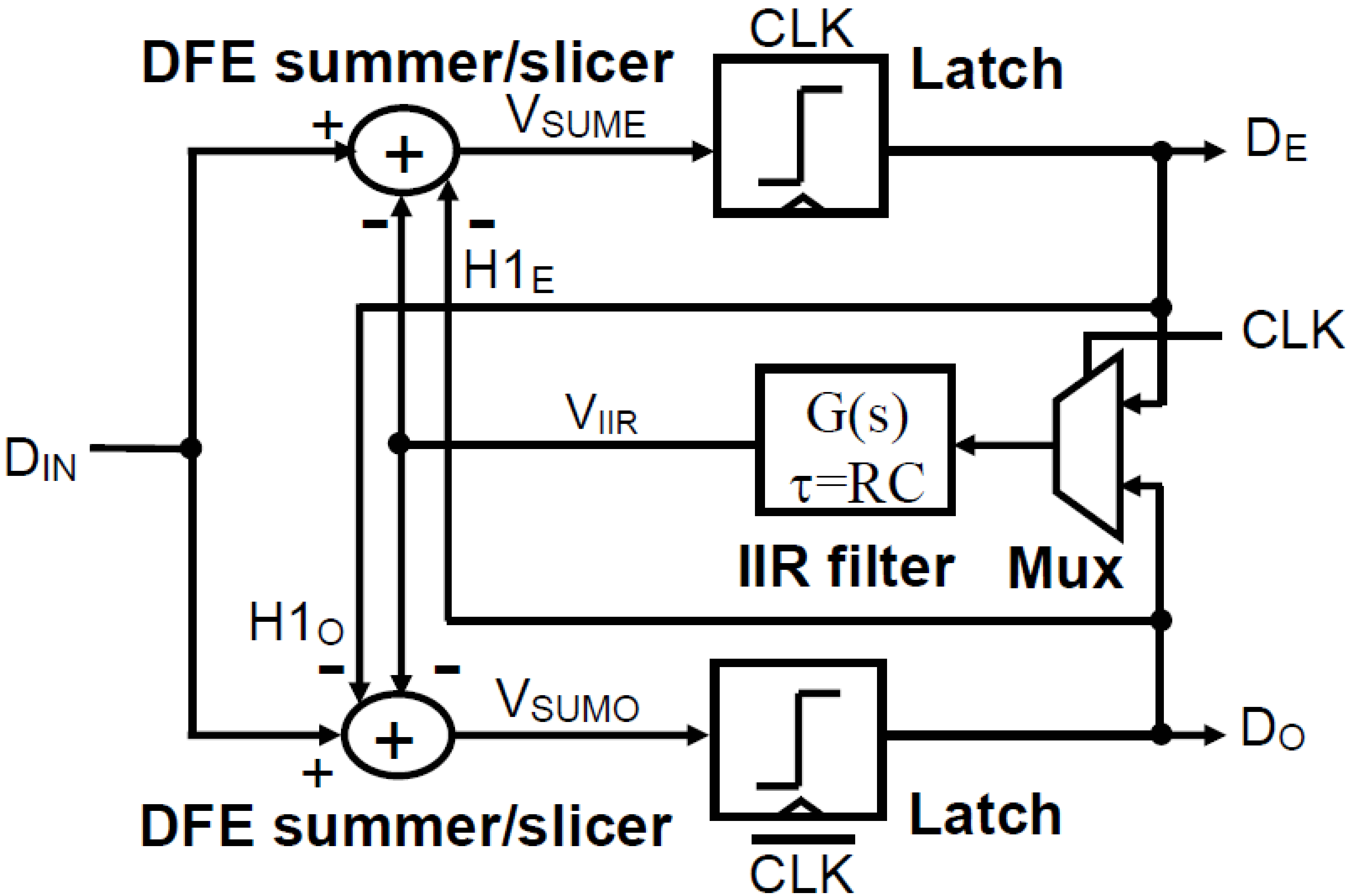
DFE with IIR Feedback

[**Liu ISSCC 2009**]



- Large 1st post-cursor H1 is canceled with normal FIR feedback tap
- Smooth long tail ISI from 2nd post-cursor and beyond is canceled with low-pass IIR feedback filter
- Note: channel needs to be smooth (not many reflections) in order for this approach to work well

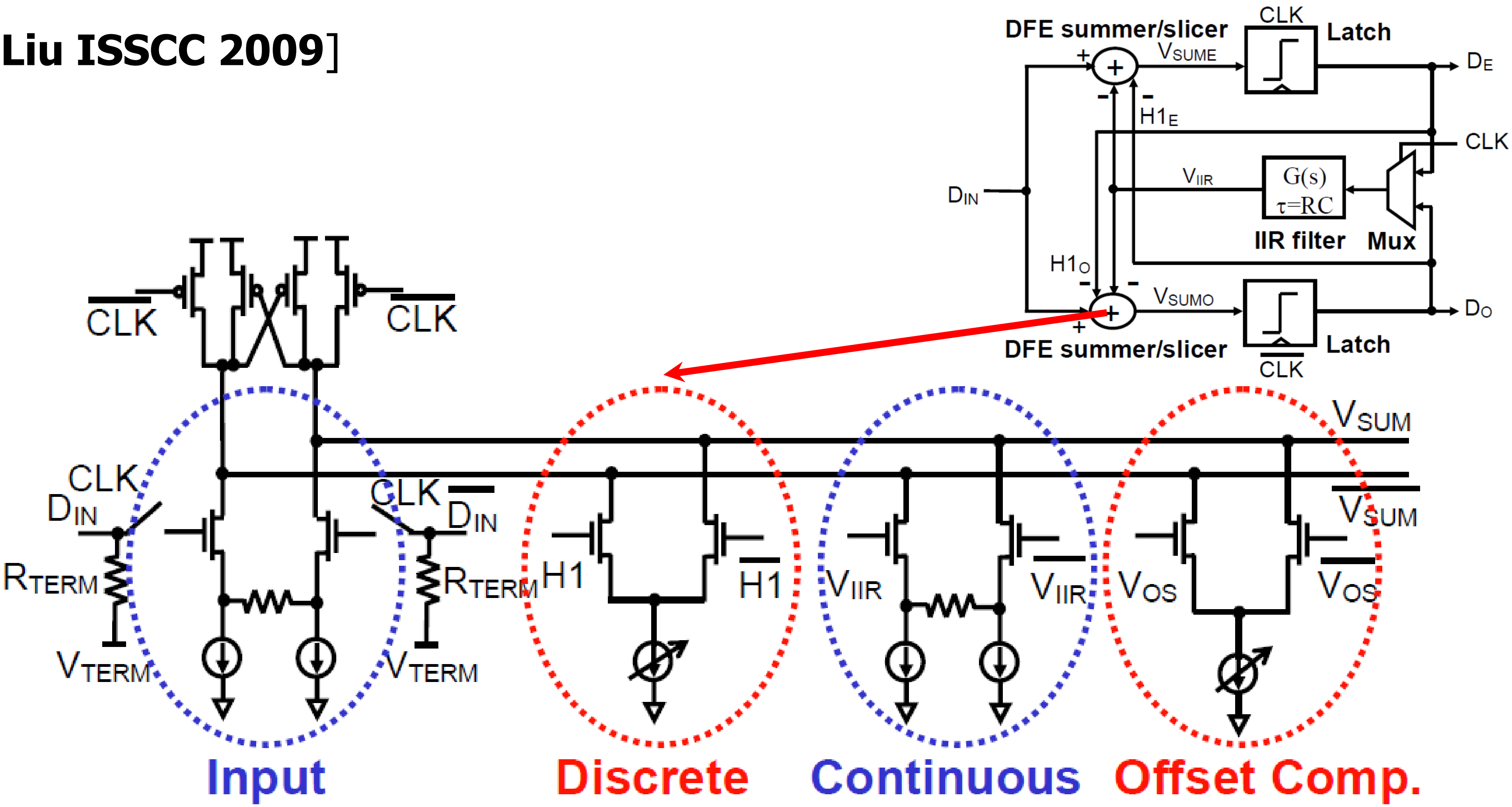
DFE with IIR Feedback RX Architecture



[**Liu ISSCC 2009**]

Merged Summer & Partial Slicer

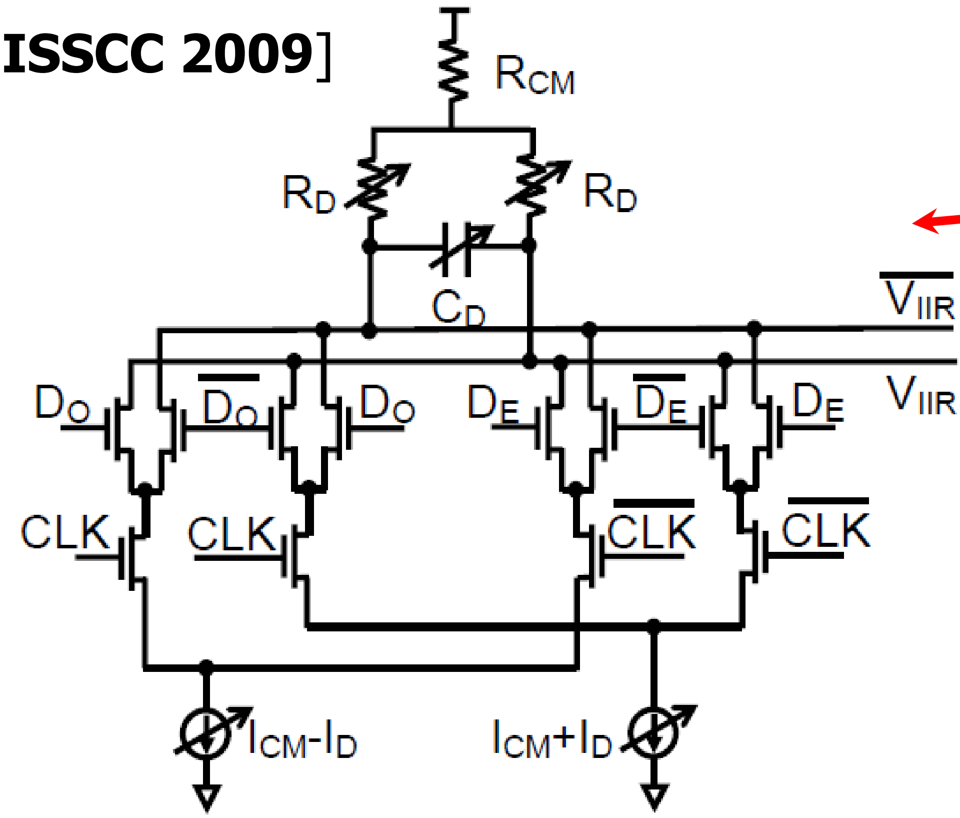
[**Liu ISSCC 2009**]

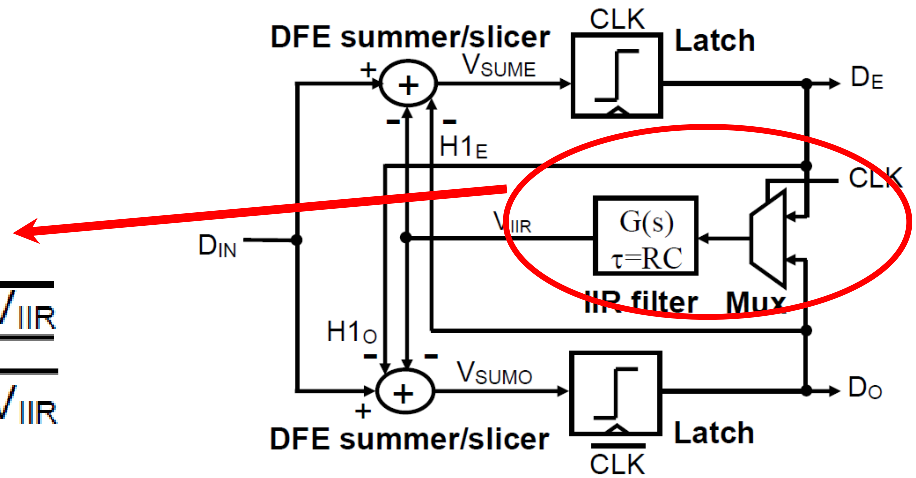


- Integrating summer with regeneration PMOS devices to realize partial slicer operation

Merged Mux & IIR Filter

[**Liu ISSCC 2009**]





- Low-pass response (time constant) implemented by R_D and C_D
- Amplitude controlled by R_D and I_D
- 2 UI delay implemented through mux to begin cancellation at 2nd post-cursor

Agenda

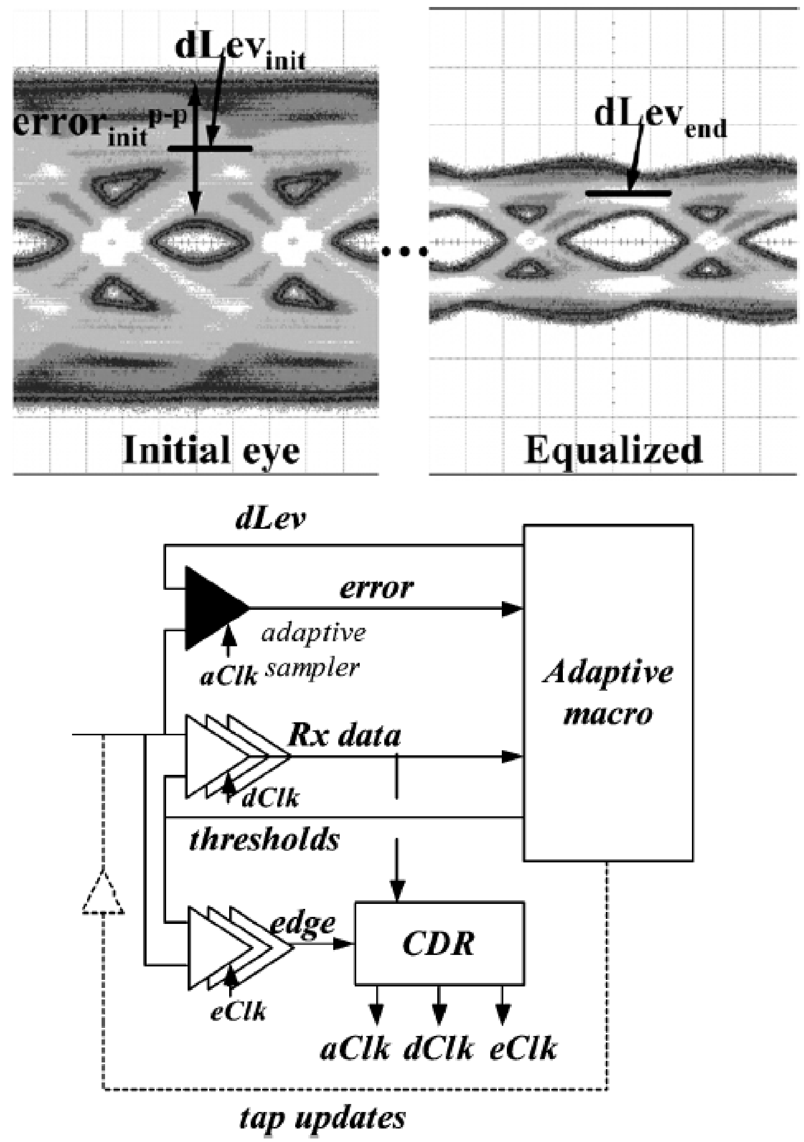
- RX FIR equalization
- RX CTLE equalization
- RX DFE equalization
- Equalization adaptation techniques
- Advanced modulation/other techniques

Setting Equalizer Values

- Simplest approach to setting equalizer values (tap weights, poles, zeros) is to fix them for a specific system
  - Choose optimal values based on lab measurements
  - Sensitive to manufacturing and environment variations
- An adaptive tuning approach allows the optimization of the equalizers for varying channels, environmental conditions, and data rates
- Important issues with adaptive equalization
  - Extracting equalization correction (error) signals
  - Adaptation algorithm and hardware overhead
  - Communicating the correction information to the equalizer circuit

TX FIR Adaptation Error Extraction

- While we are adapting the TX FIR, we need to measure the response at the receiver input
- Equalizer adaptation (error) information is often obtained by comparing the receiver input versus the desired symbol levels, dLev
- This necessitates additional samplers at the receiver with programmable threshold levels



[**Stojanovic JSSC 2005**]

TX FIR Adaptation Algorithm

- The sign-sign LMS algorithm is often used to adapt equalization taps due to implementation simplicity

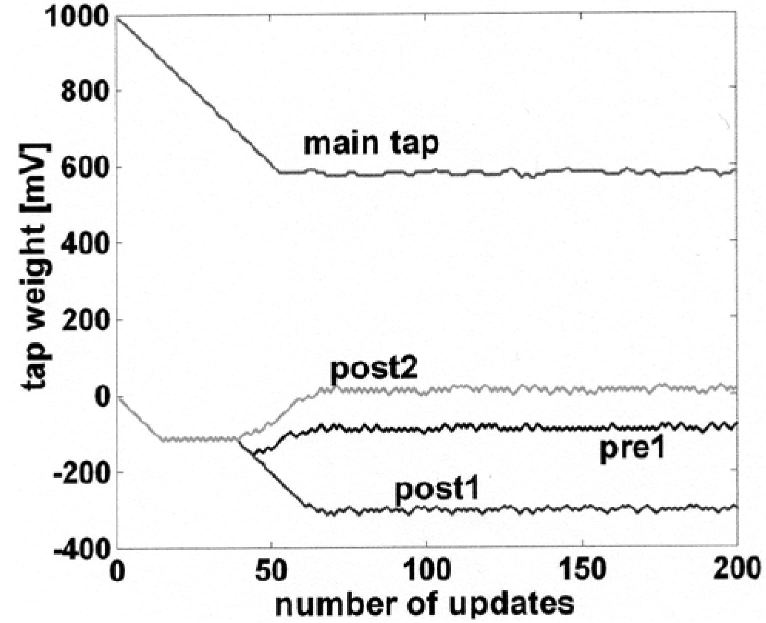
$$w_{n+1}^k = w_n^k + \Delta_w \text{sign}(d_{n-k})\text{sign}(e_n)$$

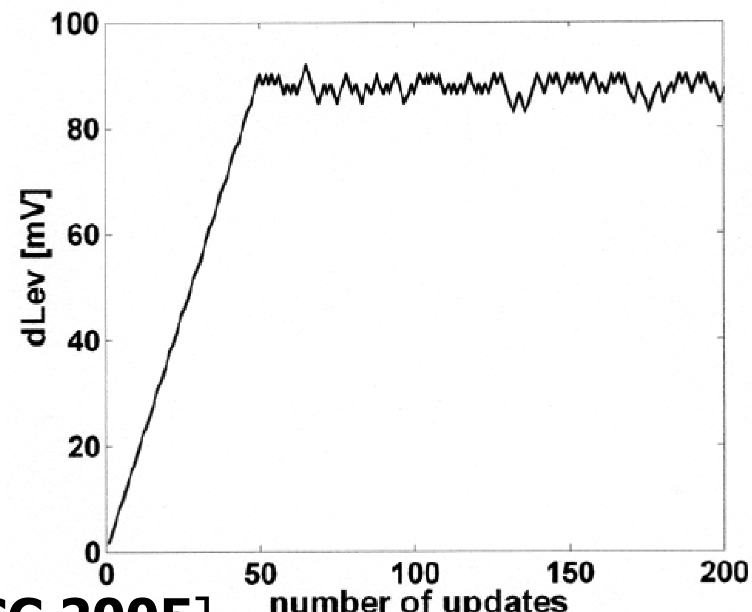
w = tap coefficients, n = time instant, k = tap index, d_n = received data,

e_n = error with respect to desired data level, $dLev$

- As the desired data level is a function of the transmitter swing and channel loss, the desired data level is not necessarily known and should also be adapted

$$dLev_{n+1} = dLev_n - \Delta_{dLev}\text{sign}(e_n)$$

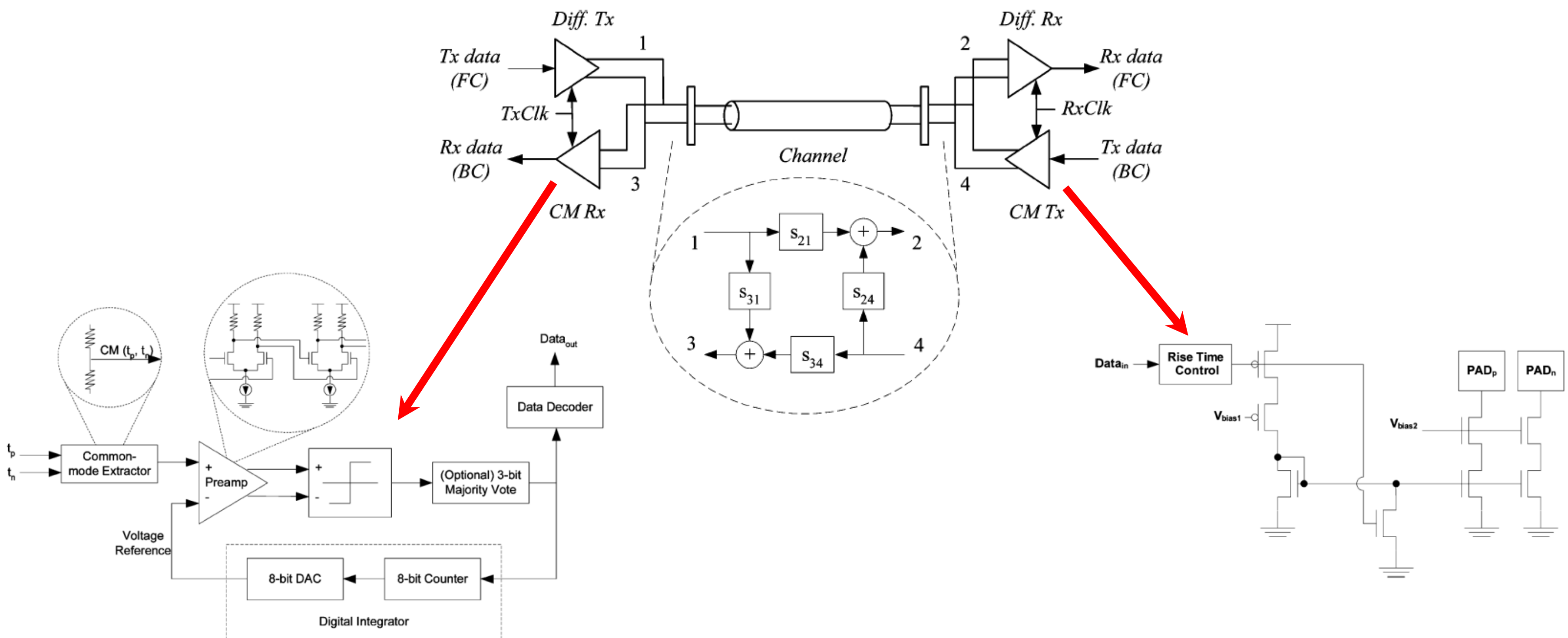




[**Stojanovic JSSC 2005**]

TX FIR Common-Mode Back-Channel

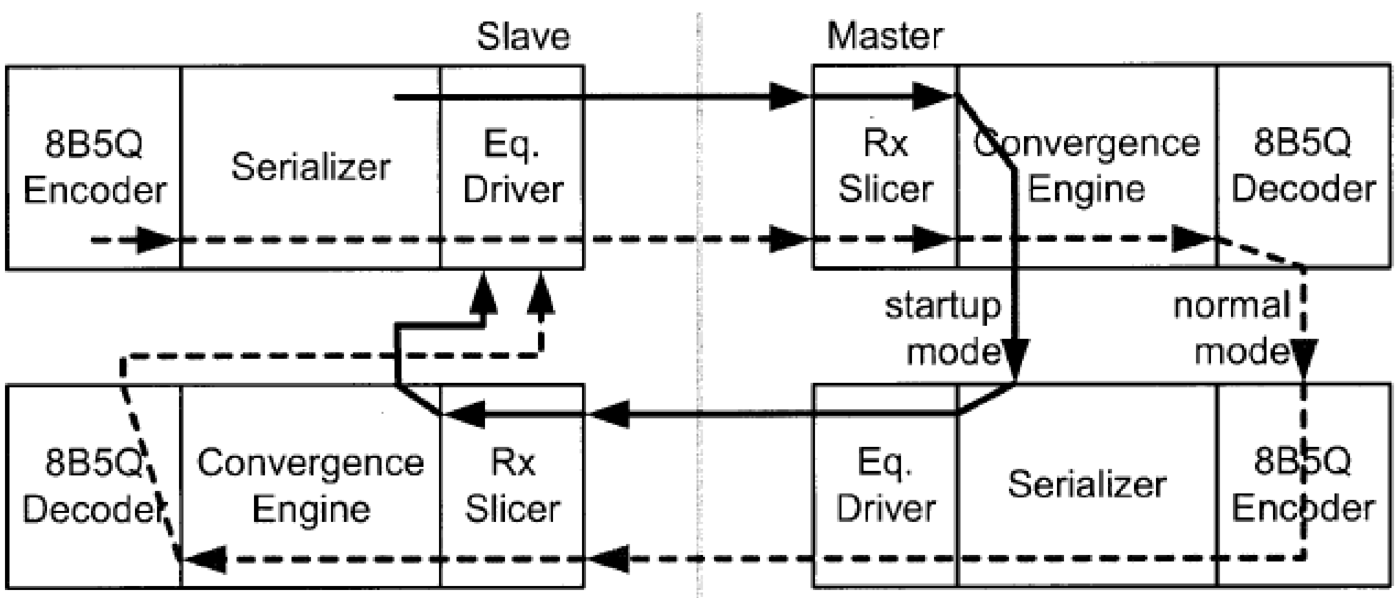
- In order to communicate FIR tap update information back to the TX, a back-channel is necessary
- One option is to use low data rate (~10Mb/s) common-mode signaling from the RX to TX on the same differential channel



[**Stojanovic JSSC 2005**]

TX FIR Data Encoder Back-Channel

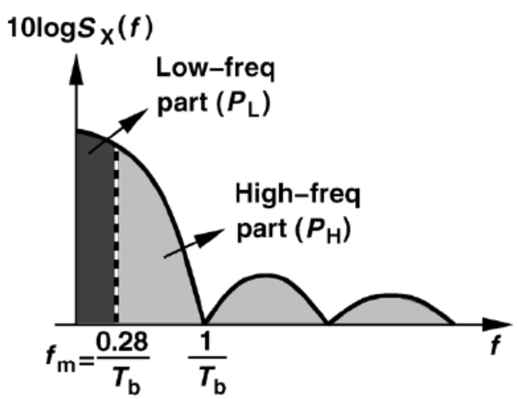
- Another option is to use a high-speed TX channel on the RX side that communicates data back to the TX under adaptation
- Flexibility in data encoding (8B10B/Q) allows low data rate tap adaptation information to be transmitted back without data rate overhead



[**Stonick JSSC 2003**]

CTLE Tuning with PSD Measurement

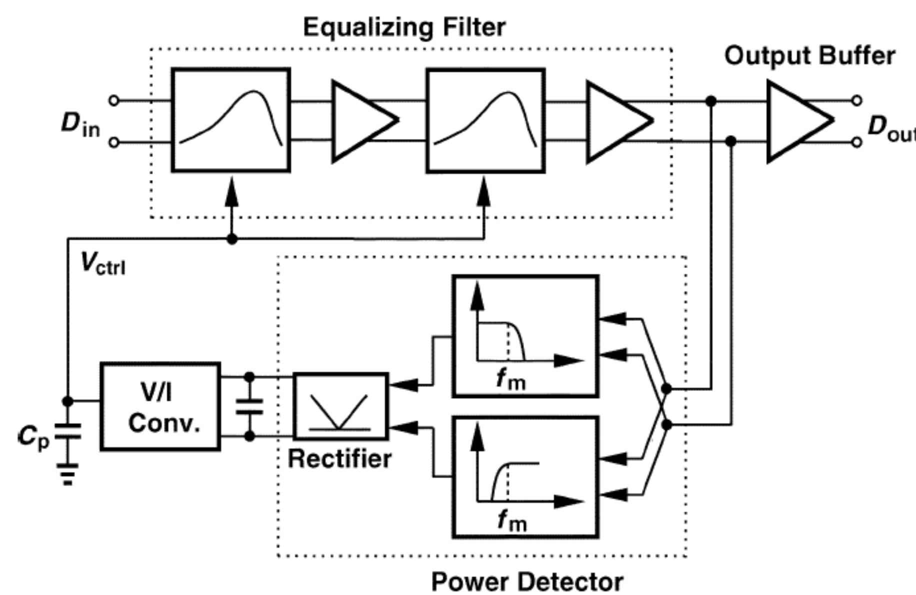
- One approach to CTLE tuning is to compare low-frequency and high-frequency spectrum content of random data
- For ideal random data, there is a predictable ratio between the low-frequency power and high-frequency power
- The error between these power components can be used in a servo loop to tune the CTLE



$$s_x(f) = T_b\left[\frac{\sin(\pi f T_b)}{\pi f T_b}\right]^2$$

$$\int_0^{f_m} s_x(f)\,df = \int_{f_m}^{\infty} s_x(f)\,df = \frac{1}{4}$$

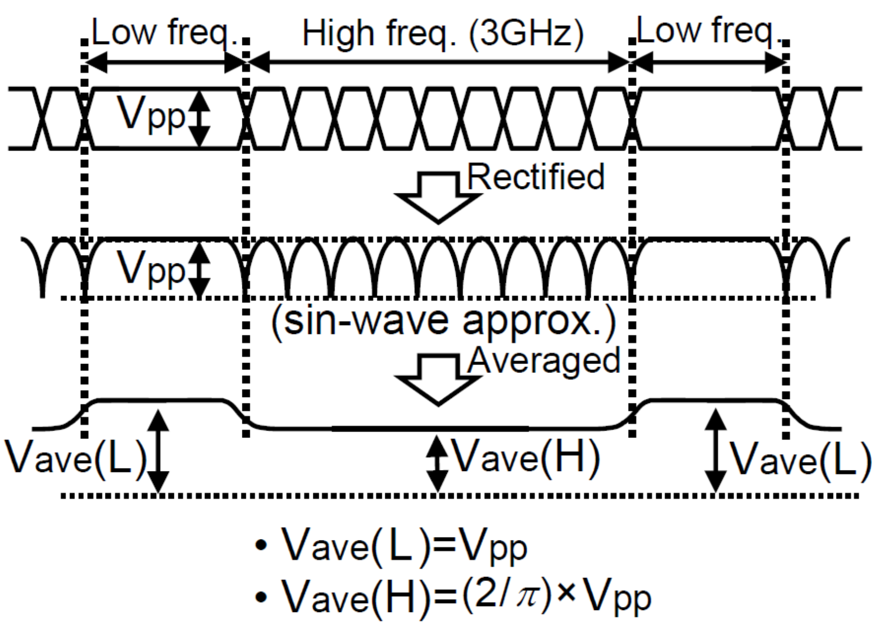
$$\text{where } f_m \approx \frac{0.28}{T_b}$$

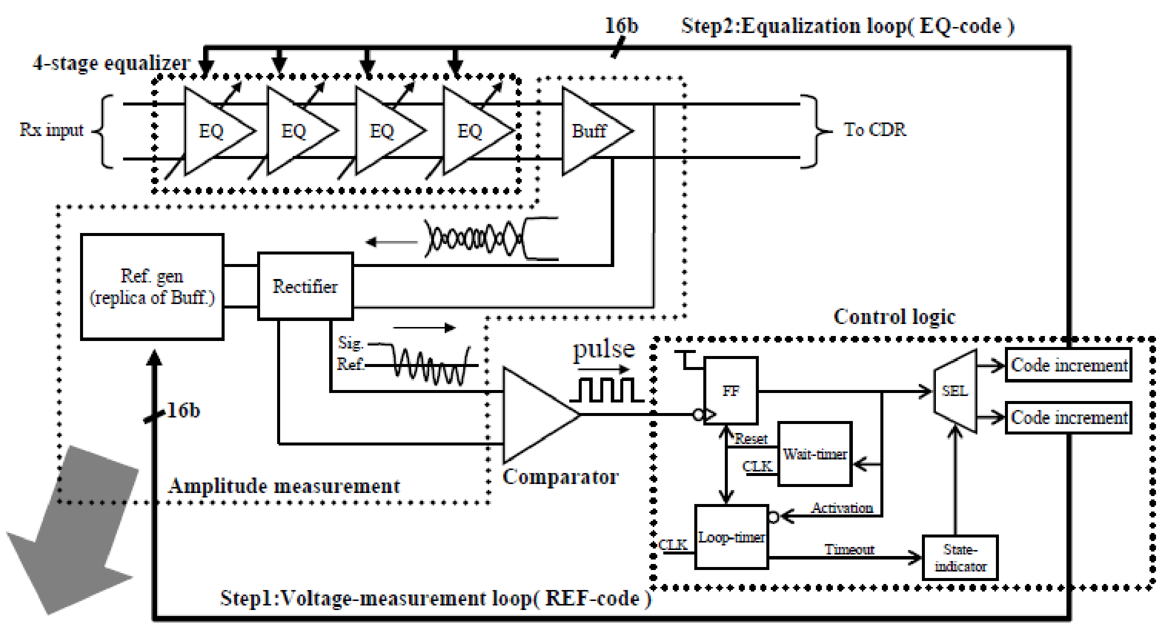


[**Lee JSSC 2006**]

CTLE Tuning w/ Output Amplitude Measurement

- CTLE tuning can also be done by comparing low-frequency and high-frequency average amplitude
- Approximating the equalized data as a sine wave, a predictable ratio exists between the low frequency average and high-frequency average
- Equalizer settings are adjusted until the high frequency peak-to-peak swing matches the low-frequency peak-to-peak swing

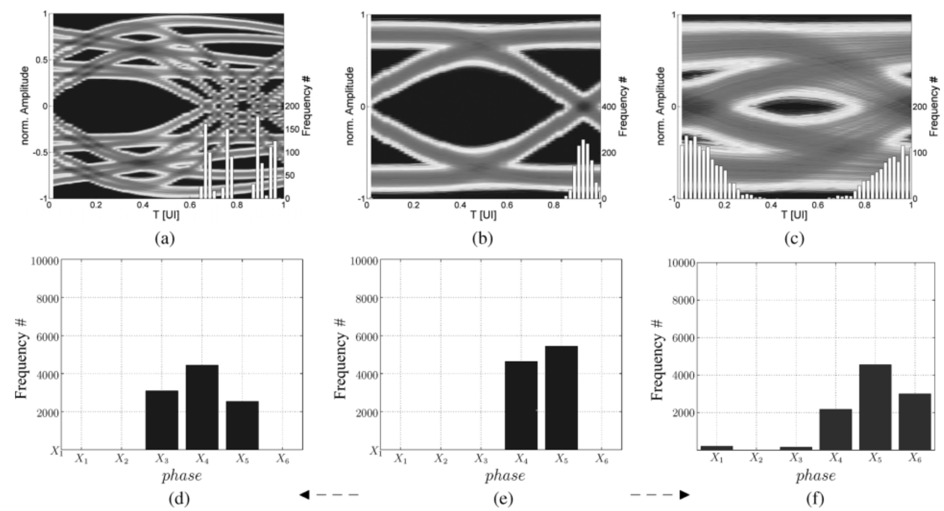


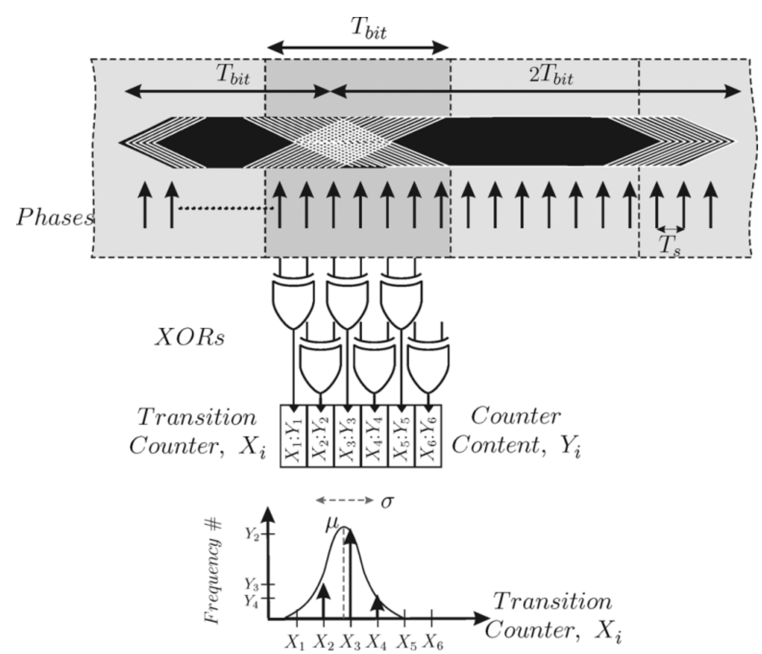


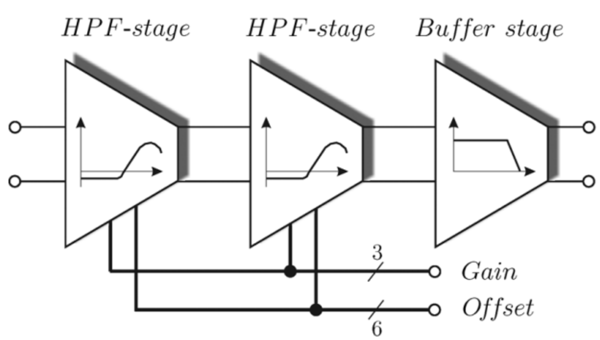
[**Uchiki ISSCC 2008**]

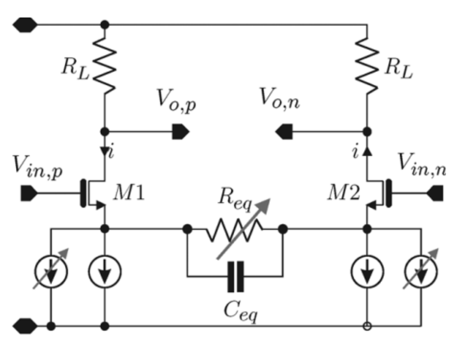
CTLE Tuning w/ Data Edge Distribution Monitoring

- The width and shape of the data edge distribution can be used to reliably calibrate an equalizer
- By oversampling the data bits with sub-period accuracy, this information can be obtained
- Objective is to maximize eye opening, or equivalently minimizing the standard deviation of the edge distribution



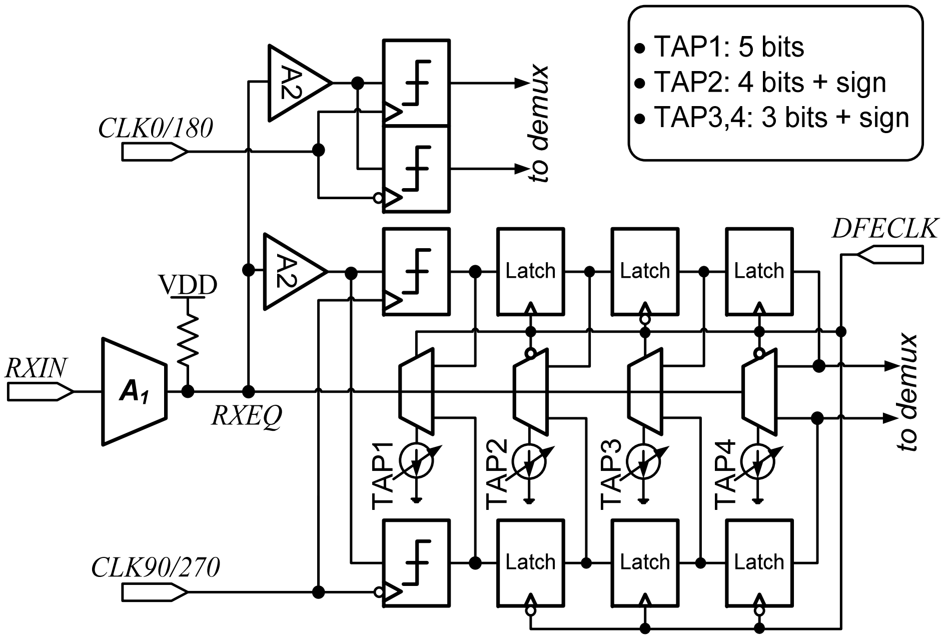


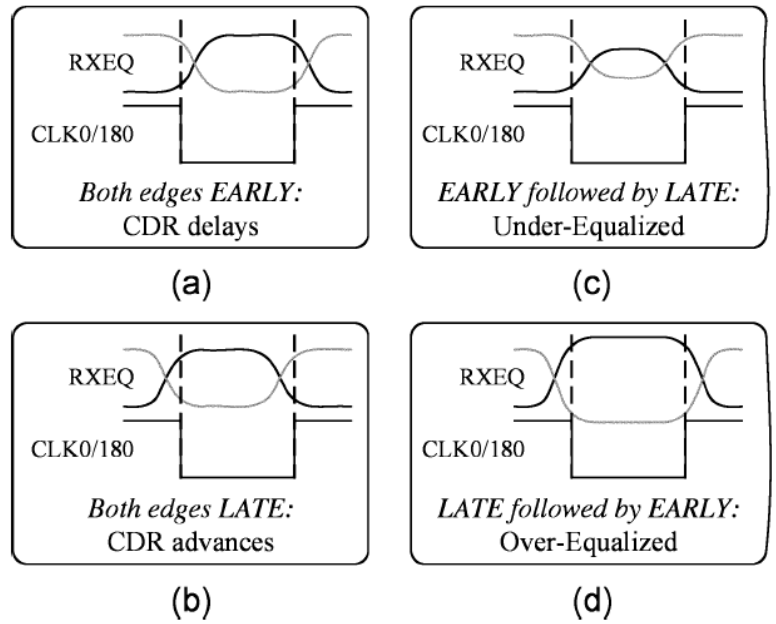




[**Gerfers JSSC 2008**]

DFE Tuning – FIR Feedback

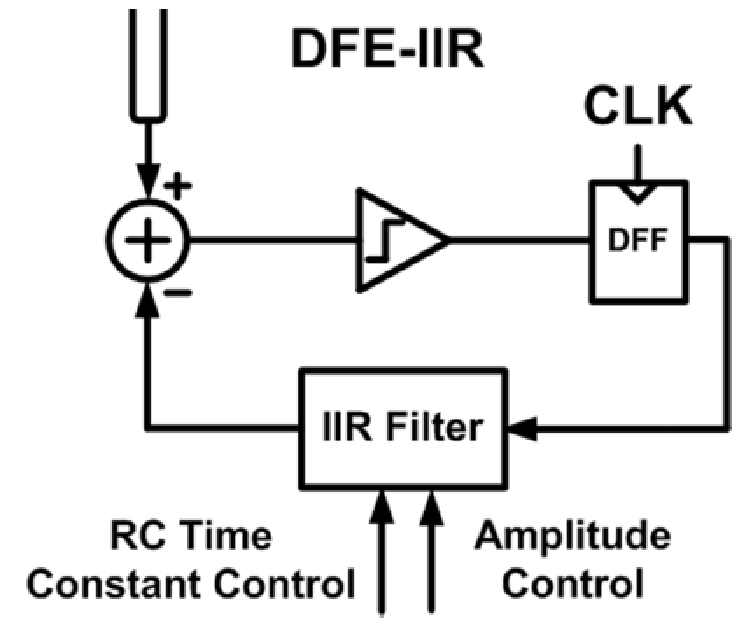


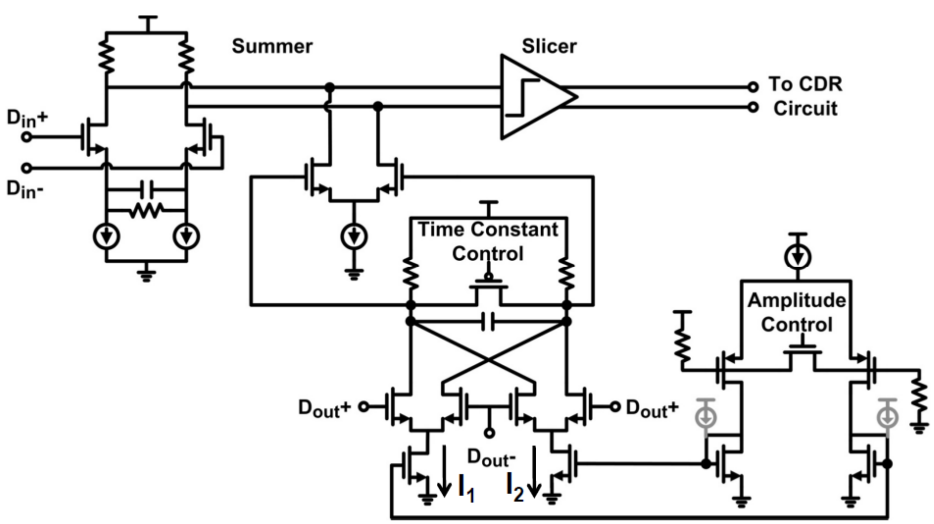


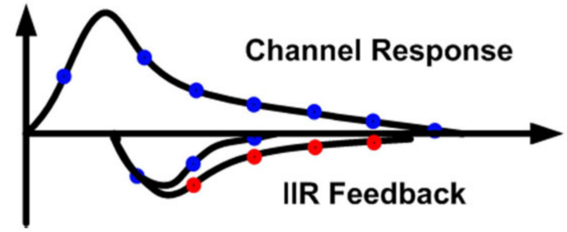
- 2x oversampling the equalized signal at the edges can be used to extract information to adapt a DFE and drive a CDR loop
- Sign-sign LMS algorithm used to adapt DFE tap values

[**Payne JSSC 2005**]

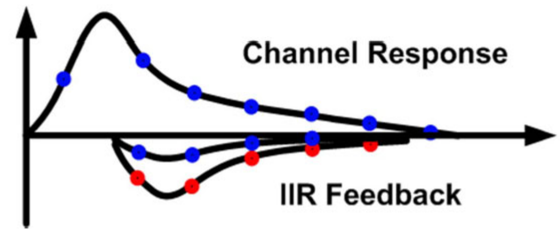
DFE Tuning – IIR Feedback



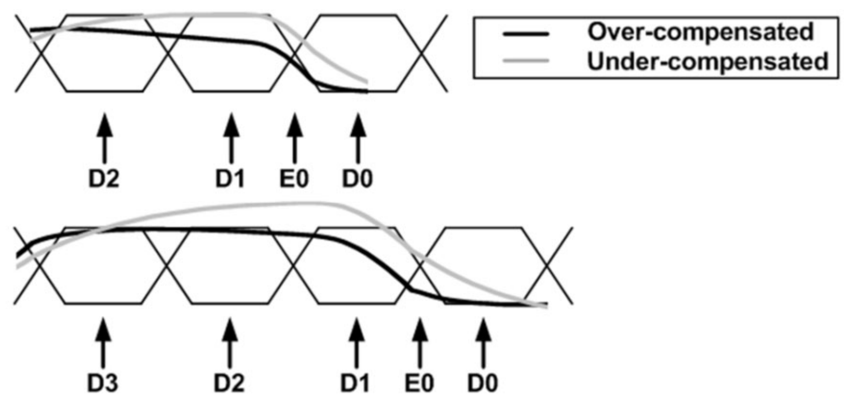




RC time constant control ➔ Equivalent tap number



Amplitude control ➔ Equivalent tap weight



Case 1 D2,D1,D0= 110	$ISI_{E0}>0$	Increases amplitude
	$ISI_{E0}<0$	Decreases amplitude
Case 2 D3,D2,D1,D0= 1110	$ISI_{E0}>0$	Increases time constant
	$ISI_{E0}<0$	Decreases time constant

Y. Hidaka, et al., ISSCC07

[**Huang ISSCC 2011**]

Agenda

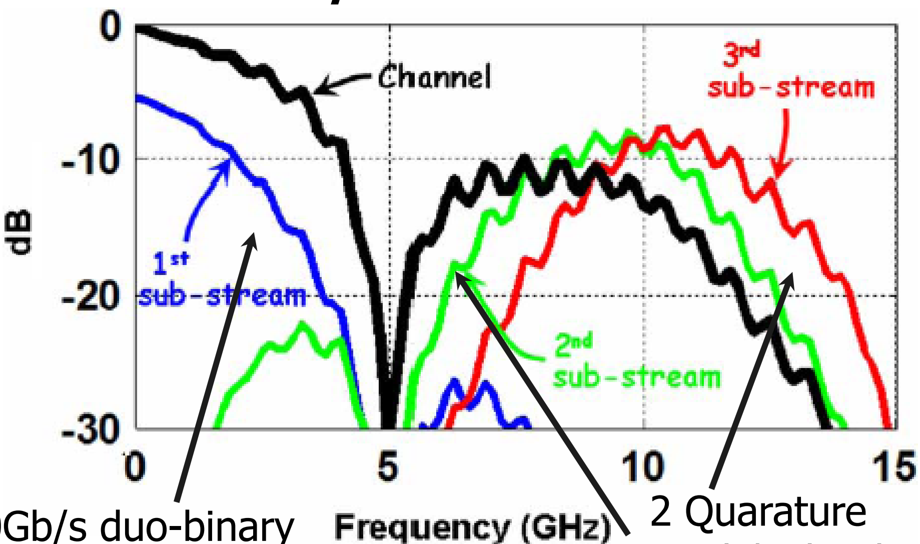
- RX FIR equalization
- RX CTLE equalization
- RX DFE equalization
- Equalization adaptation techniques
- Advanced modulation/other techniques

Advanced Modulation

- In order to remove ISI, we attempt to equalize or flatten the channel response out to the Nyquist frequency
- For less frequency-dependent loss, move the Nyquist frequency to a lower value via more advance modulation
  - 4-PAM (or higher)
  - Duo-binary
- Refer to lecture 4 for more details

Multi-tone Signaling

30Gb/s total in 2 bands

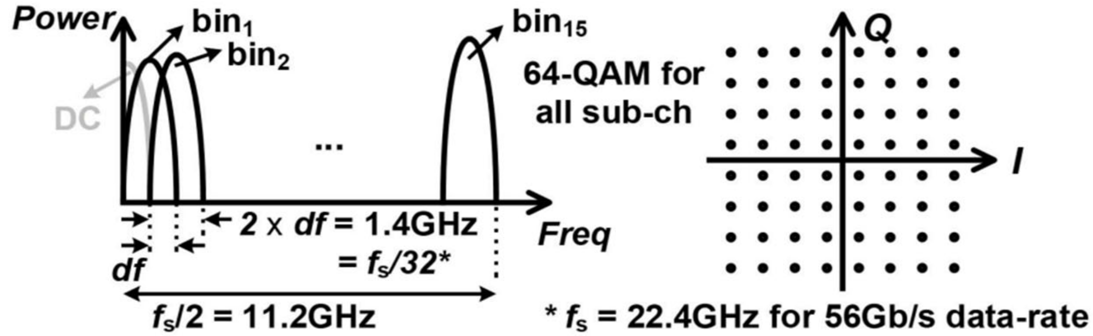


10Gb/s duo-binary

2 Quarature 10Gb/s duo-binary

[**Beyene AdvPack 2008**]

56Gb/s total in 15 bands



[**Kim ISSCC 2019**]

- Instead equalizing out to baseband Nyquist frequency
- Divide the channel into bands with less frequency-dependent loss
- Should result in less equalization complexity for each sub-band
- Requires up/down-conversion
- Discrete Multi-tone used in DSL modems with very challenging channels
  - Lower data rates allow for high performance DSP
  - Recently seeing this in some high-speed link research prototypes

Next Time

- Link Noise and BER Analysis