ECEN689: Special Topics in High-Speed Links Circuits and Systems Spring 2011

Lecture 8: Termination & TX Driver Circuits

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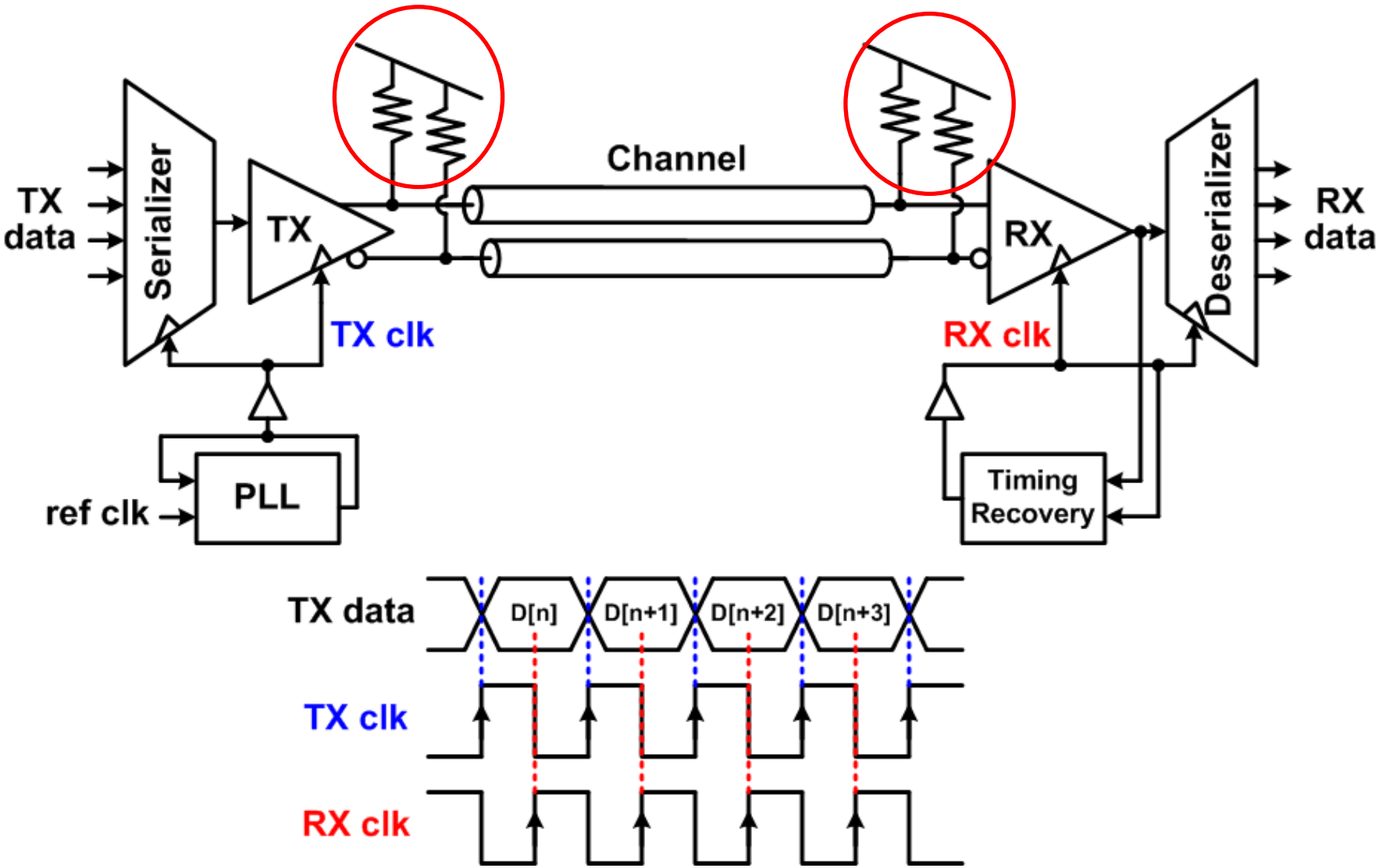
Announcements & Agenda

- Reading
  - Will post some papers on voltage-mode drivers
- Termination Circuits
- TX Driver Circuits

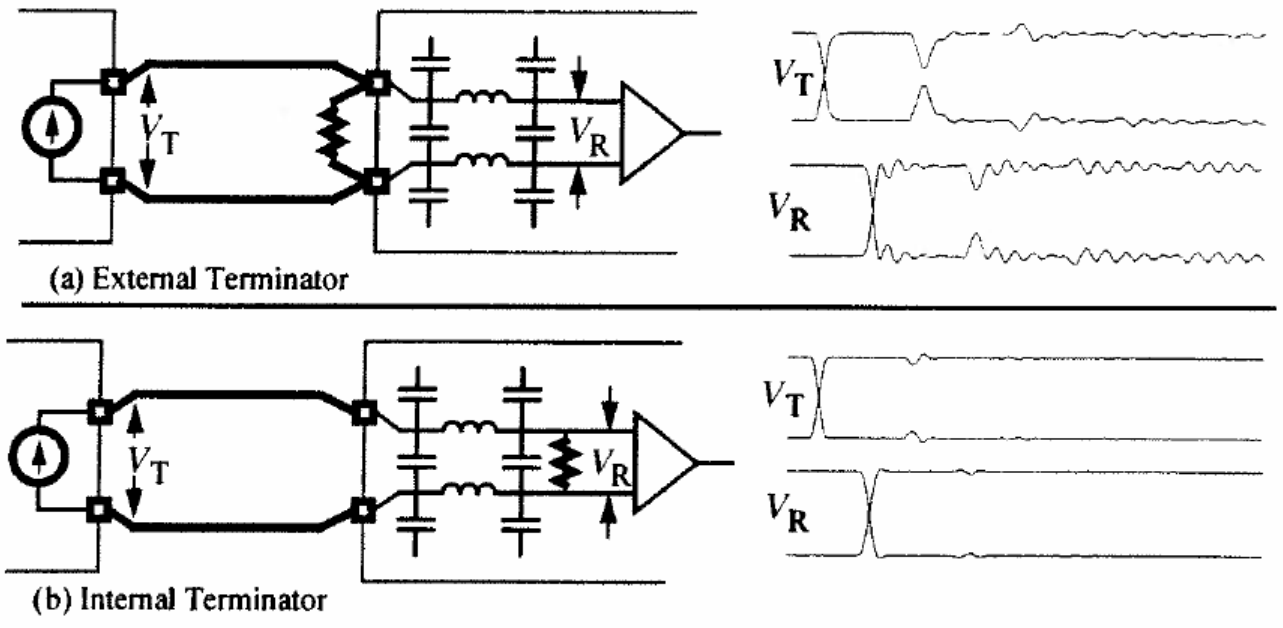
High-Speed Electrical Link System



Termination

- Off-chip vs on-chip
- Series vs parallel
- DC vs AC Coupling
- Termination circuits

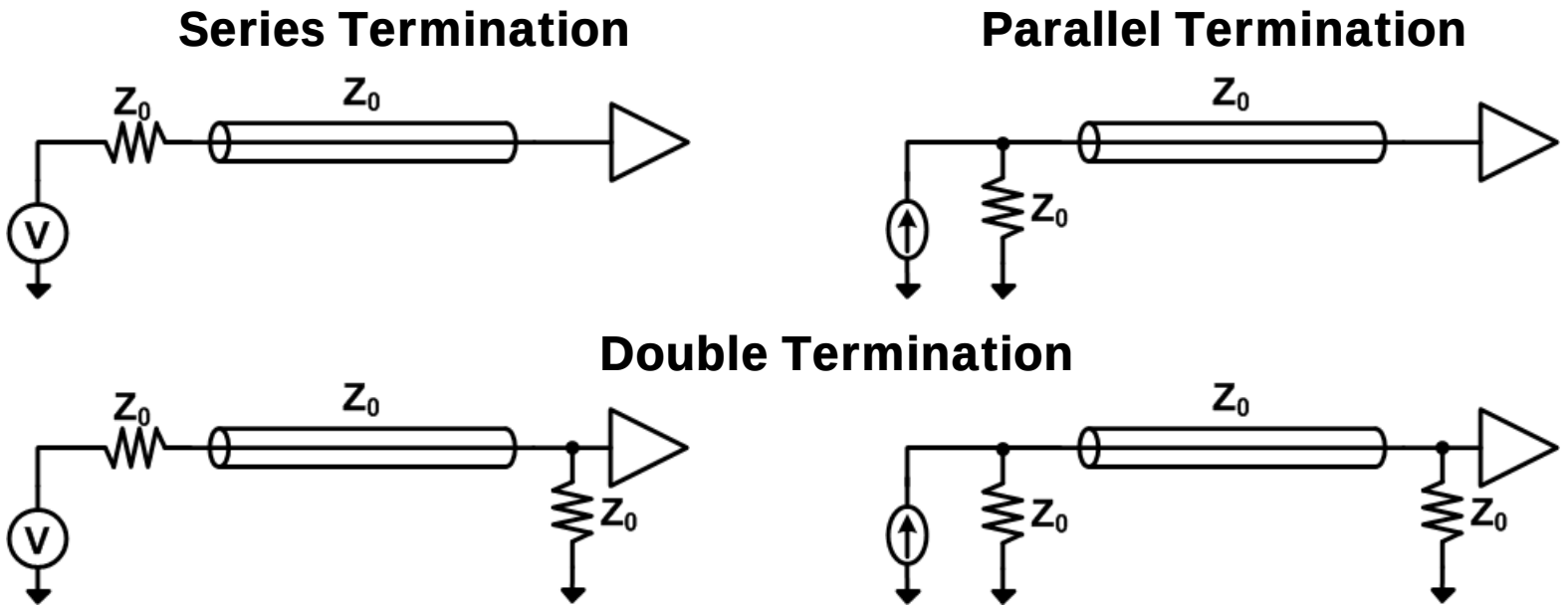
Off-Chip vs On-Chip Termination



[**Dally**]

- Package parasitics act as an unterminated stub which sends reflections back onto the line
- On-chip termination makes package inductance part of transmission line

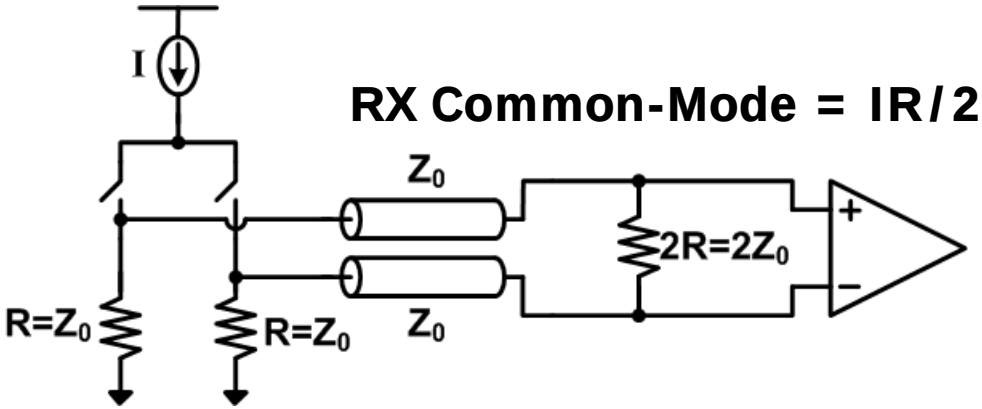
Series vs Parallel Termination



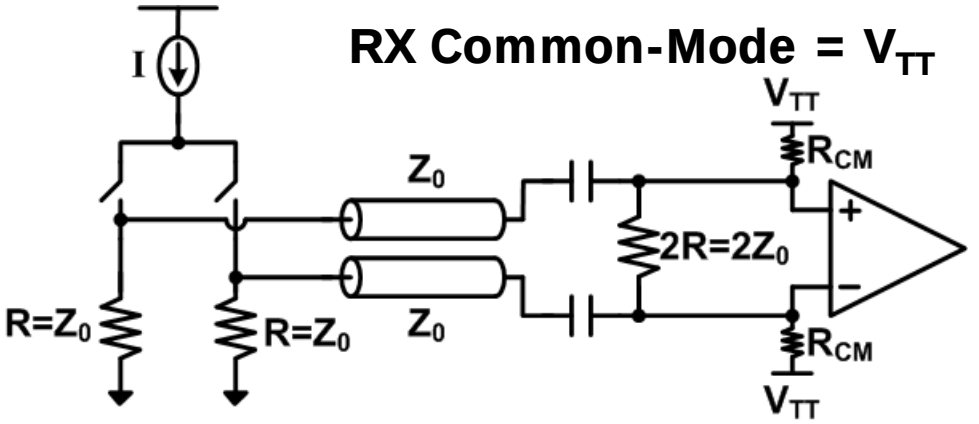
- Low impedance voltage-mode driver typically employs series termination
- High impedance current-mode driver typically employs parallel termination
- Double termination yields best signal quality
  - Done in majority of high performance serial links

AC vs DC Coupled Termination

- DC coupling allows for uncoded data
- RX common-mode set by transmitter signal level



- AC coupling allows for independent RX common-mode level
- Now channel has low frequency cut-off
  - Data must be coded



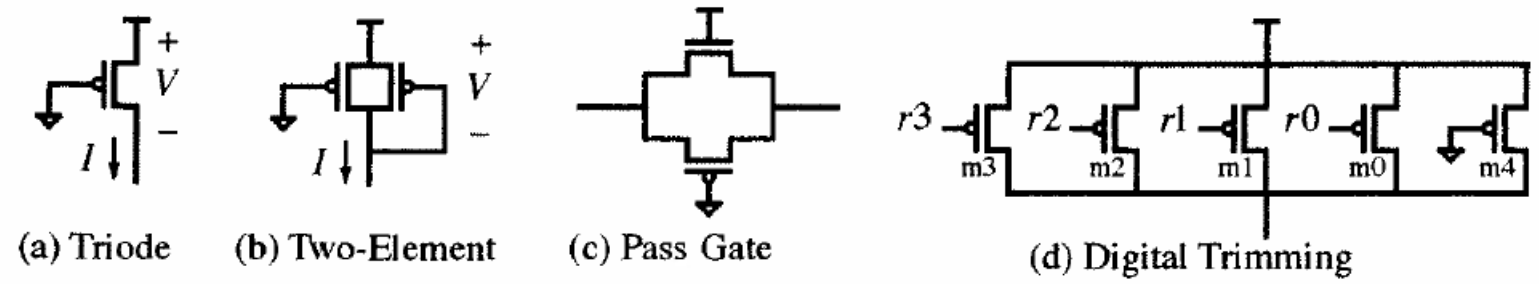
Passive Termination

- Choice of integrated resistors involves trade-offs in manufacturing steps, sheet resistance, parasitic capacitance, linearity, and ESD tolerance
- Integrated passive termination resistors are typically realized with unsalicided poly, diffusion, or n-well resistors
- Poly resistors are typically used due to linearity and tighter tolerances, but they typically vary +/-30% over process and temperature

Resistor Options (90nm CMOS)

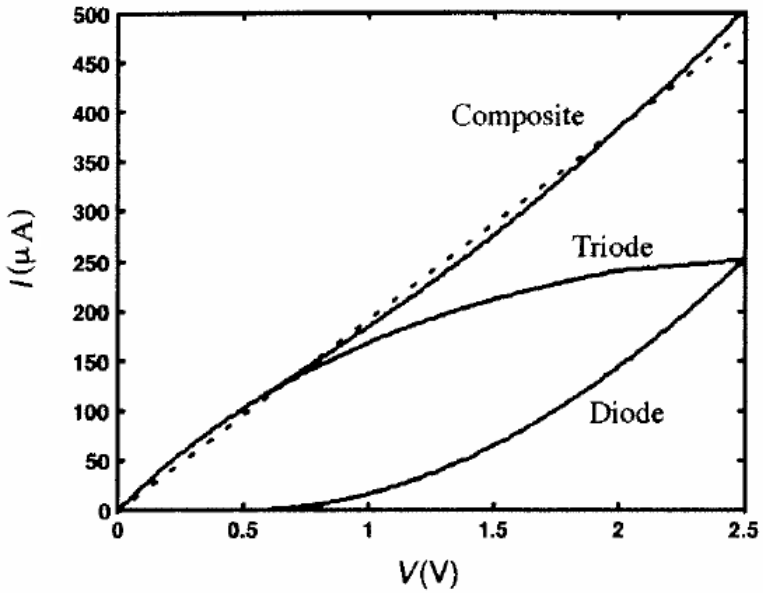
Resistor	Poly	N-diffusion	N-well
Sheet R (Ω/sq)	90±10	300±50	450±200
VC1(V^{-1})	0	10^{-3}	$8x10^{-3}$
Parasitic Cap	2-3fF/um^2 (min L poly)	0.9fF/um^2 (area), 0.04fF/um (perimeter)	0.2fF/um^2 (area), 0.7fF/um (perimeter)

Active Termination



- Transistors must be used for termination in CMOS processes which don't provide resistors
- Triode-biased FET works well for low-swing (<500mV)
  - Adding a diode connected FET increases linear range
- Pass-gate structure allows for differential termination

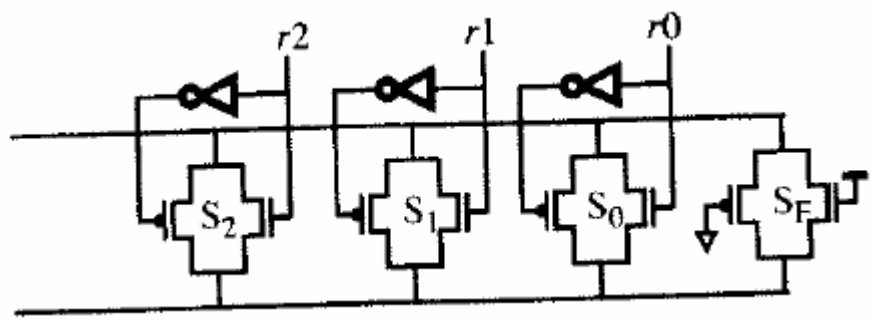
[Dally]



Adjustable Termination

- FET resistance is a function of gate overdrive

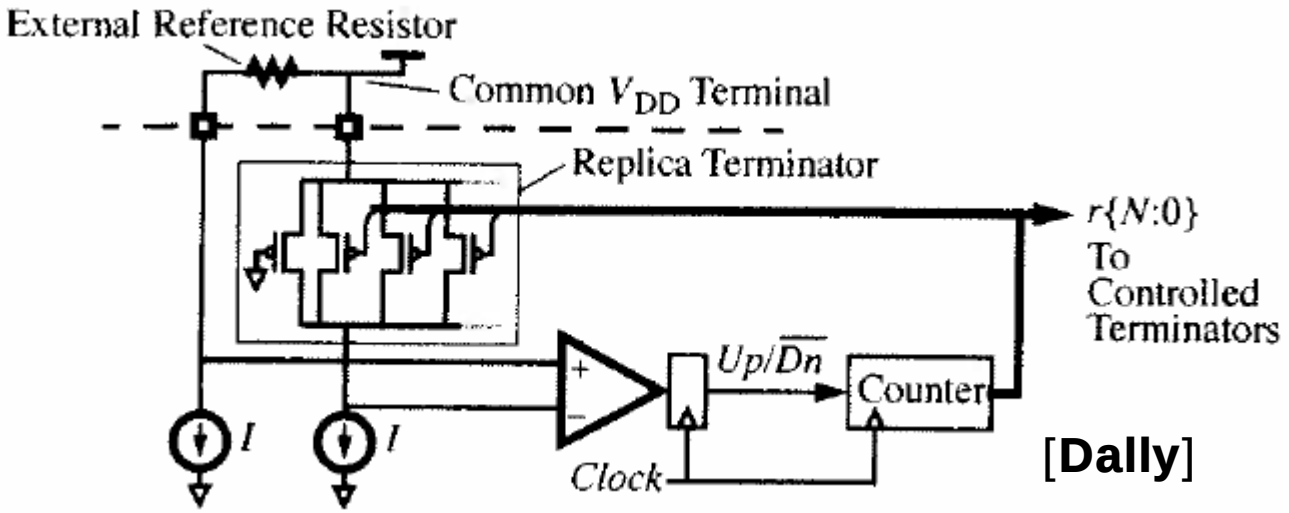
$$R_{FET} = \frac{1}{\mu C_{ox}(W/L)(V_{GS} - V_t)}$$



[**Dally**]

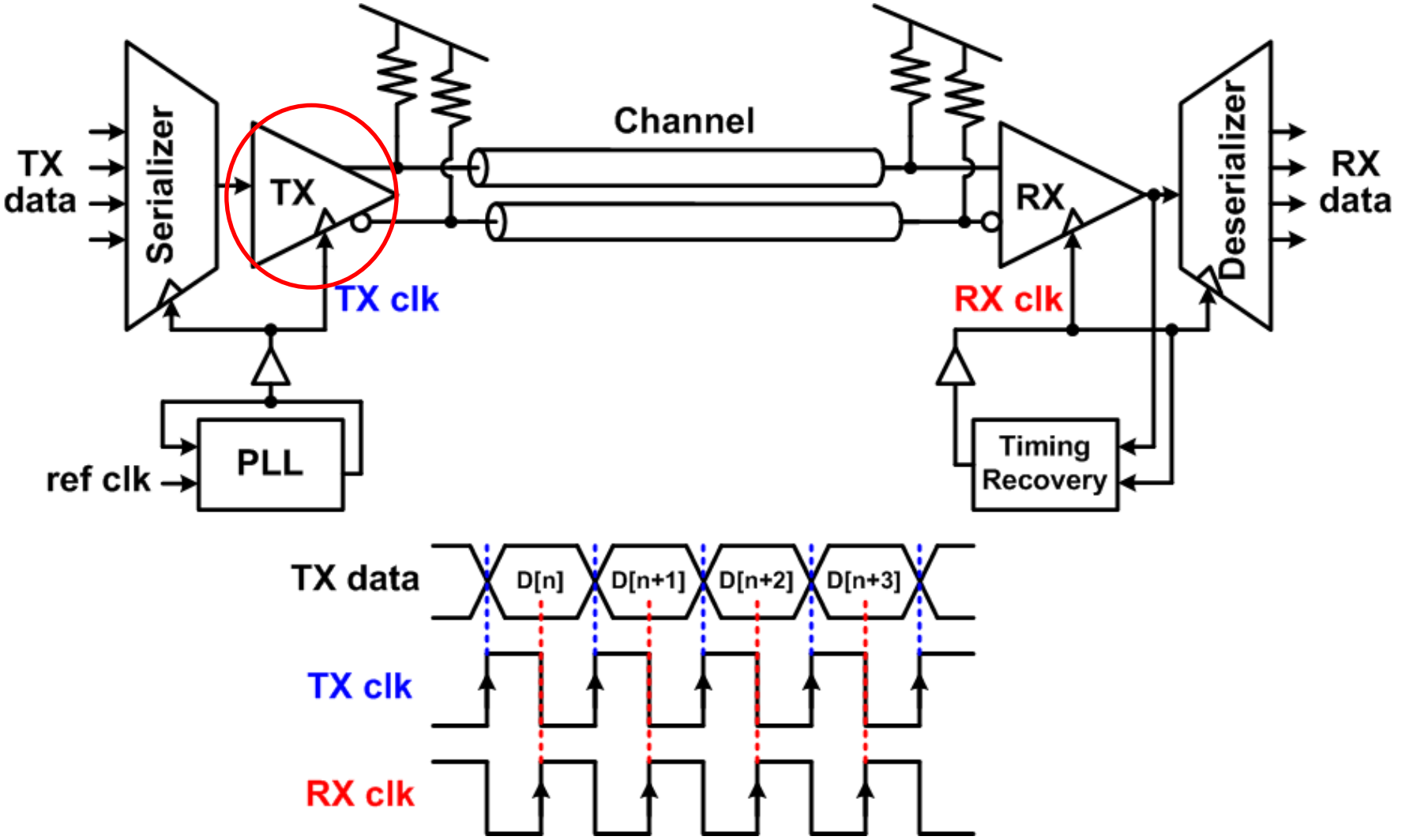
- Large variance in FET threshold voltage requires adjustable termination structures
- Calibration can be done with an analog control voltage or through digital "trimming"
  - Analog control reduces V_{GS} and linear range
  - Digital control is generally preferred

Termination Digital Control Loop



- Off-chip precision resistor is used as reference
- On-chip termination is varied until voltages are within an LSB
  - Dither filter typically used to avoid voltage noise
- Control loop may be shared among several links, but with increased nanometer CMOS variation per-channel calibration may be necessary

High-Speed Electrical Link System

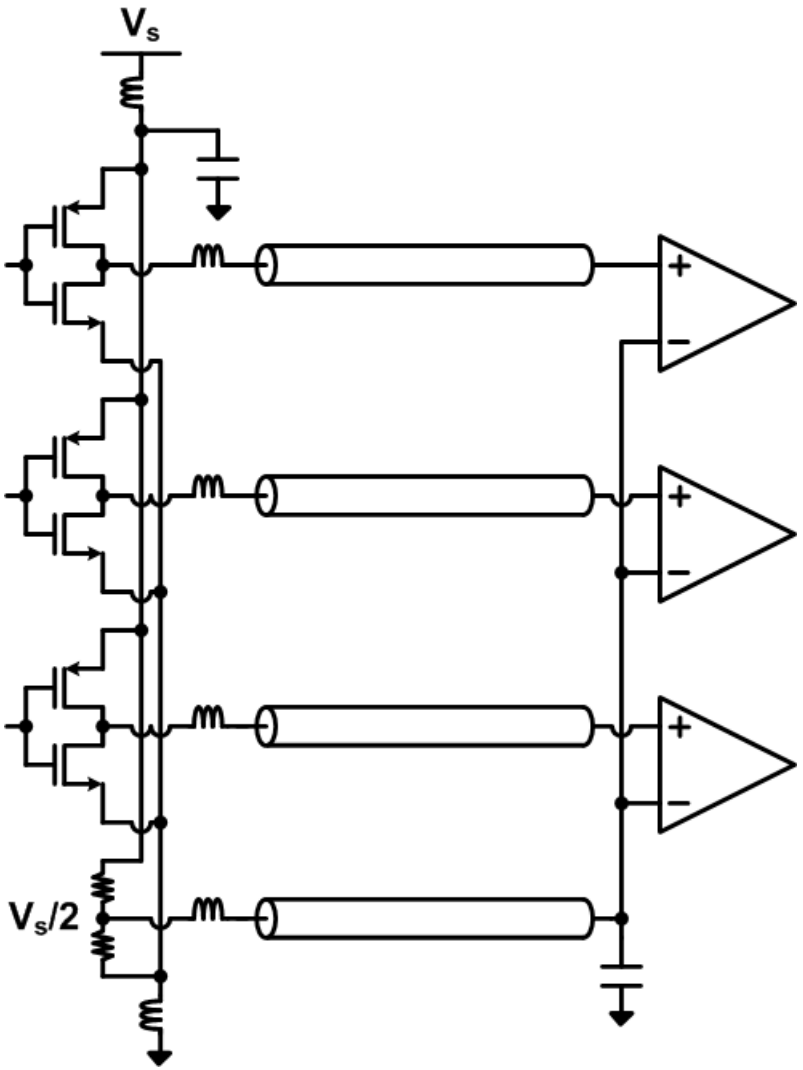


TX Driver Circuits

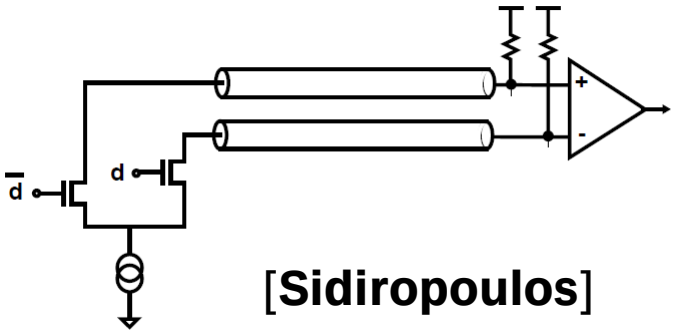
- Single-ended vs differential signaling
- Current-mode drivers
- Voltage-mode drivers
- Slew-rate control

Single-Ended Signaling

- Finite supply impedance causes significant Simultaneous Switching Output (SSO) noise (xtalk)
- Necessitates large amounts of decoupling capacitance for supplies and reference voltage
  - Decap limits I/O area more that circuitry



Differential Signaling

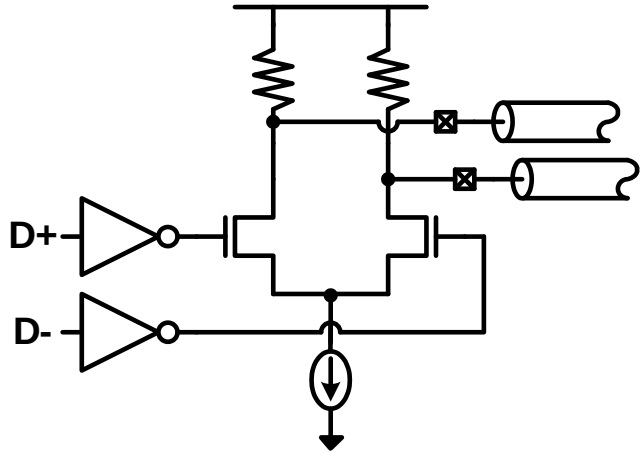


[**Sidiropoulos**]

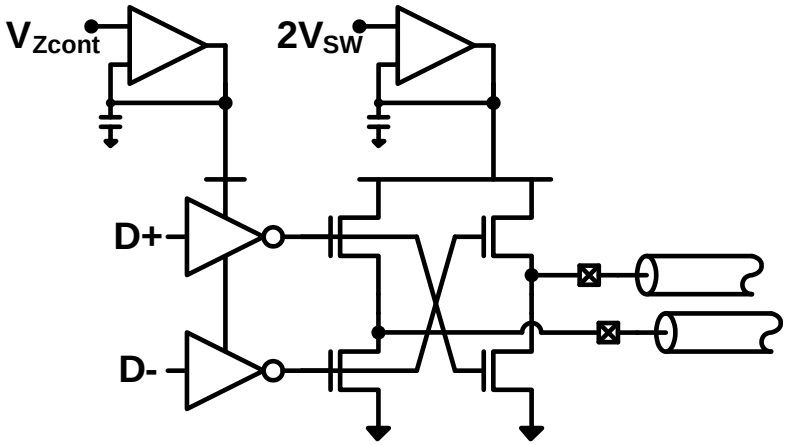
- A difference between voltage or current is sent between two lines
- Requires 2x signal lines relative to single-ended signaling, but less return pins
- Advantages
  - Signal is self-referenced
  - Can achieve twice the signal swing
  - Rejects common-mode noise
  - Return current is ideally only DC

Current vs Voltage-Mode Driver

- Signal integrity considerations (min. reflections) requires 50Ω driver output impedance
- To produce an output drive voltage
  - Current-mode drivers use Norton-equivalent parallel termination
    - Easier to control output impedance
  - Voltage-mode drivers use Thevenin-equivalent series termination
    - Potentially ½ to ¼ the current for a given output swing

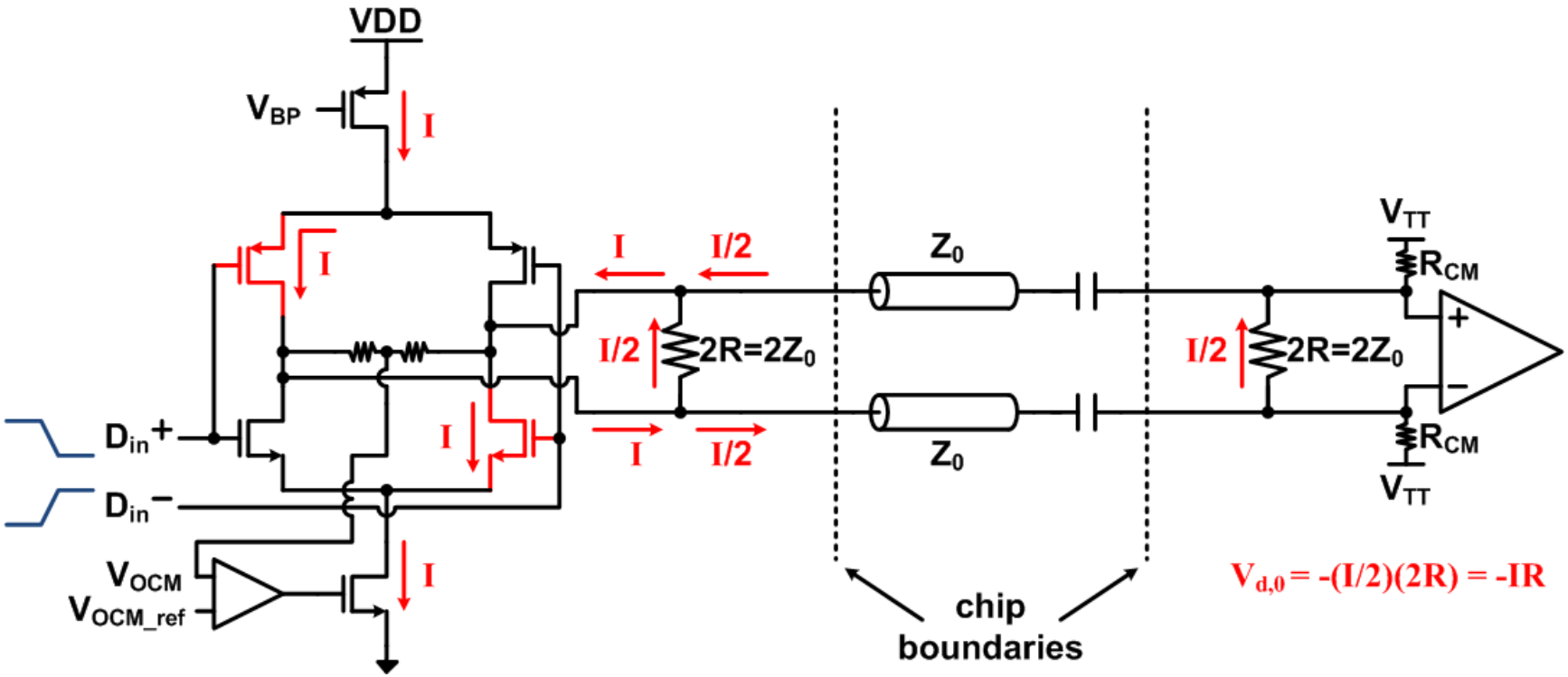


Current-Mode



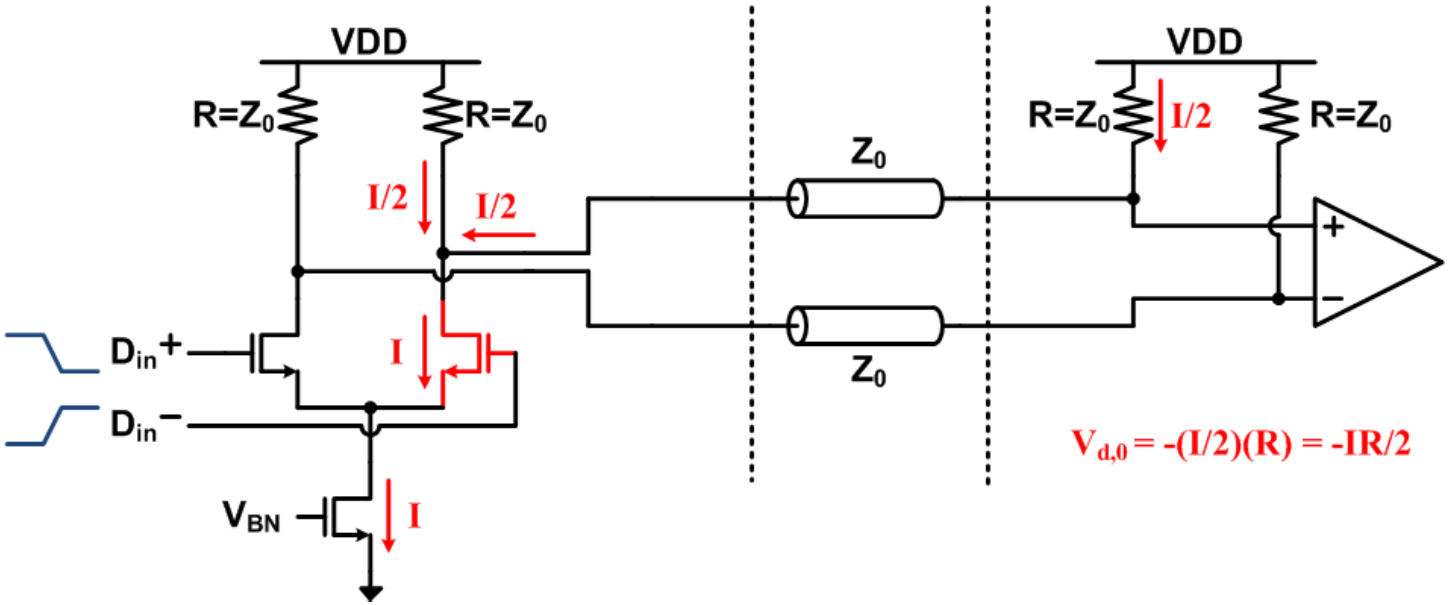
Voltage-Mode

Push-Pull Current-Mode Driver



- Used in Low-Voltage Differential Signals (LVDS) standard
- Driver current is ideally constant, resulting in low dI/dt noise
- Dual current sources allow for good PSRR, but headroom can be a problem in low-voltage technologies
- Differential peak-to-peak RX swing is ±IR with double termination

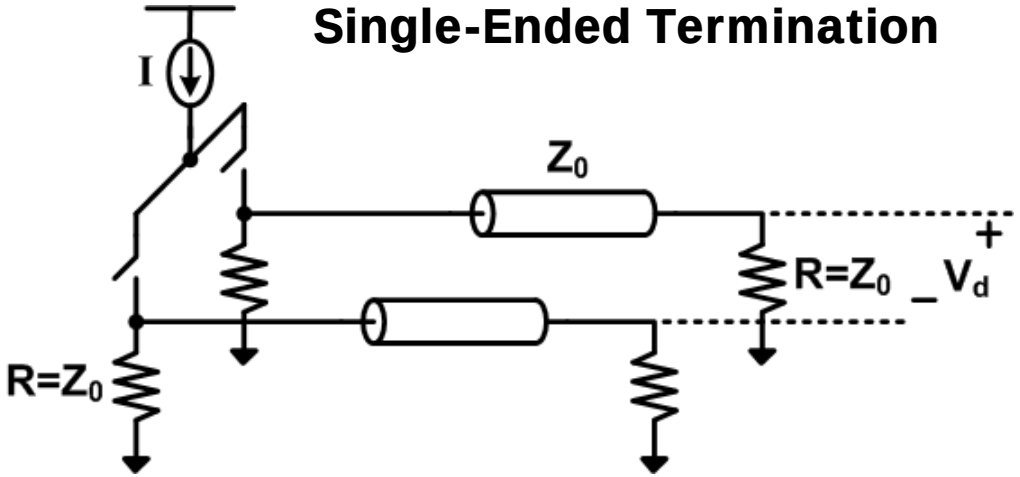
Current-Mode Logic (CML) Driver



- Used in most high performance serial links
- Low voltage operation relative to push-pull driver
  - High output common-mode keeps current source saturated
- Can use DC or AC coupling
  - AC coupling requires data coding
- Differential pp RX swing is ±IR/2 with double termination

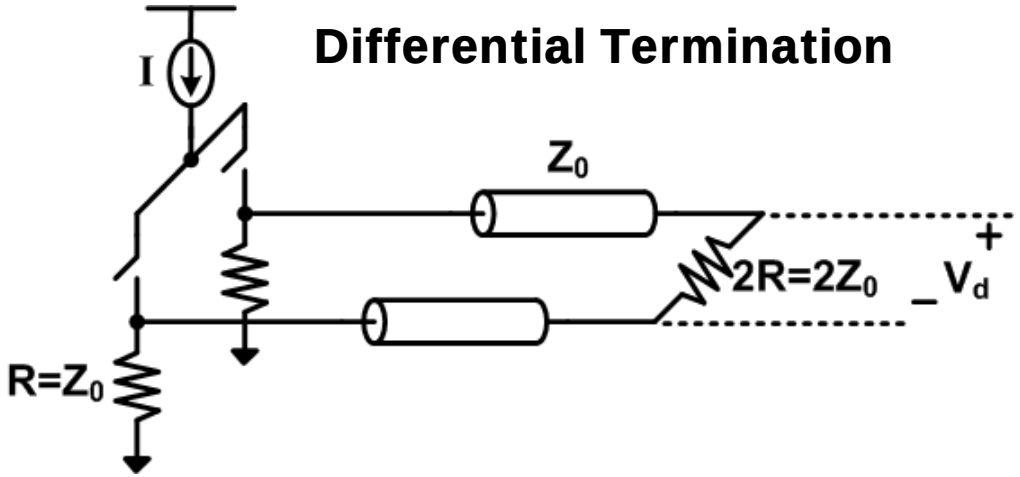
Current-Mode Current Levels

Single-Ended Termination



$$V_{d,1} = (I/2)R$$
$$V_{d,0} = -(I/2)R$$
$$V_{d,pp} = IR$$
$$\boldsymbol{I = \frac{V_{d,pp}}{R}}$$

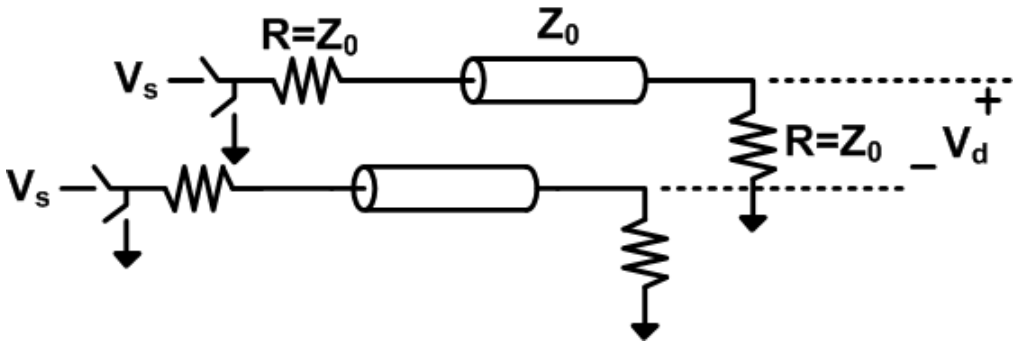
Differential Termination



$$V_{d,1} = (I/4)(2R)$$
$$V_{d,0} = -(I/4)(2R)$$
$$V_{d,pp} = IR$$
$$\boldsymbol{I = \frac{V_{d,pp}}{R}}$$

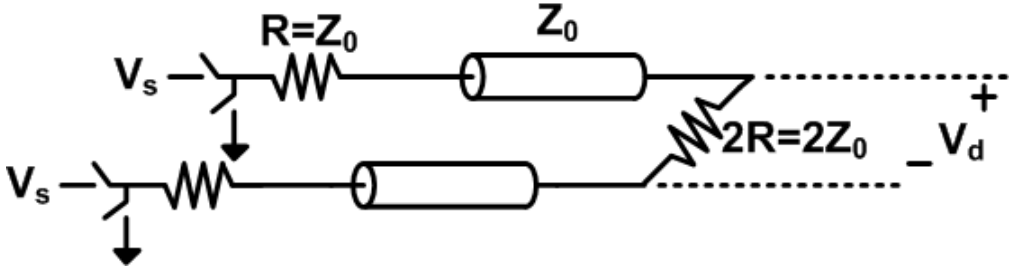
Voltage-Mode Current Levels

Single-Ended Termination



$$V_{d,1} = (V_s/2)$$
$$V_{d,1} = -(V_s/2)$$
$$V_{d,pp} = V_s$$
$$I = (V_s/2R)$$
$$\boldsymbol{I = \frac{V_{d,pp}}{2R}}$$

Differential Termination



$$V_{d,1} = (V_s/2)$$
$$V_{d,1} = -(V_s/2)$$
$$V_{d,pp} = V_s$$
$$I = (V_s/4R)$$
$$\boldsymbol{I = \frac{V_{d,pp}}{4R}}$$

Current-Mode vs Voltage-Mode Summary

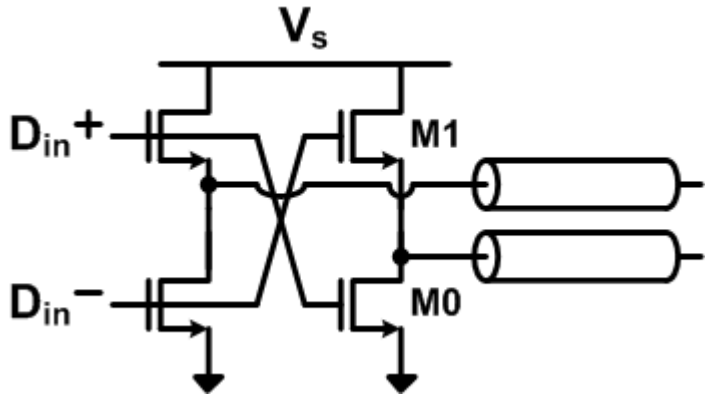
Driver / Termination	Current Level	Normalized Current Level
Current-Mode/SE	$V_{d,pp}/Z_0$	1x
Current-Mode/Diff	$V_{d,pp}/Z_0$	1x
Voltage-Mode/SE	$V_{d,pp}/2Z_0$	0.5x
Voltage-Mode/Diff	$V_{d,pp}/4Z_0$	0.25x

- An ideal voltage-mode driver with differential RX termination enables a *potential* 4x reduction in driver power
- *Actual* driver power levels also depend on
  - Output impedance control
  - Pre-driver power
  - Equalization implementation

Voltage-Mode Drivers

- Voltage-mode driver implementation depends on output swing requirements
- For low-swing (<400-500mVpp), an all NMOS driver is suitable
- For high-swing, CMOS driver is used

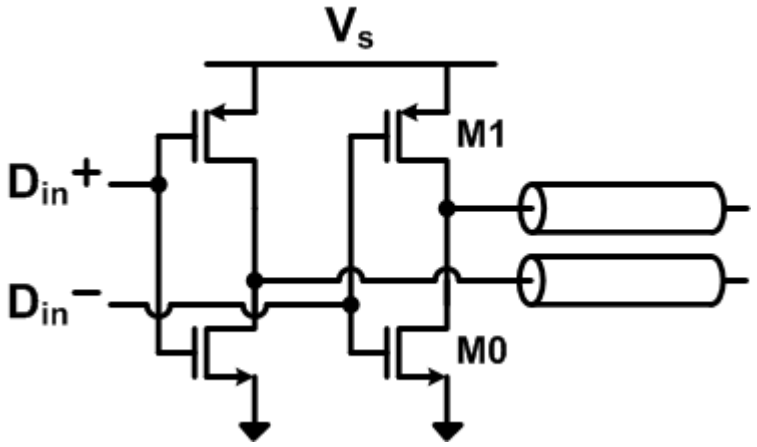
Low-Swing Voltage-Mode Driver



$$V_s < \frac{4}{3}\left(VDD - V_{t1} - V_{OD1}\right) \text{ (Diff. Term)}$$

$$V_s < 2\left(VDD - V_{t1} - V_{OD1}\right) \text{ (SE Term)}$$

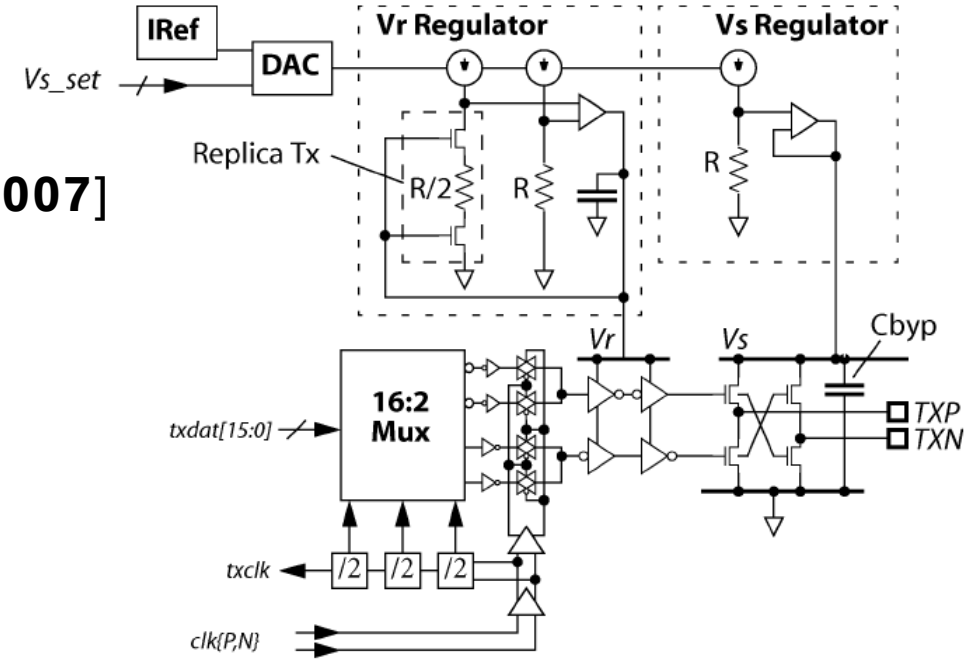
High-Swing Voltage-Mode Driver



$$V_s > \left|V_{t1}\right| + V_{OD1}$$

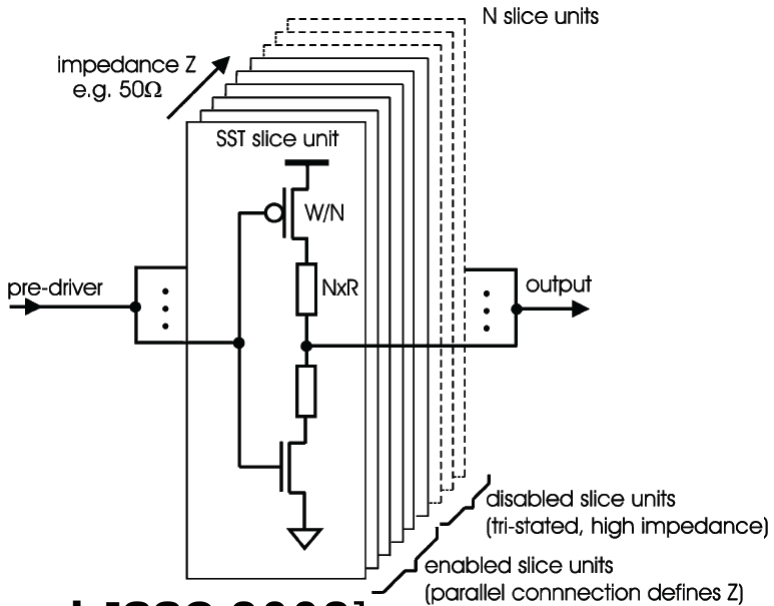
Low-Swing VM Driver Impedance Control

[**Poulton JSSC 2007**]

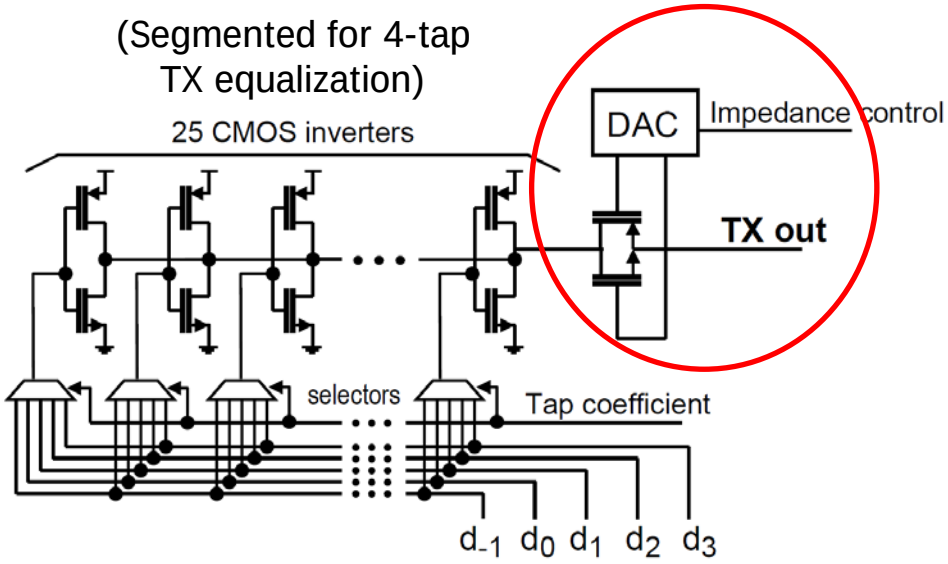


- A linear regulator sets the output stage supply, V_s
- Termination is implemented by output NMOS transistors
- To compensate for PVT and varying output swing levels, the pre-drive supply is adjusted with a feedback loop
- The top and bottom output stage transistors need to be sized differently, as they see a different V_{OD}

High-Swing VM Driver Impedance Control



[**Kossel JSSC 2008**]



[**Fukada ISSCC 2008**]

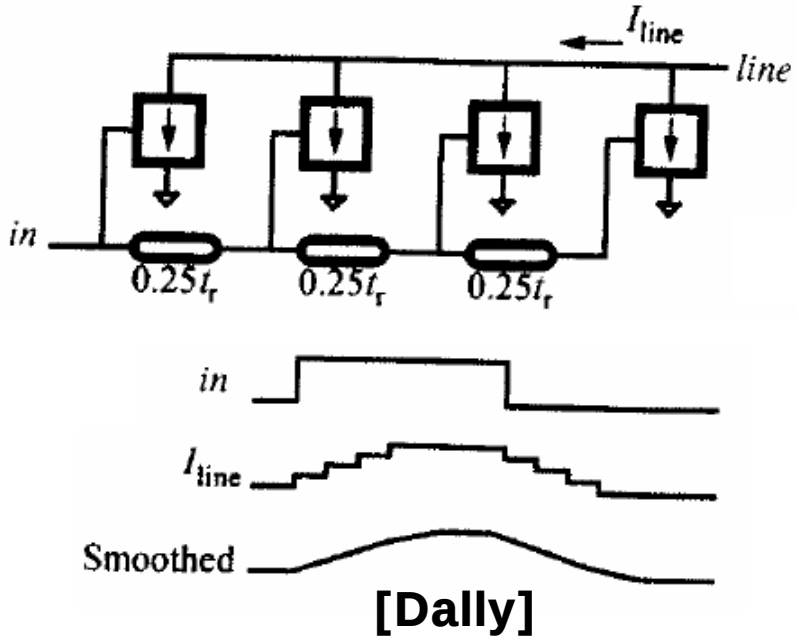
- High-swing voltage-mode driver termination is implemented with a combination of output driver transistors and series resistors
- To meet termination resistance levels (50Ω), large output transistors are required
  - Degrades potential power savings vs current-mode driver

TX Driver Slew Rate Control

- Output transition times should be controlled
  - Too slow
    - Limits max data rate
  - Too fast
    - Can excite resonant circuits, resulting in ISI due to ringing
    - Cause excessive crosstalk
- Slew rate control reduces reflections and crosstalk

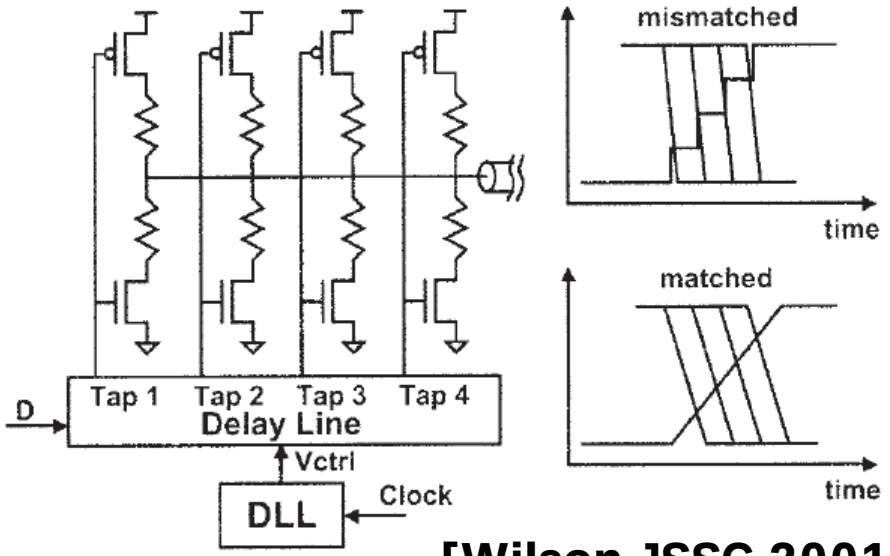
Slew Rate Control w/ Segmented Driver

Current-Mode Driver



[Dally]

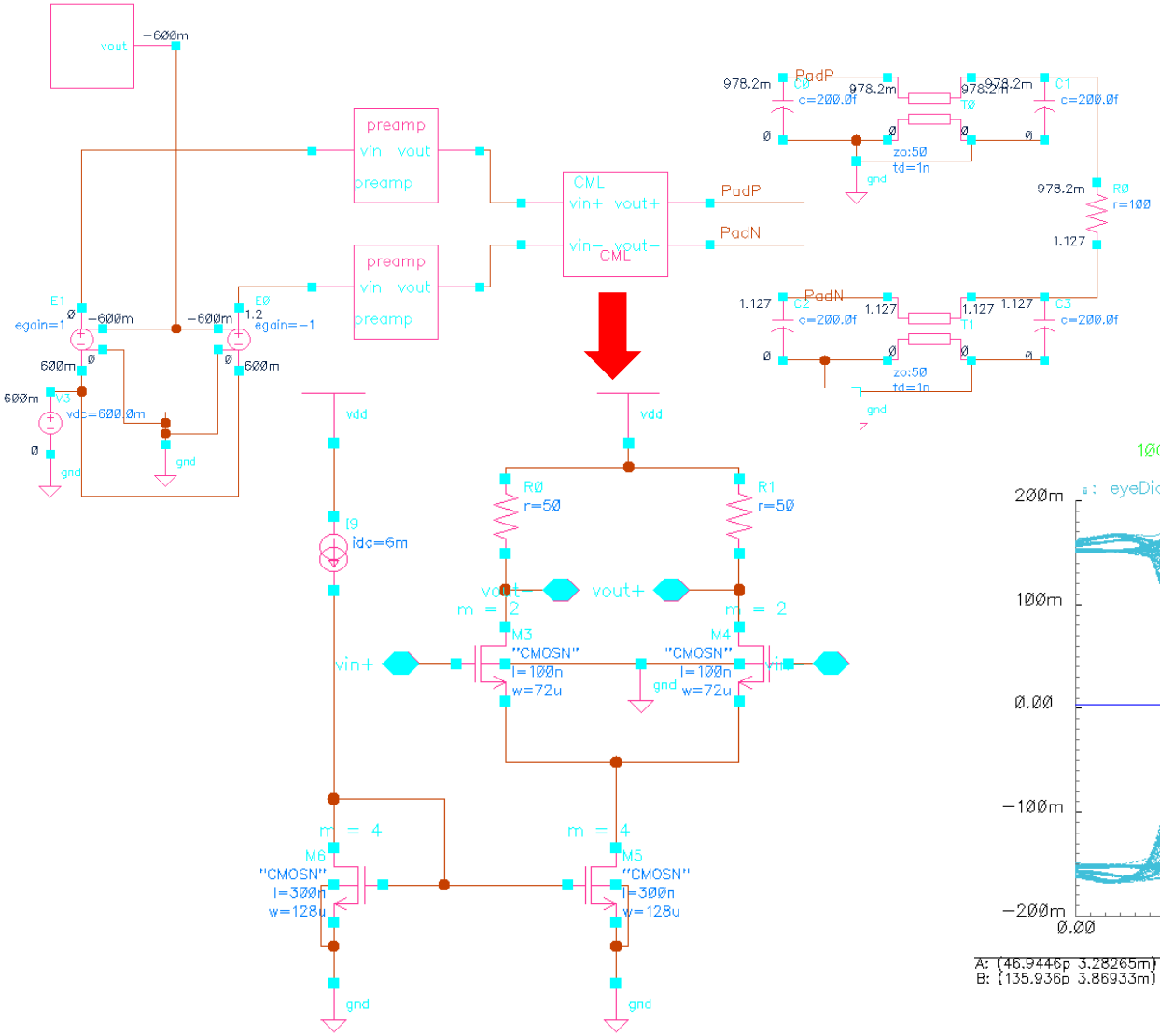
Voltage-Mode Driver

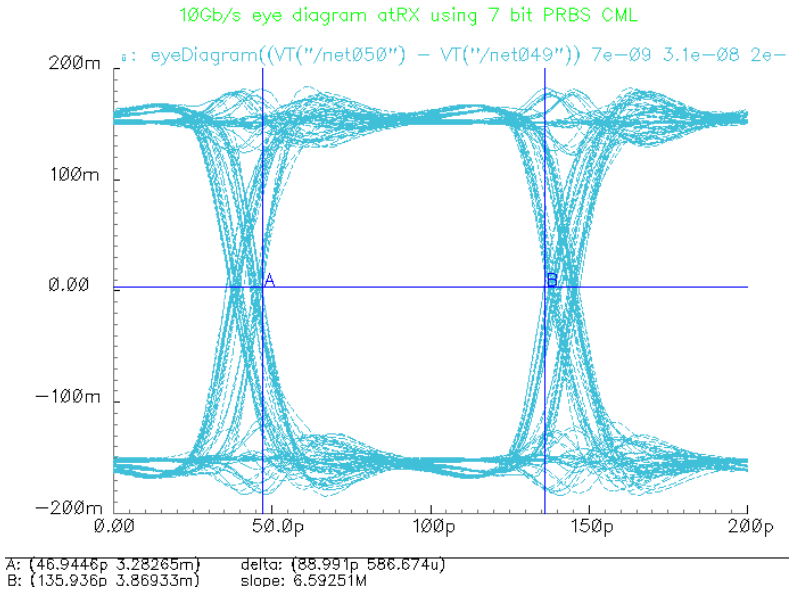


[Wilson JSSC 2001]

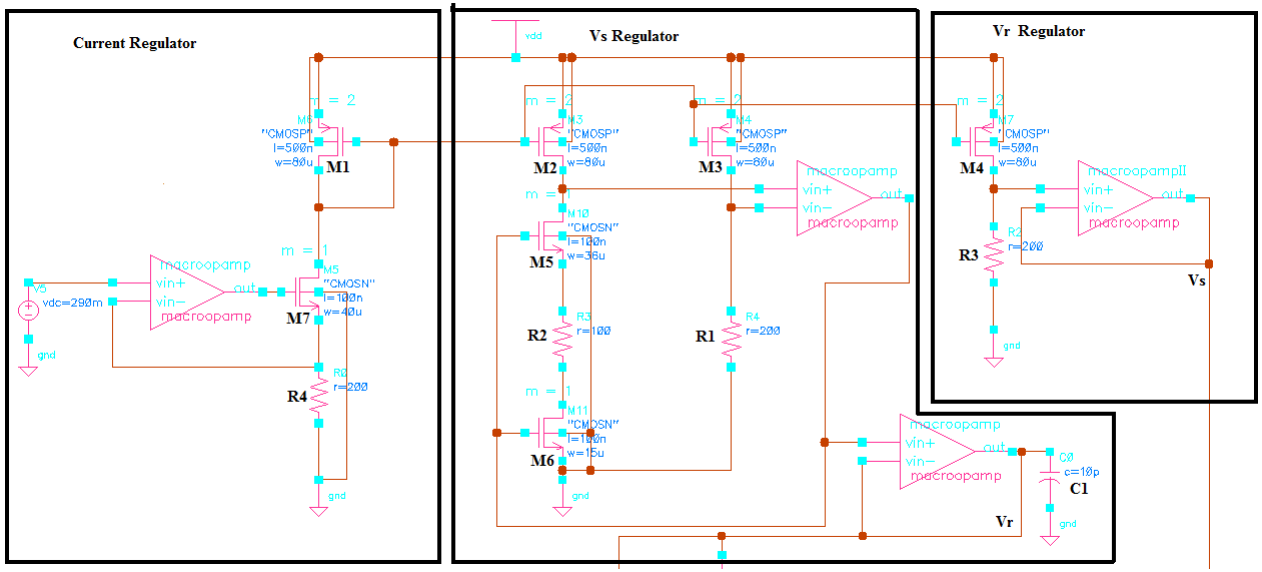
- Slew rate control can be implemented with a segmented output driver
- Segments turn-on time are spaced by 1/n of desired transition time
- Predriver transition time should also be controlled

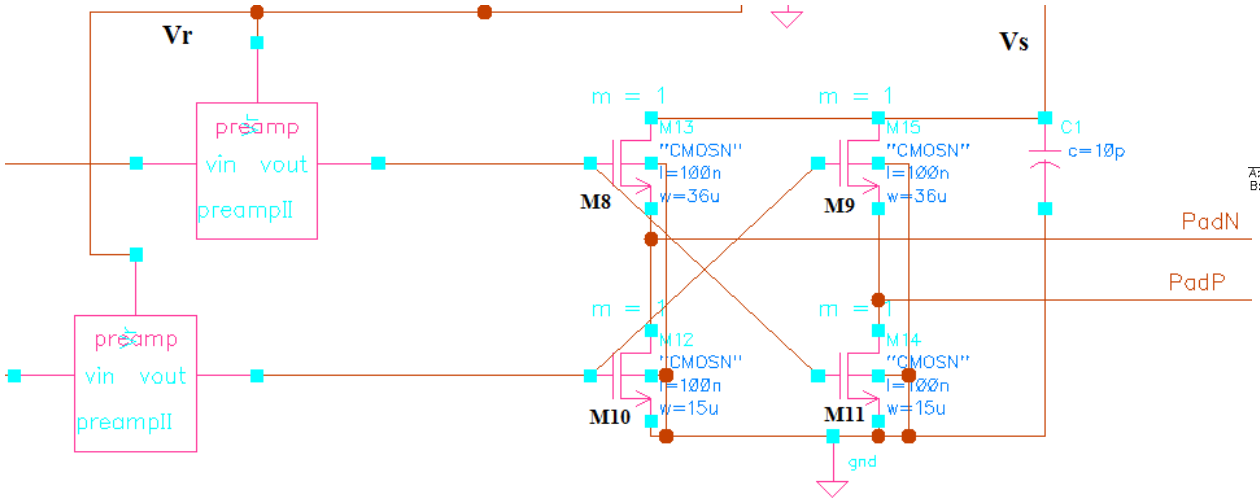
Current-Mode Driver Example

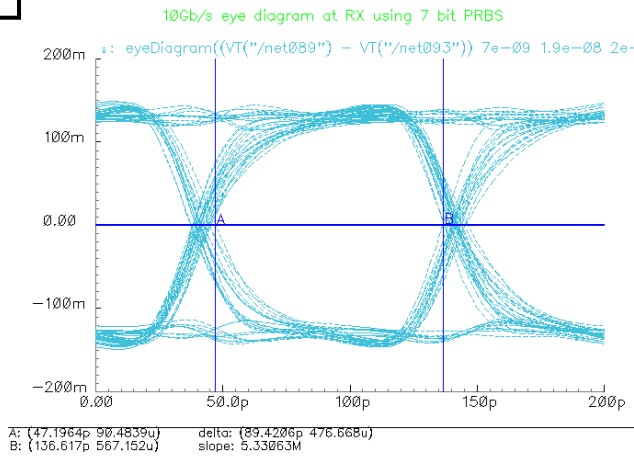




Voltage-Mode Driver Example







Next Time

- TX circuit speed limitations
  - Clock distribution
  - Multiplexing circuits
- Receiver Circuits