ECEN689: Special Topics in High-Speed Links Circuits and Systems
Spring 2010

Lecture 32: CDR Wrap-Up

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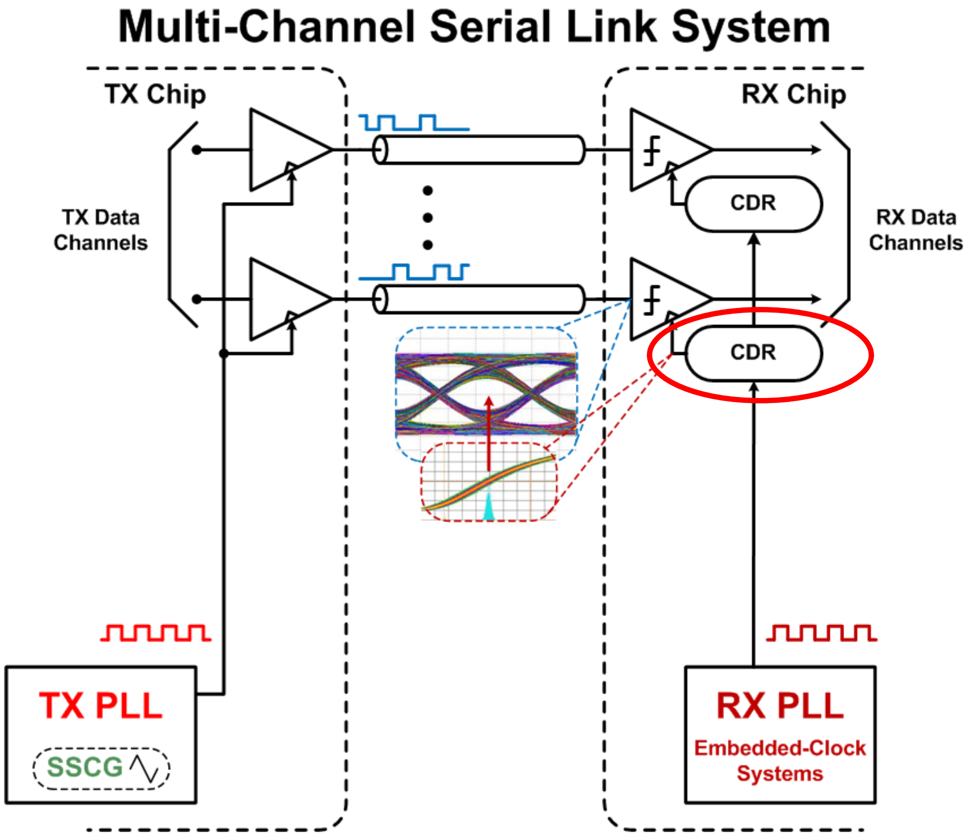
Announcements

- Exam 2 is April 30
  - Will emphasize (but not limited to)
    - Equalization properties & circuits
    - Link Budgeting (noise & timing)
    - PLLs
    - CDRs (high-level properties)
- Project Feedback meetings on Friday
- Final Project Report Due May 4

Agenda

- CDR circuits
  - PI
  - DLL
- CDR Jitter Properties
- Injection-Locked Oscillator De-Skew

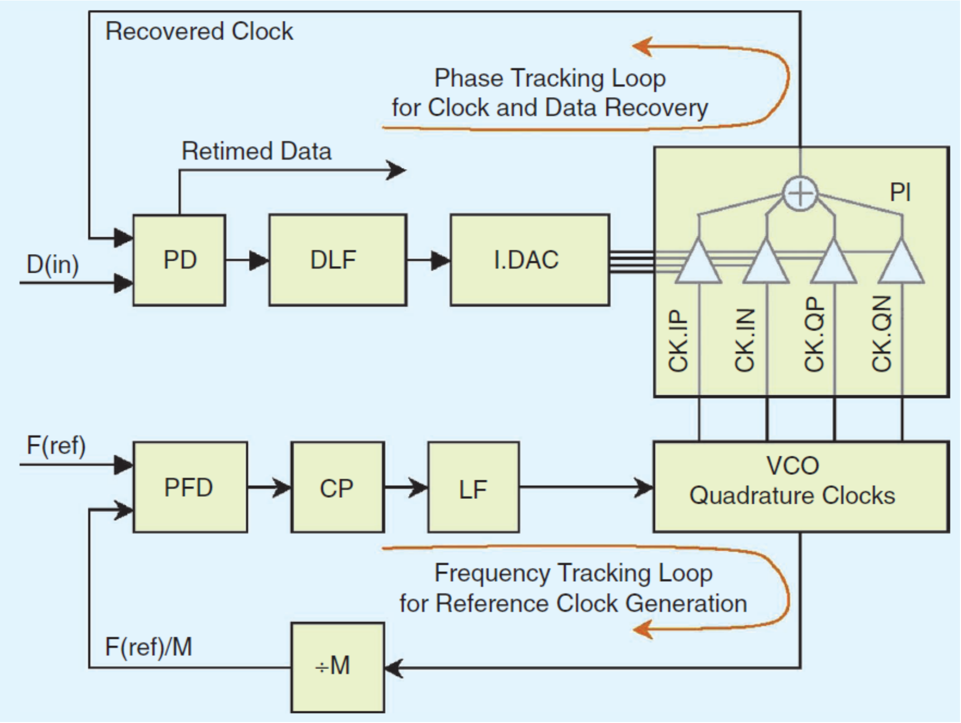
Embedded Clock I/O Circuits



- TX PLL
- TX Clock Distribution
- CDR
  - Per-channel PLL-based
  - Dual-loop w/ Global PLL &
    - Local DLL/PI
    - Local Phase-Rotator PLLs
    - Global PLL requires RX clock distribution to individual channels

Phase Interpolator (PI) Based CDR

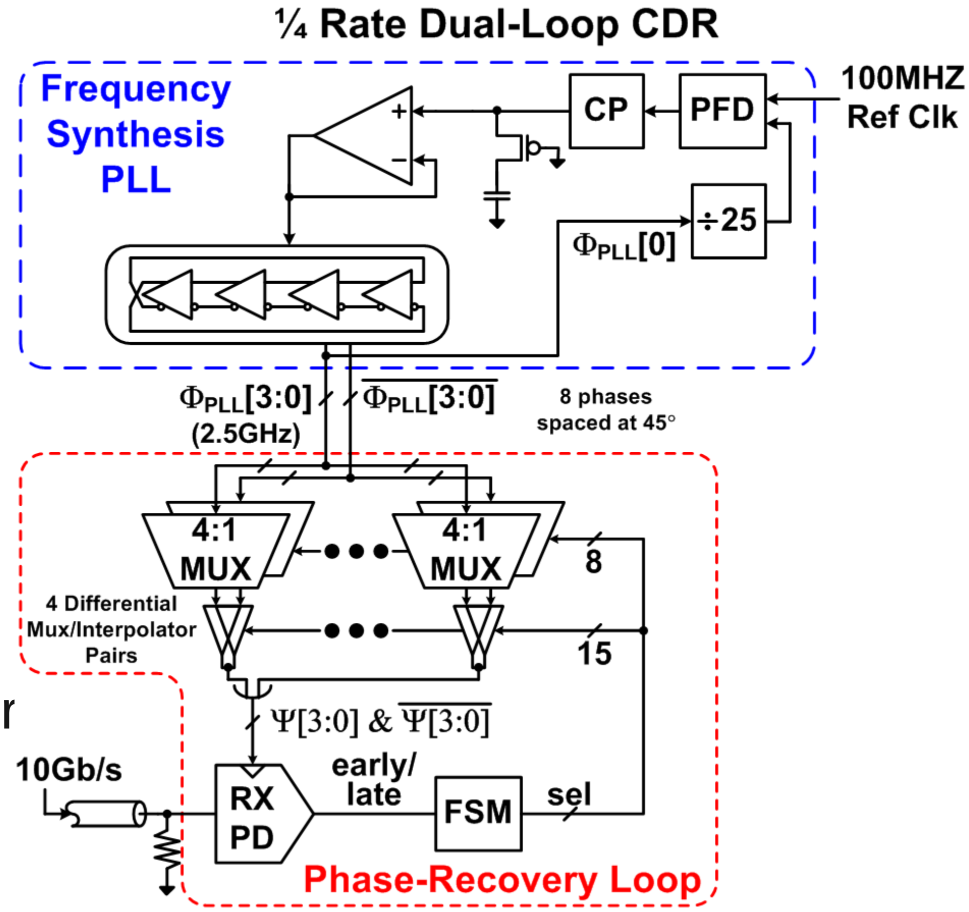
- Frequency synthesis loop produces multiple clock phases used by the phase interpolators
- Phase interpolator mixes between input phases to produce a fine sampling phase
  - Ex: Quadrature 90° PI inputs with 5 bit resolution provides sampling phases spaced by $90°/(2^5\text{-}1)=2.9°$
- Digital phase tracking loop offers advantages in robustness, area, and flexibility to easily reprogram loop parameters



[Hsieh]

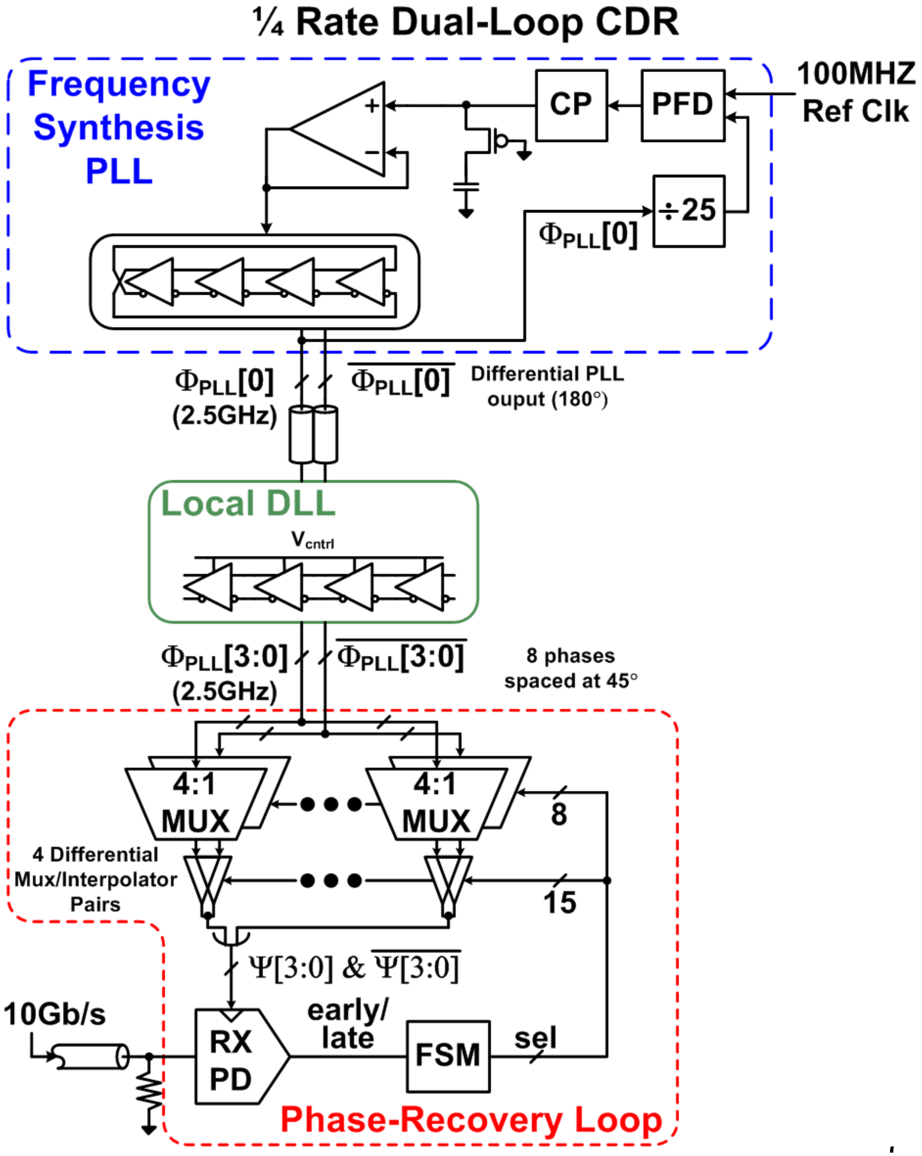
Phase Interpolator (PI) Based CDR

- Frequency synthesis loop can be a global PLL
- Can be difficult to distribute multiple phases long distance
  - Need to preserve phase spacing
  - Clock distribution power increases with phase number
  - If CDR needs more than 4 phases consider local phase generation



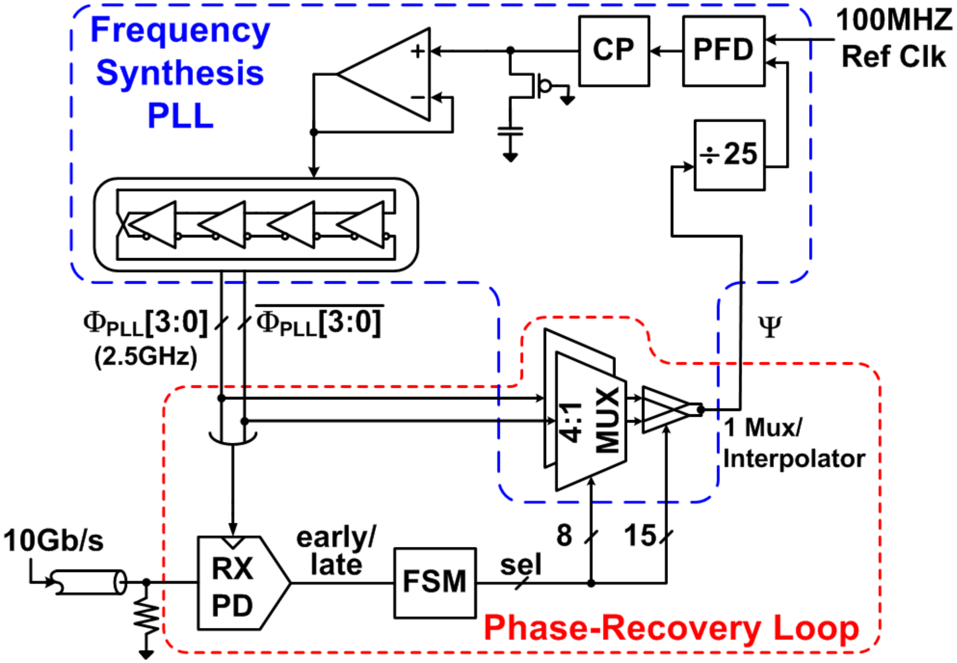
DLL Local Phase Generation

- Only differential clock is distributed from global PLL
- Delay-Locked Loop (DLL) locally generates the multiple clock phases for the phase interpolators
  - DLL can be per-channel or shared by a small number (4)
- Same architecture can be used in a forwarded-clock system
  - Replace frequency synthesis PLL with forwarded-clock signals



Phase Rotator PLL

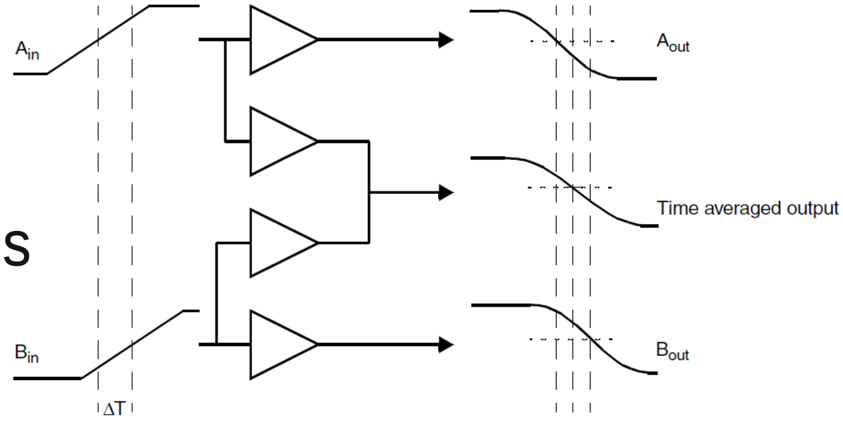
- Phase interpolators can be expensive in terms of power and area
- Phase rotator PLL places **one** interpolator in PLL feedback to adjust all VCO output phases simultaneously
- Now frequency synthesis and phase recovery loops are coupled
  - Need PLL bandwidth greater than phase loop
    - Useful in filtering VCO noise

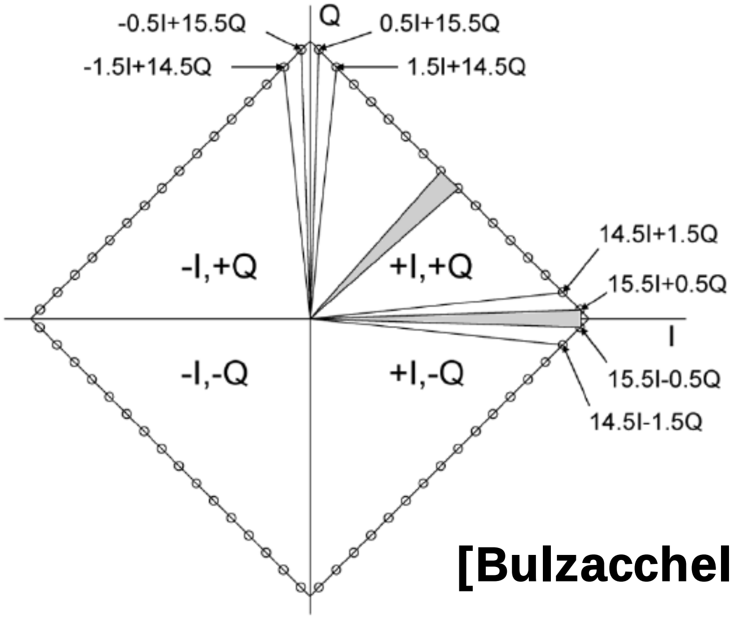


Phase Interpolators

- Phase interpolators realize digital-to-phase conversion (DPC)
- Produce an output clock that is a weighted sum of two input clock phases
- Common circuit structures
  - Tail current summation interpolation
  - Voltage-mode interpolation
- Interpolator code mapping techniques
  - Sinusoidal
  - Linear

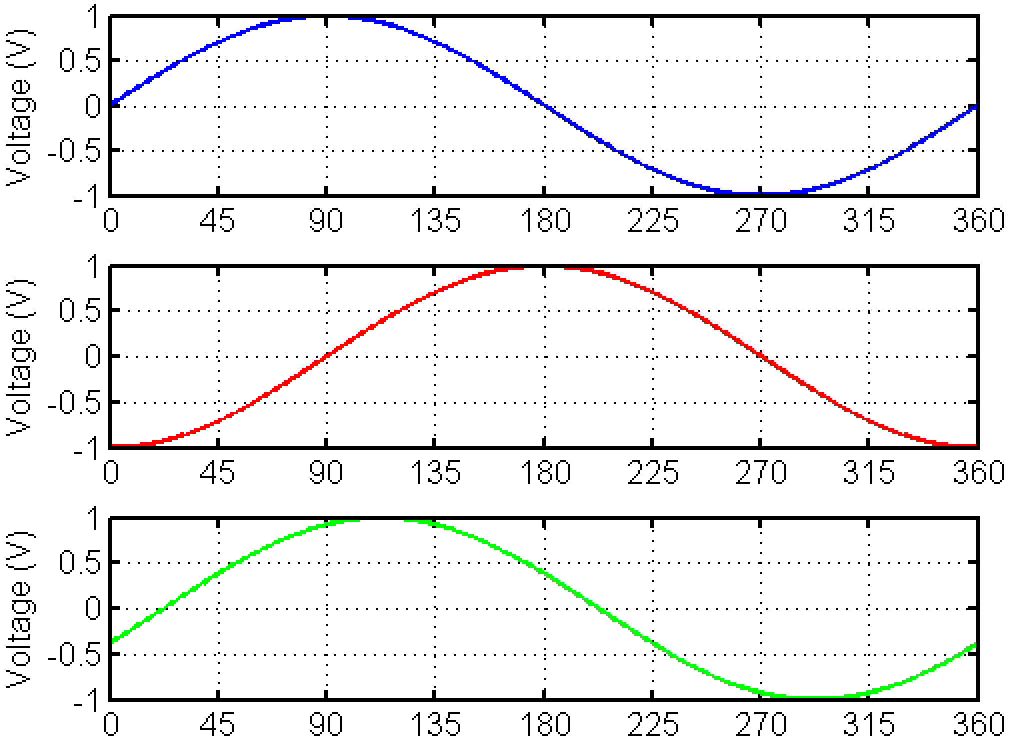
[Weinlader]

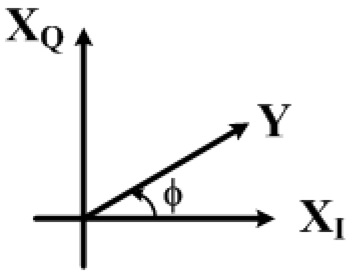




[Bulzacchelli]

Sinusoidal Phase Interpolation





$$X_I = A\sin(\omega t)$$

$$X_Q = A\sin(\omega t - \pi/2) = -A\cos(\omega t)$$

$$\begin{aligned} Y &= A\sin(\omega t - \phi) \\ &= A\cos(\phi)\sin(\omega t) - A\sin(\phi)\cos(\omega t) \quad \left(0 \le \phi \le \frac{\pi}{2}\right) \\ &= \cos(\phi)X_I + \sin(\phi)X_Q = a_1 X_I + a_2 X_Q \end{aligned}$$

- Arbitrary phase shift can be generated with linear summation of I/Q clock signal

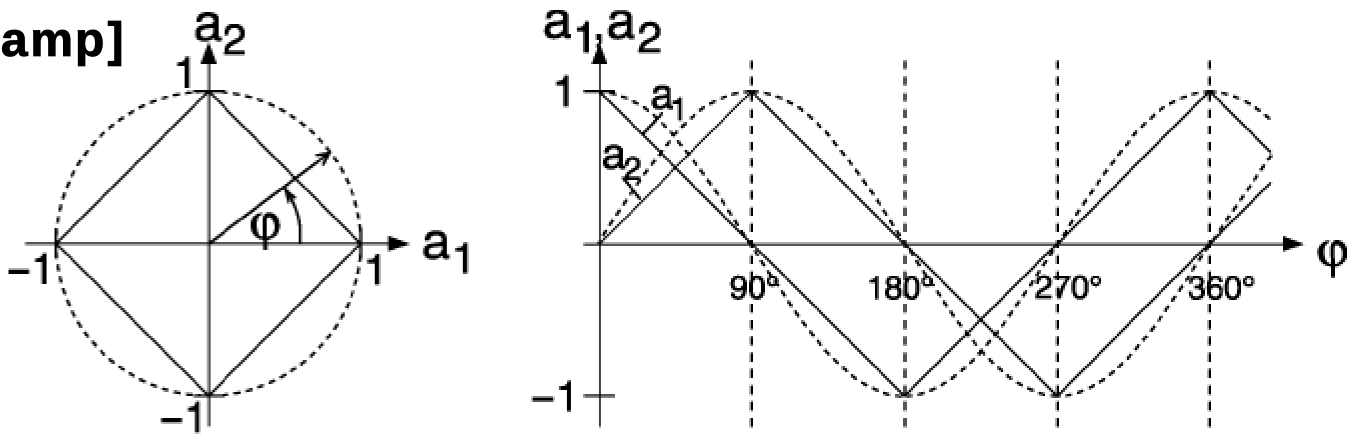
$$Y = A\sin(\omega t - \phi) = a_1 X_1 + a_2 X_Q$$

$$\textbf{where } a_1 = \cos(\phi) \textbf{ and } a_2 = \sin(\phi)$$

$$a_1^2 + a_2^2 = 1$$

Sinusoidal vs Linear Phase Interpolation

[Kreienkamp]

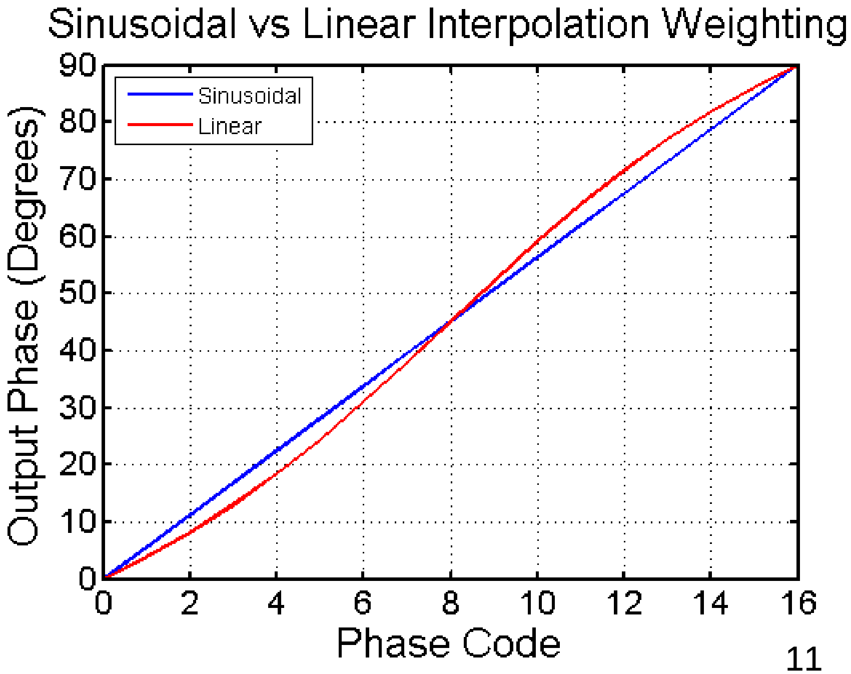


- It can be difficult to generate a circuit that implements sinusoidal weighting

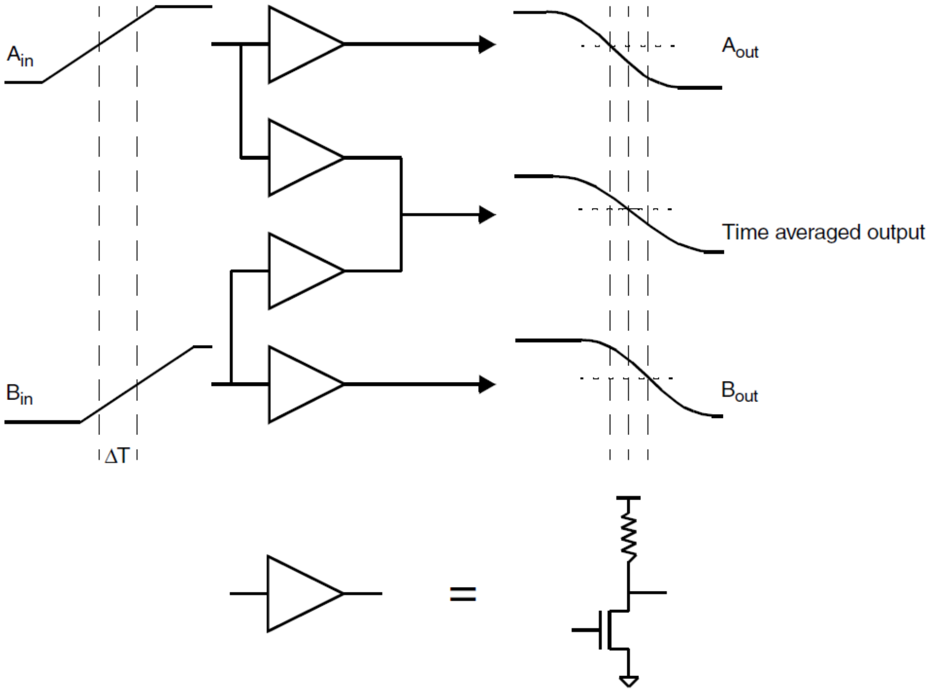
$$a_1^2 + a_2^2 = 1$$

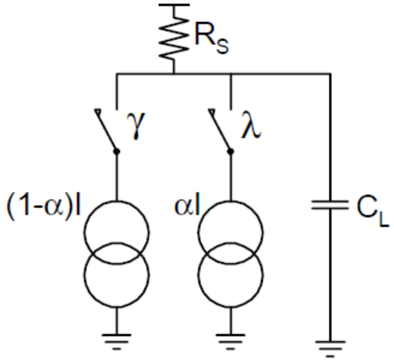
- In practice, a linear weighting is often used

$$a_1 + a_2 = 1$$



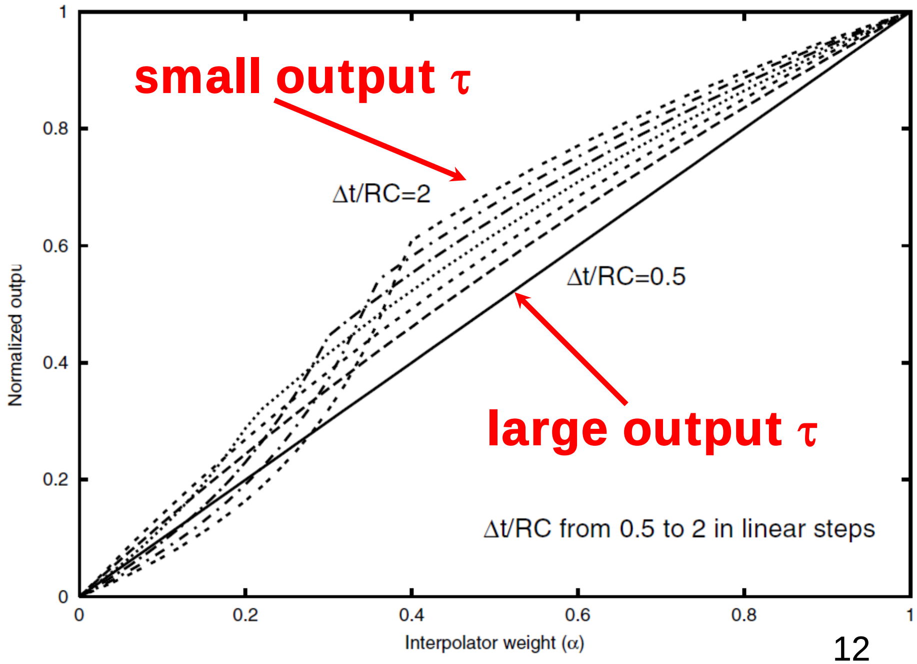
Phase Interpolator Model





- Interpolation linearity is a function of the phase spacing, Δt, to ouput time constant, RC, ratio

w/ ideal step inputs



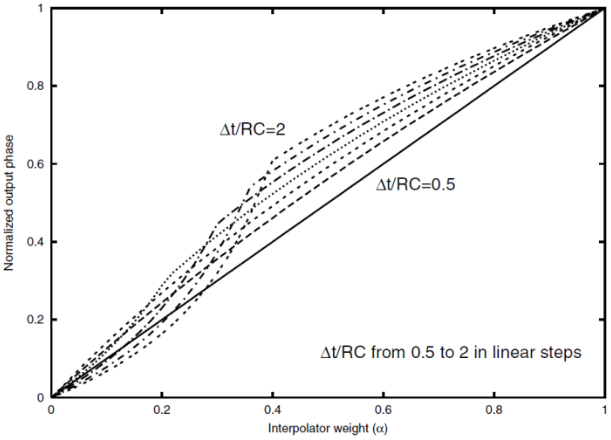
small output τ

large output τ

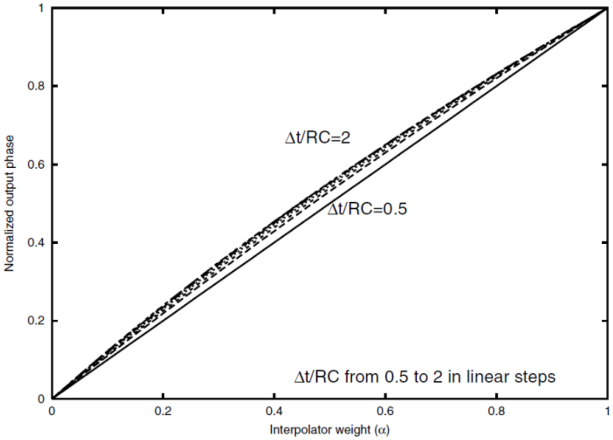
Δt/RC from 0.5 to 2 in linear steps

Phase Interpolator Model

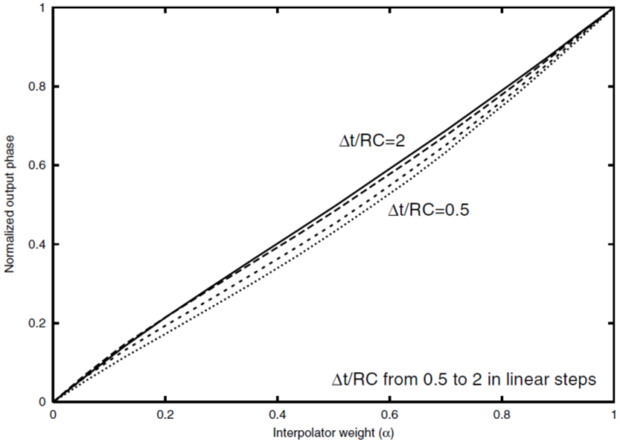
w/ ideal step inputs



w/ finite input transition time



Spice simulation



w/ ideal step inputs:

$$V_o(t) = V_{cc} + R \cdot I \cdot \left[(1-\alpha) \cdot u(t) \cdot \left(e^{-\frac{t}{RC}} - 1\right) + \alpha \cdot u(t-\Delta t) \cdot \left(e^{-\frac{t-\Delta t}{RC}} - 1\right)\right]$$

w/ finite input transition time:

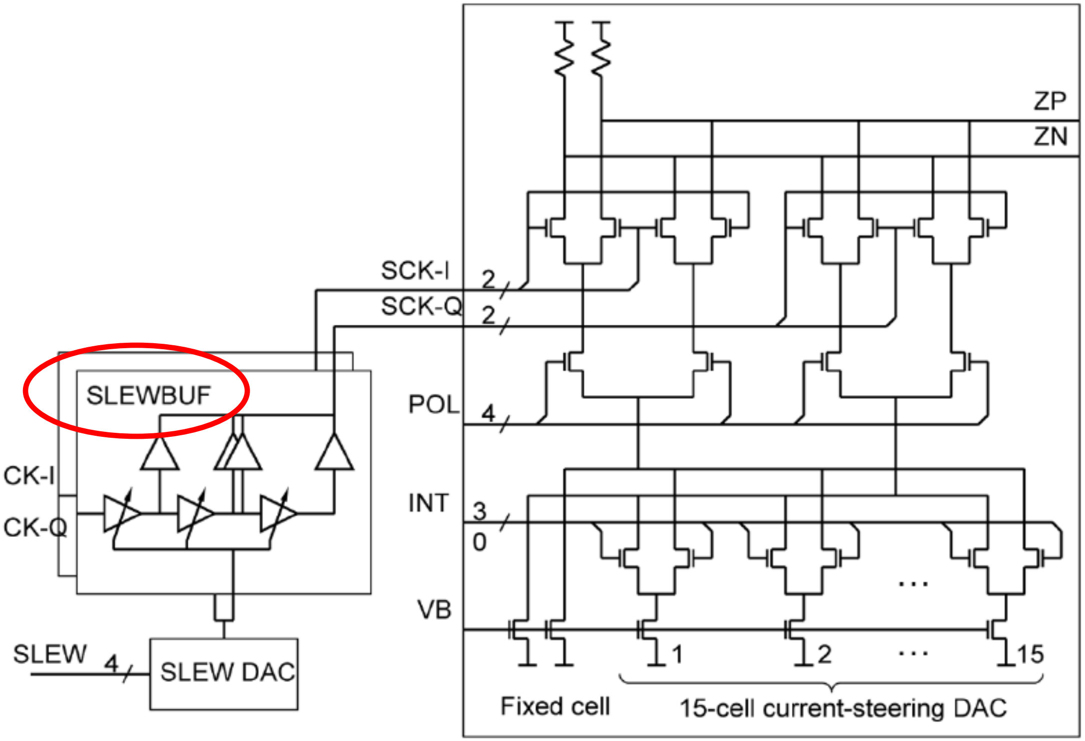
$$V_o(t) = V_{cc} + (1-\alpha) \cdot \frac{I_{max} \cdot t}{\Delta t} \cdot R \cdot \alpha \cdot [u(t) - u(t-\Delta t)] \cdot \left(e^{-\frac{t}{RC}} - 1\right) +$$

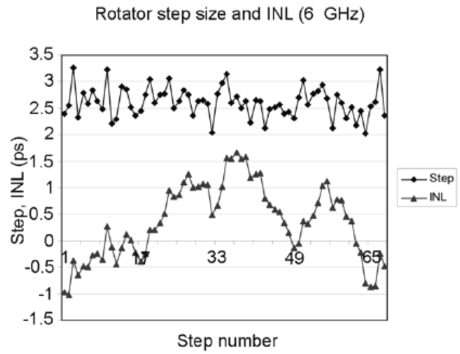
$$\alpha \cdot \frac{I_{max} \cdot t}{\tau_r} \cdot R \cdot [u(t-\Delta t) - u(t-3\Delta t)] \cdot \left(e^{-\frac{t-\Delta t}{RC}} - 1\right).$$

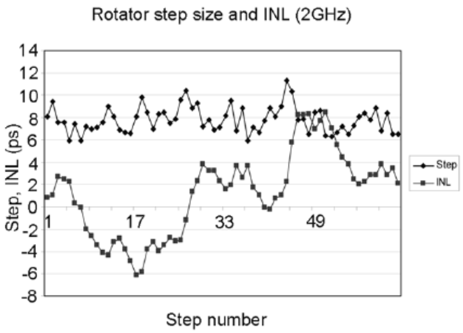
For more details see D. Weinlader’s Stanford PhD thesis

Tail-Current Summation PI

[Bulzacchelli JSSC 2006]



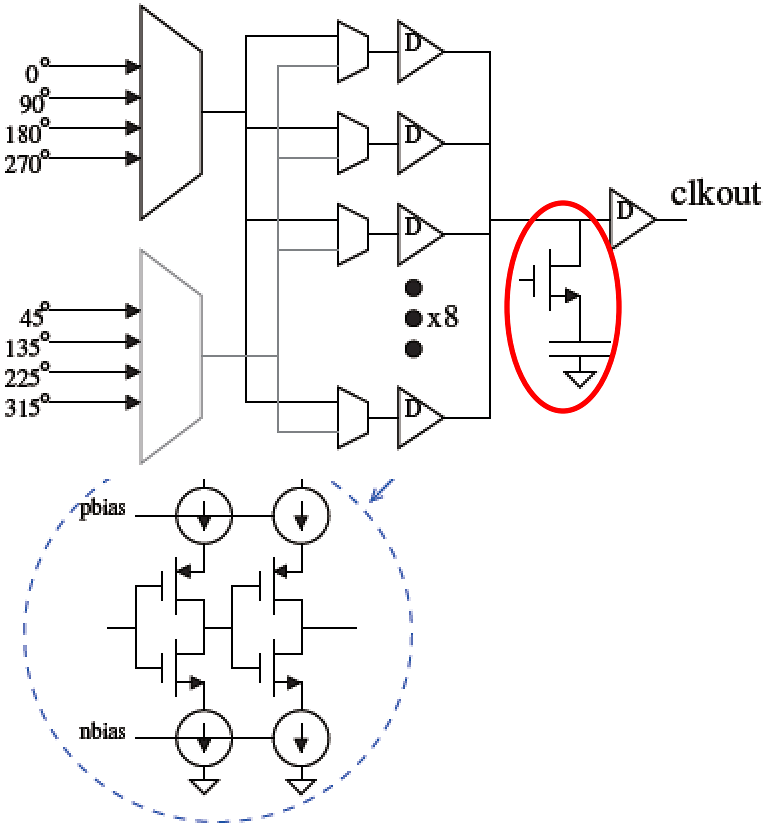

Rotator step size and INL (6 GHz)

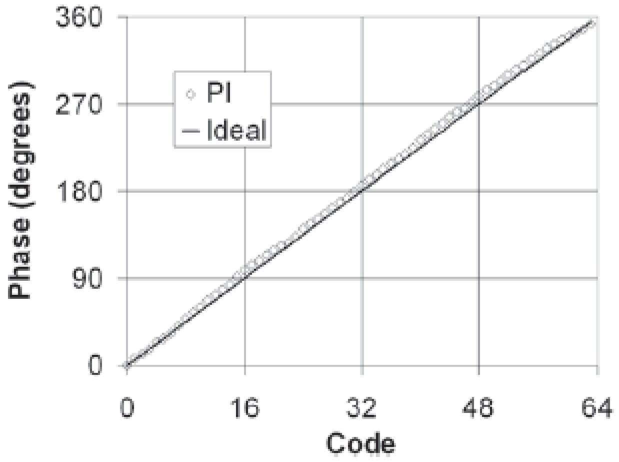

Rotator step size and INL (2GHz)

- For linearity over a wide frequency range, important to control either input or output time constant (slew rate)

Voltage-Mode Summation PI

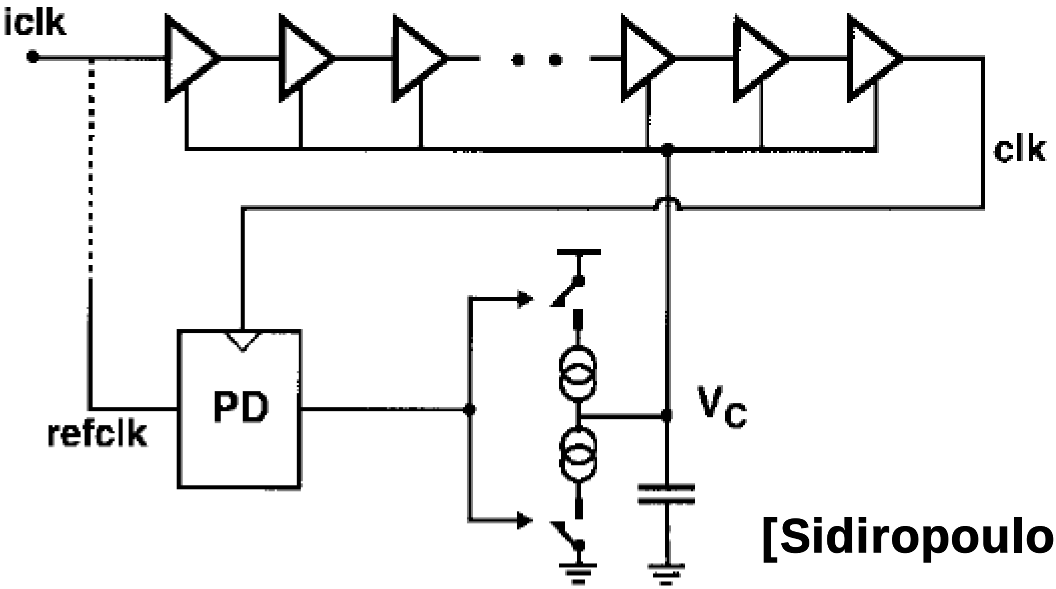
[Joshi VLSI Symp 2009]





- For linearity over a wide frequency range, important to control either input or output time constant (slew rate)

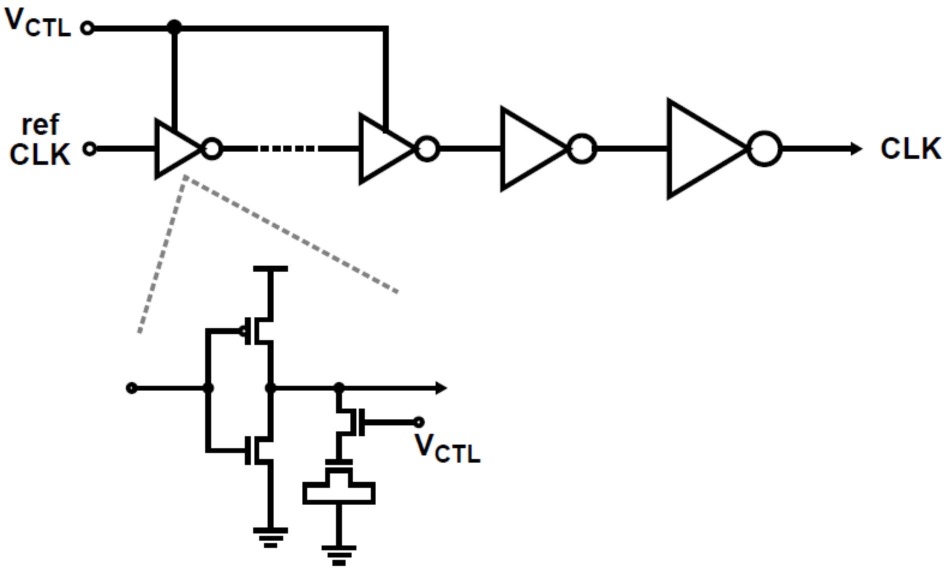
Delay-Locked Loop (DLL)

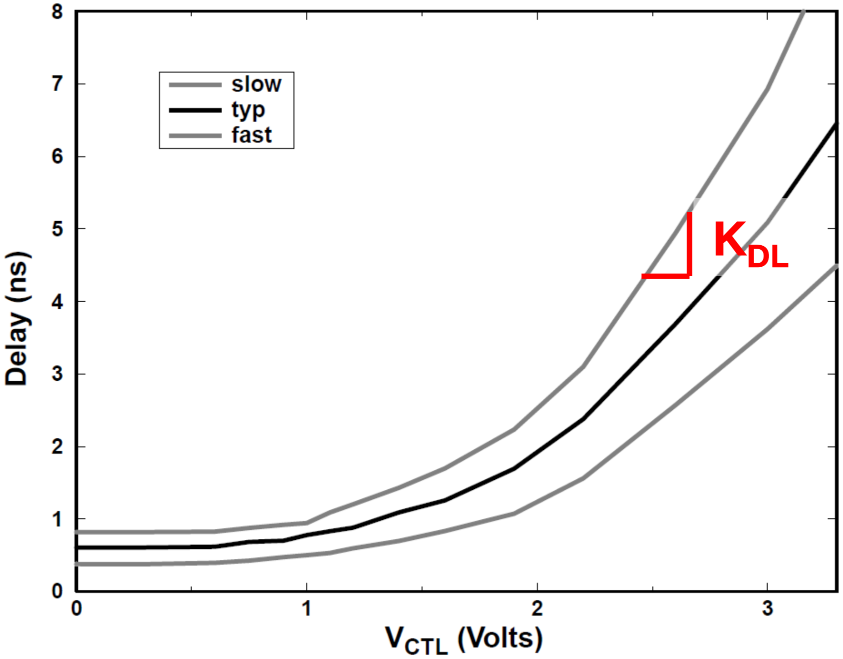


[Sidiropoulos JSSC 1997]

- DLLs lock delay of a voltage-controlled delay line (VCDL)
- Typically lock the delay to 1 or ½ input clock cycles
  - If locking to ½ clock cycle the DLL is sensitive to clock duty cycle
- DLL does not self-generate the output clock, only delays the input clock

Voltage-Controlled Delay Line

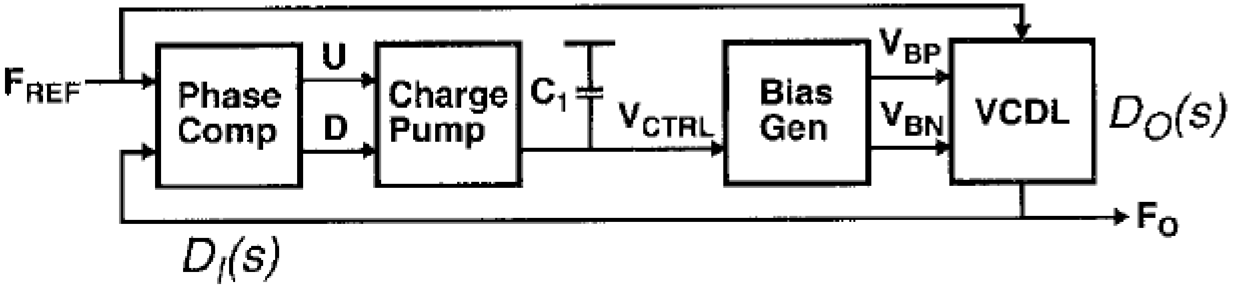




[Sidiropoulos]

Delay-Locked Loop (DLL)

[Maneatis JSSC 1996]



$$D_O(s) = (D_I(s) - D_O(s)) \cdot F_{\mathrm{REF}} \cdot \frac{I_{CH}}{sC_1} \cdot K_{DL}$$

$$\frac{D_O(s)}{D_I(s)} = \frac{1}{1 + s/\omega_N}$$

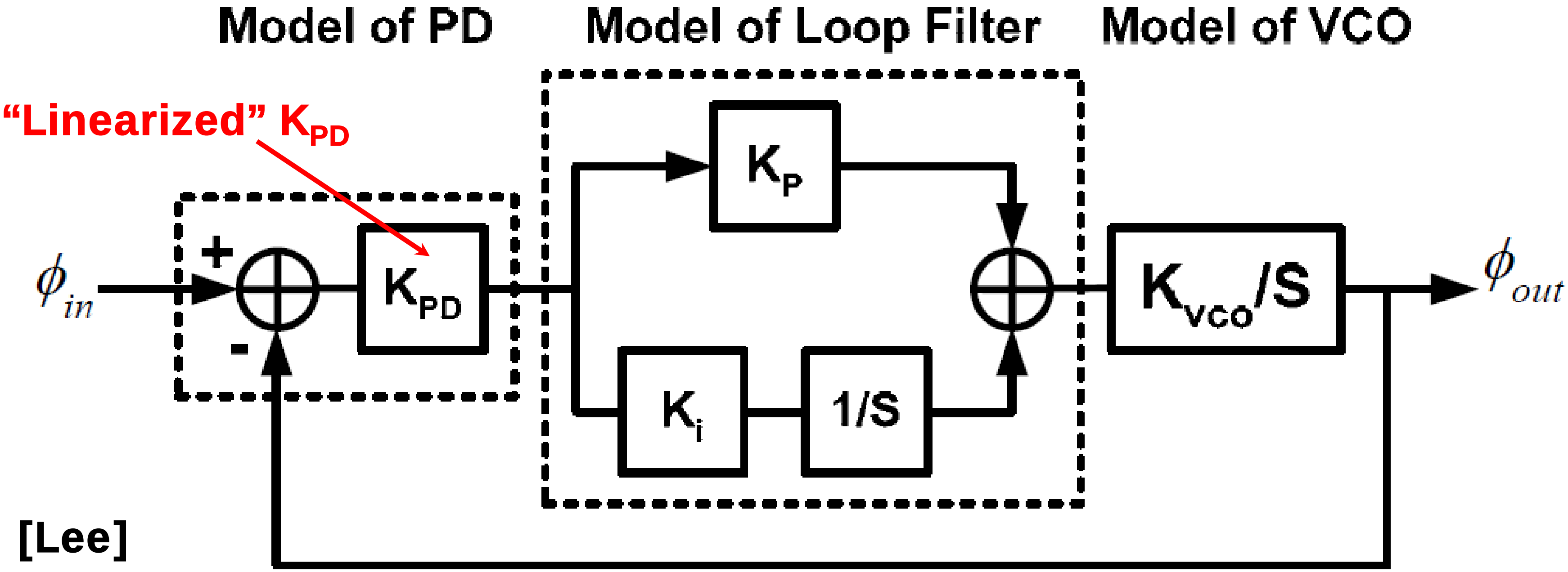
$$\omega_N = I_{CH} \cdot K_{DL} \cdot F_{\mathrm{REF}} \cdot \frac{1}{C_1}$$

- First-order loop as delay line doesn't introduce a pole
- VCDL doesn't accumulate jitter like a VCO
- DLL doesn't filter input jitter

CDR Jitter Properties

- Jitter Transfer
- Jitter Generation
- Jitter Tolerance

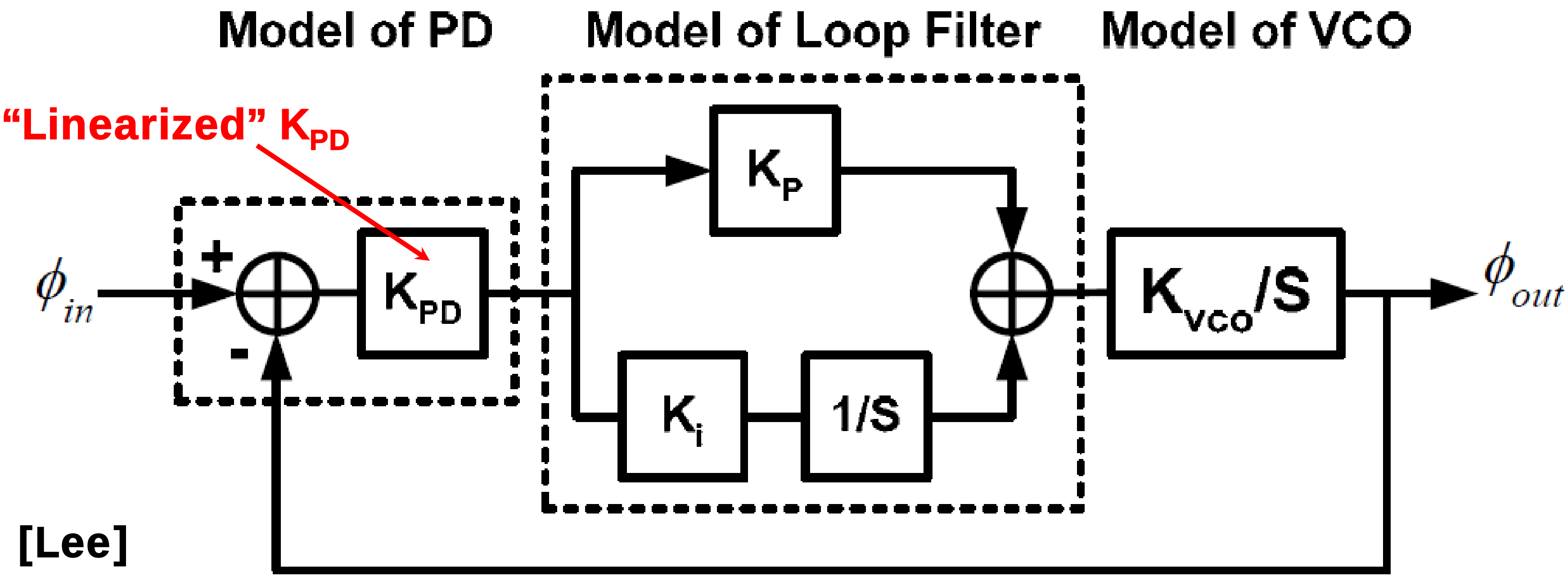
CDR Jitter Model



$$\frac{\phi_{out}}{\phi_{in}} = \frac{s \cdot K_P \cdot K_{PD} \cdot K_{VCO} + K_i \cdot K_{PD} \cdot K_{VCO}}{s^2 + s \cdot K_P \cdot K_{PD} \cdot K_{VCO} + K_i \cdot K_{PD} \cdot K_{VCO}}$$

$$K_P = I_C \cdot R \qquad K_i = \frac{I_C}{C} \qquad \omega_n = \sqrt{K_i \cdot K_{PD} \cdot K_{VCO}} \qquad \zeta = \frac{K_P}{K_i} \cdot \frac{\omega_n}{2}$$

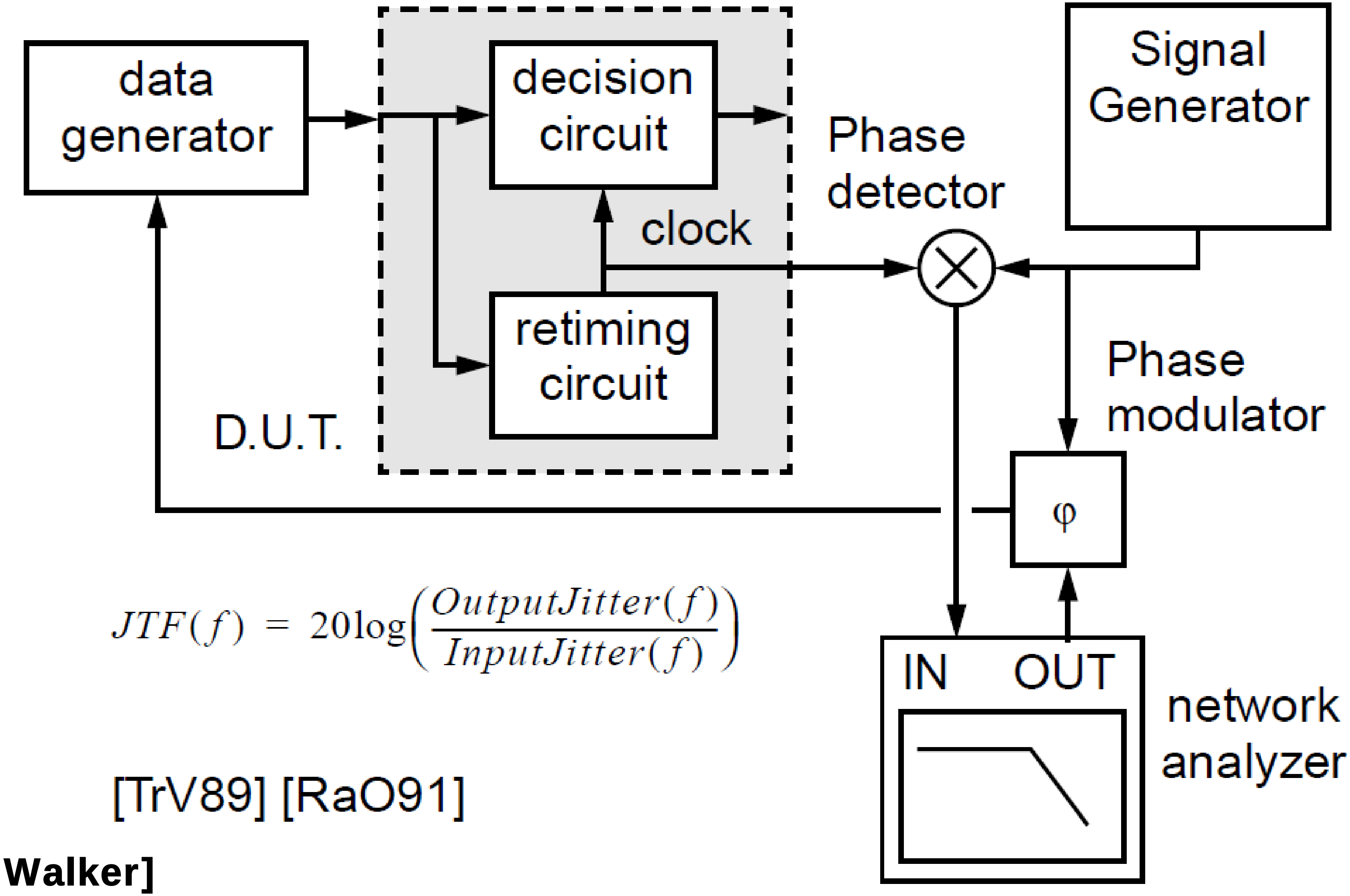
Jitter Transfer



- Jitter transfer is how much input jitter "transfers" to the output
  - If the PLL has any peaking in the phase transfer function, this jitter can actually be amplified

$$\frac{\phi_{out}}{\phi_{in}} = \frac{s \cdot K_P \cdot K_{PD} \cdot K_{VCO} + K_i \cdot K_{PD} \cdot K_{VCO}}{s^2 + s \cdot K_P \cdot K_{PD} \cdot K_{VCO} + K_i \cdot K_{PD} \cdot K_{VCO}}$$

Jitter Transfer Measurement

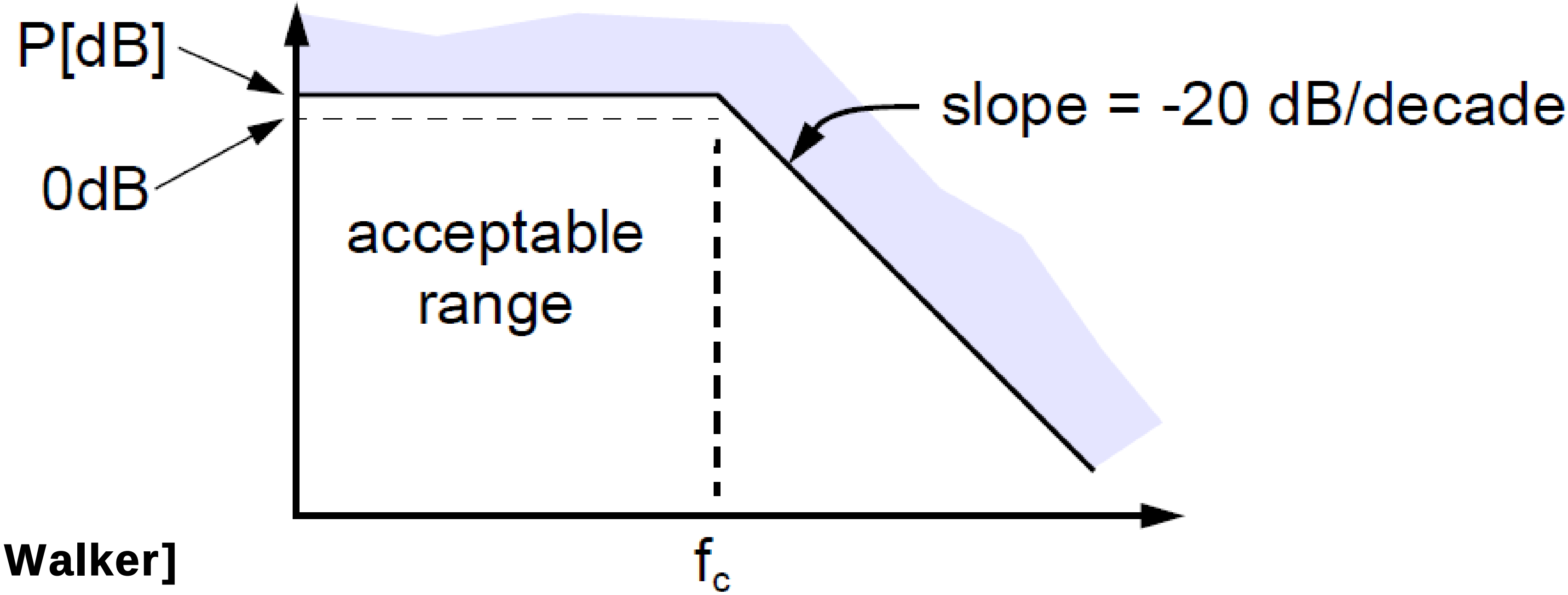


$$JTF(f) = 20\log\left(\frac{OutputJitter(f)}{InputJitter(f)}\right)$$

[TrV89] [RaO91]

[Walker]

Jitter Transfer Specification



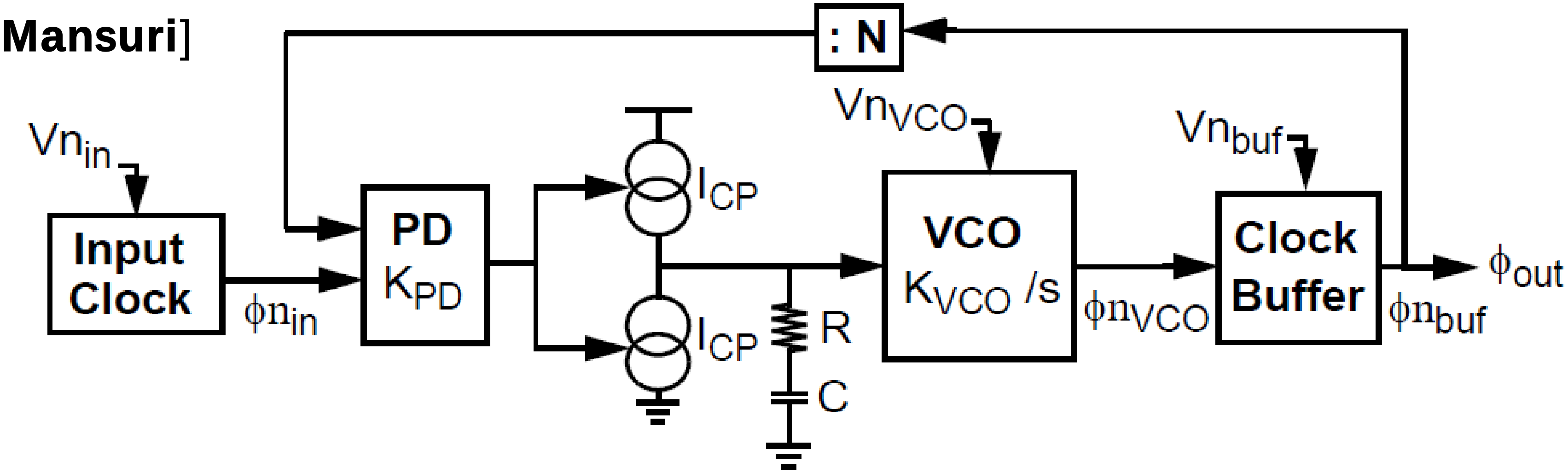
[Walker]

Data Rate	f_c[kHz]	P[dB]
155 Mb	130	0.1
622 Mb	500	0.1
2.488 Gb	2000	0.1

This specification is intended to control jitter peaking in long repeater chains

Jitter Generation

[**Mansuri**]



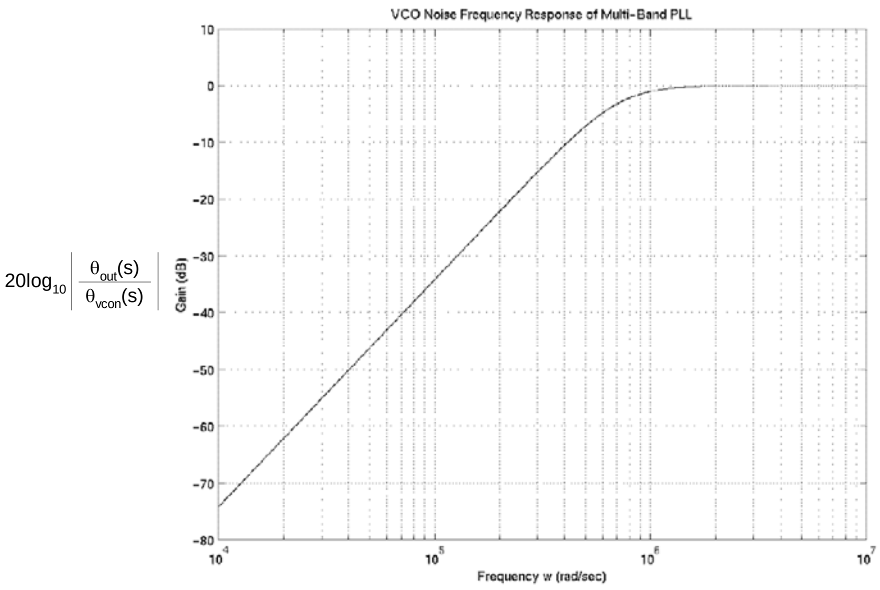
- Jitter generation is how much jitter the CDR “generates”
  - Assumed to be dominated by VCO
- Assumes jitter-free serial data input

VCO Phase Noise: $$H_{n_{VCO}}(s)=\frac{\phi_{out}}{\phi_{n_{VCO}}}=\frac{s^2}{s^2+\left(\frac{K_{Loop}}{N}\right)RCs+\frac{K_{Loop}}{N}}=\frac{s^2}{s^2+2\zeta\omega_n s+\omega_n^2}$$

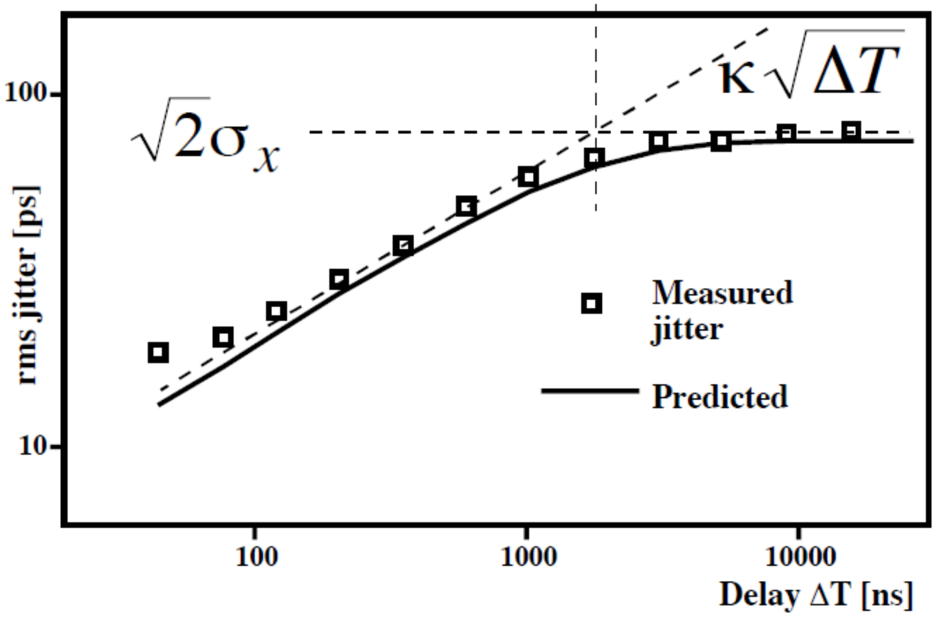
For CDR, N should be 1

Jitter Generation

High-Pass Transfer Function



Jitter accumulates up to time ∝ 1 / PLL bandwidth



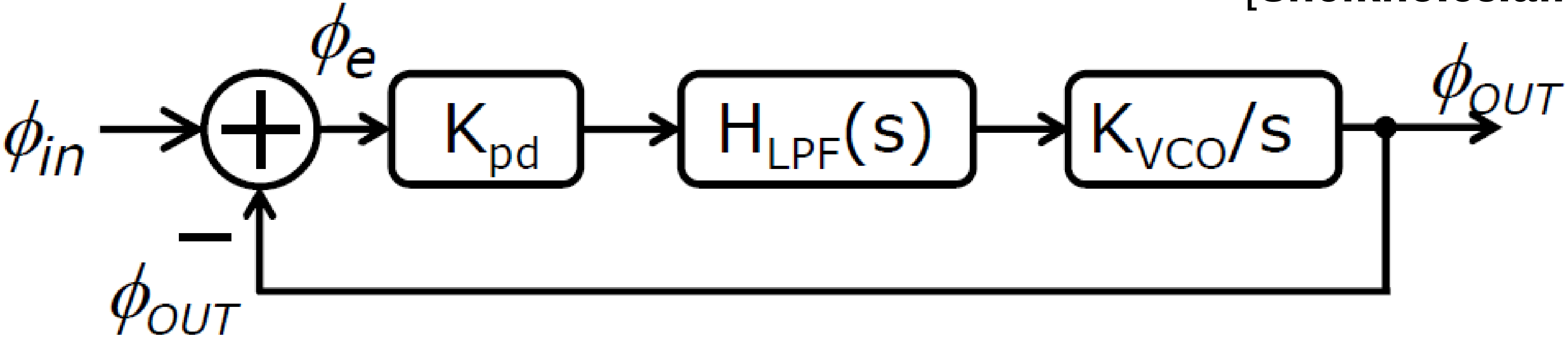
[McNeill]

- SONET specification:
  - rms output jitter ≤ 0.01 UI

Jitter Tolerance

- How much sinusoidal jitter can the CDR “tolerate” and still achieve a given BER?

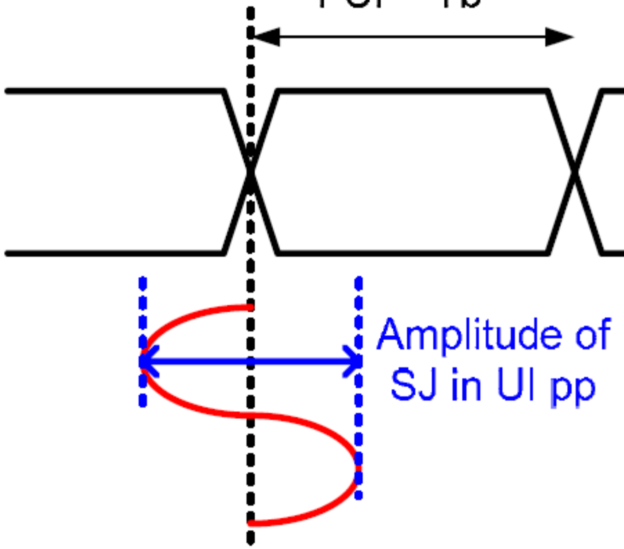
[**Sheikholeslami**]



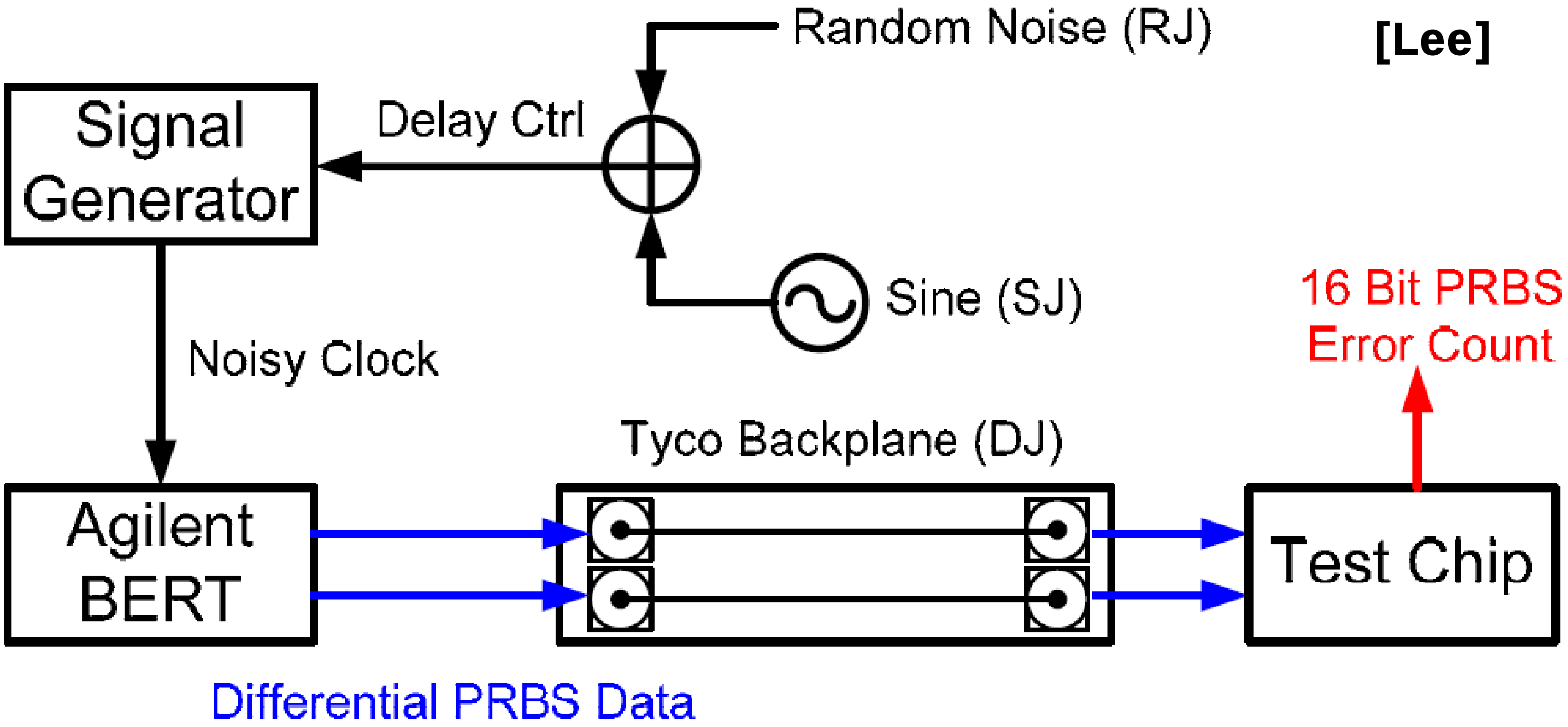
$$\phi_e = (1-\frac{\phi_{out}}{\phi_{in}})\cdot\phi_{n,in} = \frac{TM}{2}$$

$$JTOL(s) = 2\cdot\phi_{n,in} = \frac{TM}{(1-\frac{\phi_{out}}{\phi_{in}})}$$

[**Lee**]

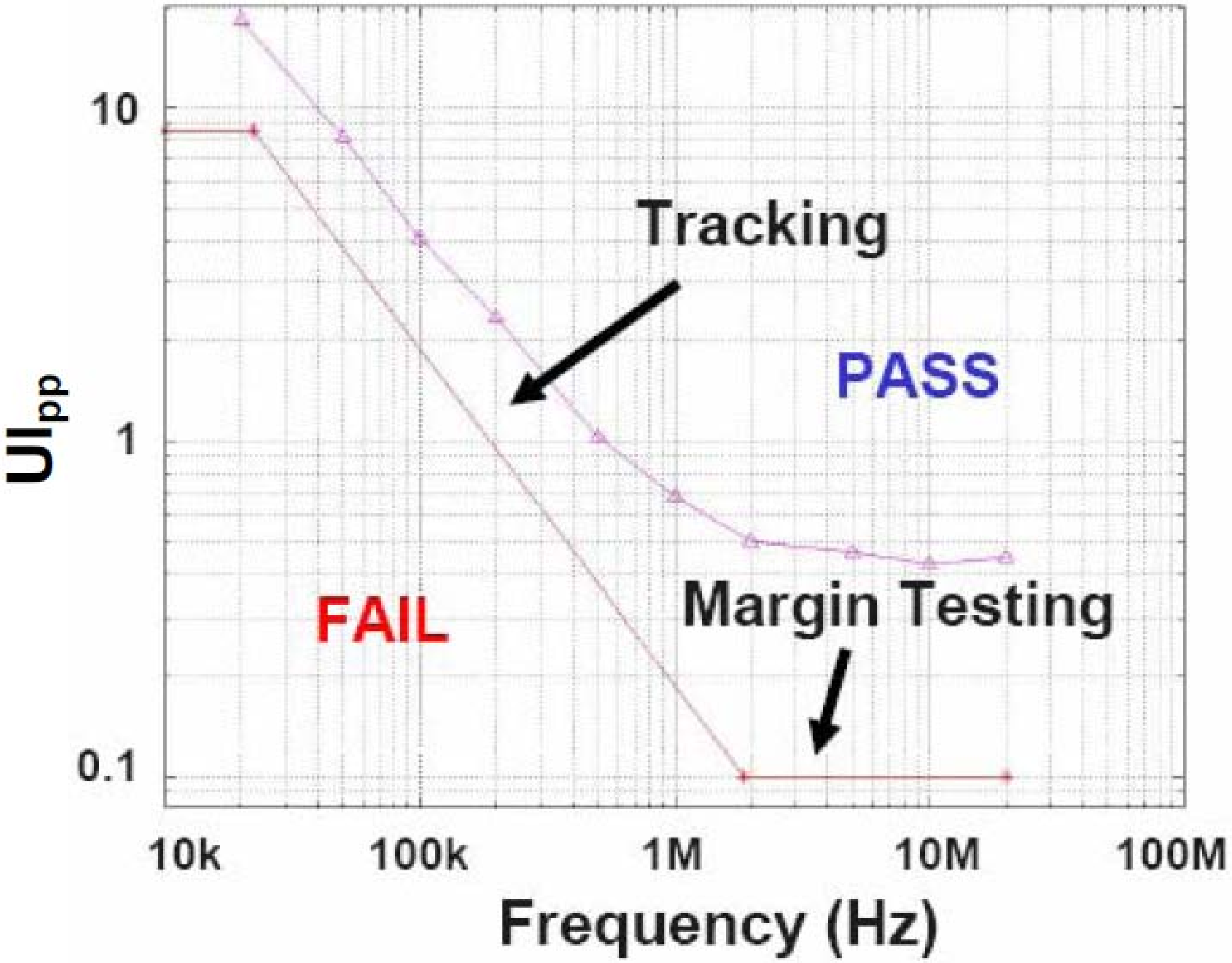


Jitter Tolerance Measurement



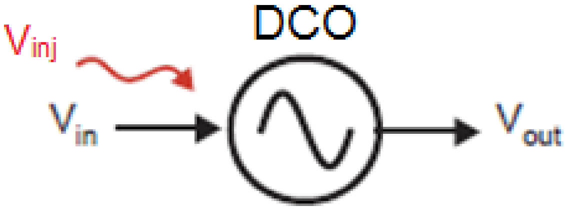
Jitter Tolerance Measurement

[Lee]



Injection Locking Oscillation

Jie Zou



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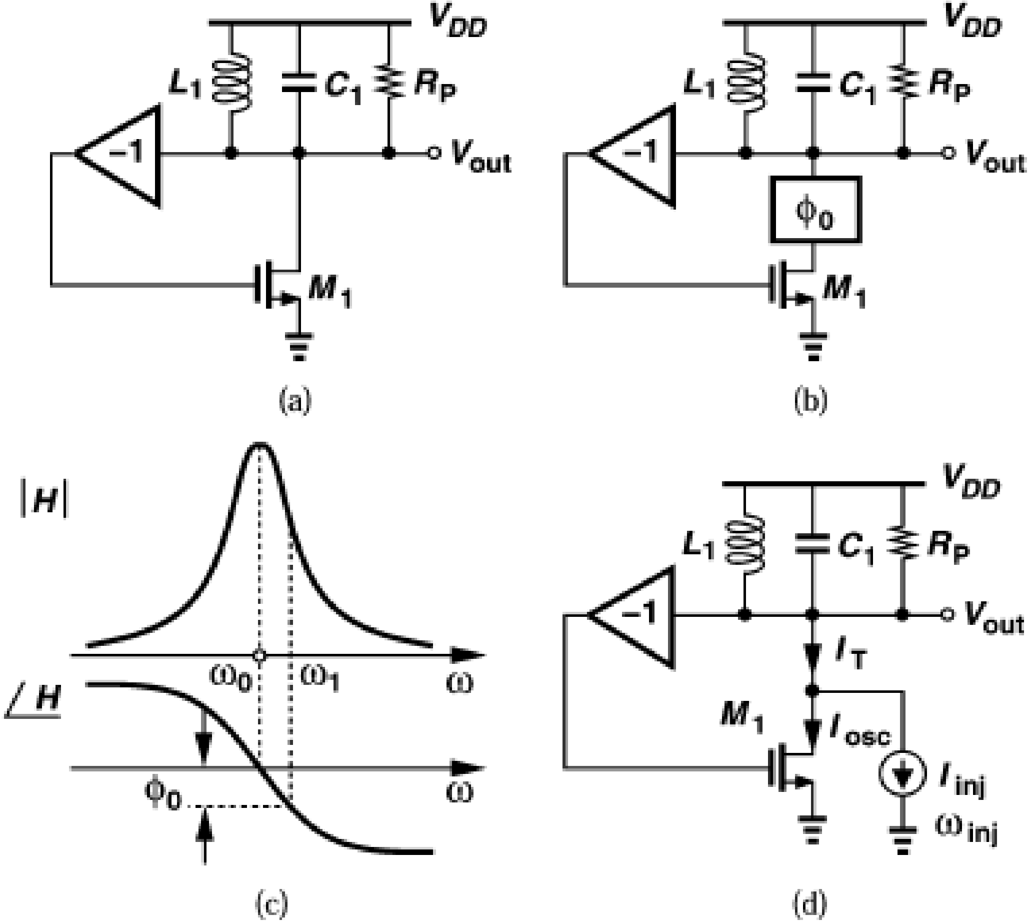
Injection Locking in LC Tanks

a) a free-running oscillator consisting of an ideal positive feedback amplifier and an LC tank;

b) we insert a phase shift in the loop. We know this will cause the oscillation frequency to shift since the loop gain has to
have exactly 2π phase shift (or multiples).

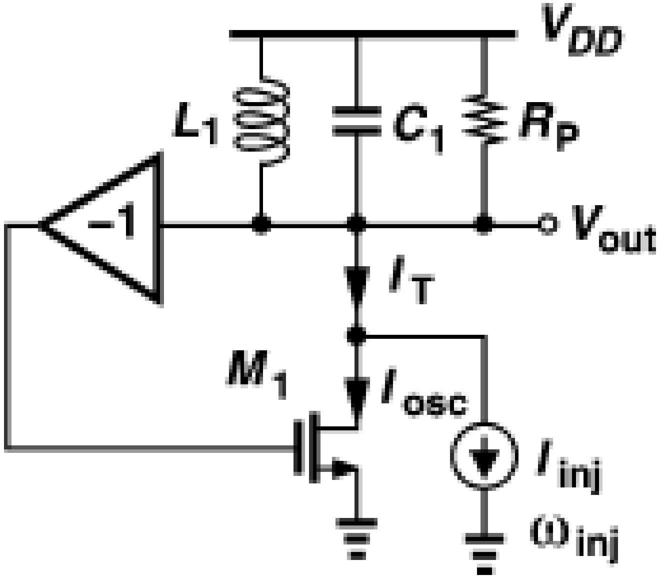


Phase Shift for Injected Signal

- Assume the oscillator “locks” onto the injected current and oscillates at the same frequency.

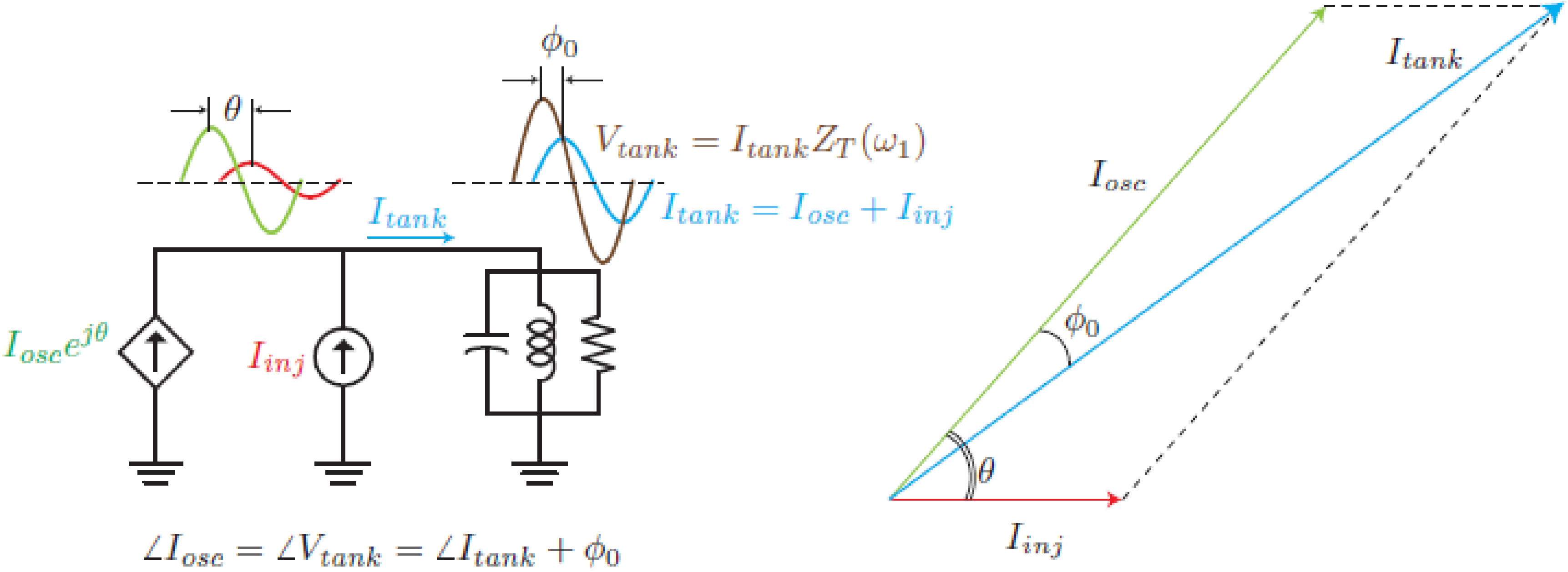
- Since the locking signal is not in general at the resonant center frequency, the tank introduces a phase shift

- In order for the oscillator loop gain to be equal to unity with zero phase shift, the sum of the current of the transistor and the injected currents must have the proper phase shift to compensate for the tank phase shift.



Source: [Razavi]

Injection Locked Oscillator Phasors


θ
ϕ_0
$V_{tank} = I_{tank} Z_T(\omega_1)$
I_{tank}
$I_{tank} = I_{osc} + I_{inj}$
$I_{osc}e^{j\theta}$
I_{inj}
$\angle I_{osc} = \angle V_{tank} = \angle I_{tank} + \phi_0$
I_{tank}
I_{osc}
ϕ_0
θ
I_{inj}

Note that the frequency of the injection signal determines the extra phase shift Φ_0 of the tank. This is fixed by the frequency offset.

❑ The current from the transistor is fed by the tank voltage, which by definition the tank current times the tank impedance, which introduces Φ_0 between the tank current/voltage.
❑ The angle between the injected current and the oscillator current θ must be such that their sum aligns with the tank current.

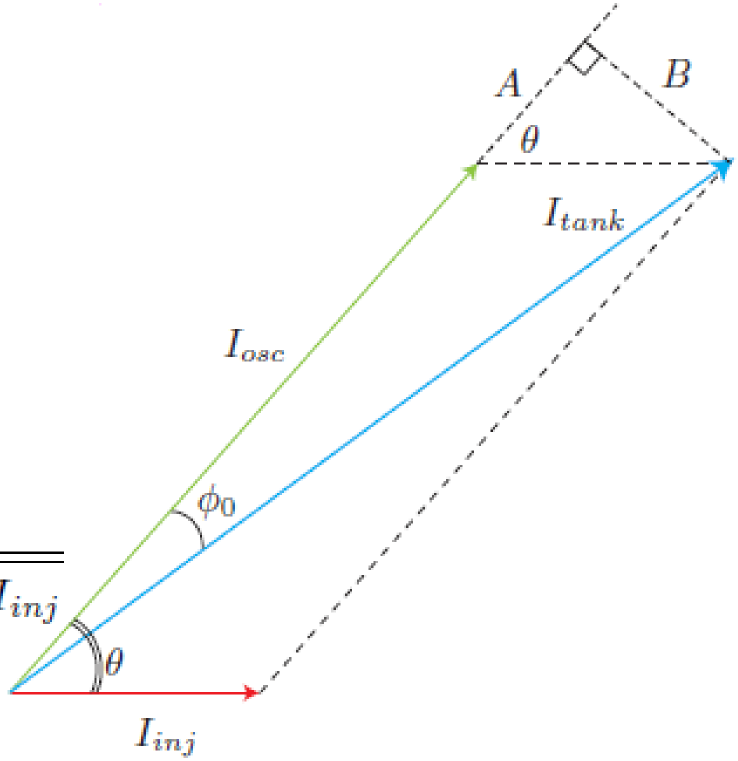
Injection Geometry

$$\sin\phi_0 = \frac{B}{I_{tank}}$$

$$\cos(\pi/2 - \theta) = \sin(\theta) = \frac{B}{I_{inj}}$$

$$\sin\phi_0 = \frac{I_{inj}}{I_{tank}}\sin(\theta)$$

$$\sin\phi_0 = \frac{I_{inj}\sin(\theta)}{|I_{osc}e^{j\theta} + I_{inj}|} = \frac{I_{inj}\sin(\theta)}{\sqrt{I_{osc}^2 + I_{inj}^2 + 2\cos\theta I_{osc}I_{inj}}}$$



The geometry of the problem implies the following constraints on the injected current amplitude relative to the oscillation amplitude.

Locking Range

$$\sin\phi_0 = \frac{I_{inj}}{I_T}\sin\theta = \frac{I_{inj}\sin\theta}{\sqrt{I_{osc}^2 + I_{inj}^2 + 2I_{osc}I_{inj}\cos\theta}}$$

$$\Rightarrow \sin\phi_{0,\max} = \frac{I_{inj}}{I_{iosc}}, if.\cos\theta = -\frac{I_{inj}}{I_{iosc}}$$

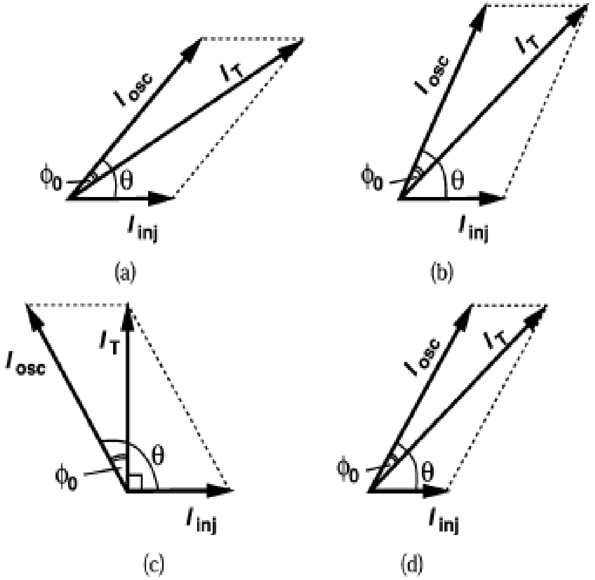
A second-order parallel tank consisting of L. C, Rp exhibits a phase shift of:

$$\phi_0 = \frac{\pi}{2} - \tan^{-1}\left(\frac{L\cdot\omega}{R_p}\cdot\frac{\omega_0^2}{\omega_0^2-\omega^2}\right)$$

$$\because \omega_0^2 - \omega^2 \approx 2\omega_0(\omega_0-\omega), \frac{L\cdot\omega}{R_p} = \frac{1}{Q}, \frac{\pi}{2} - \tan^{-1}(x) = \tan^{-1}(x^{-1})$$

$$\therefore \tan\phi_0 \approx \frac{2Q}{\omega_0}(\omega_0-\omega)$$

$$\because \tan\phi_0 = \frac{I_{inj}}{I_T}, I_T = \sqrt{I_{osc}^2 - I_{inj}^2}$$



Source: Razavi

At the edge of the lock range, the injected current is orthogonal to the tank current.

The phase angle between the injected current and the oscillator is 90° + $\Phi_{0,\max}$

Locking Range

$$\Rightarrow \frac{I_{inj}}{I_T} \approx \frac{2Q}{\omega_0}(\omega_0 - \omega)$$

$$\frac{I_{inj}}{I_{osc}} \cdot \frac{I_{osc}}{I_T} = \frac{I_{inj}}{I_{osc}} \cdot \frac{1}{\sqrt{1 - \frac{I_{inj}^2}{I_{osc}^2}}}$$

$$\Rightarrow \frac{I_{inj}}{I_{osc}} \cdot \frac{1}{\sqrt{1 - \frac{I_{inj}^2}{I_{osc}^2}}} \approx \frac{2Q}{\omega_0}(\omega_0 - \omega)$$

$$\Rightarrow \omega_0 - \omega_{inj} \approx \frac{\omega_0}{2Q} \cdot \frac{I_{inj}}{I_{osc}} \cdot \frac{1}{\sqrt{1 - \frac{I_{inj}^2}{I_{osc}^2}}}$$

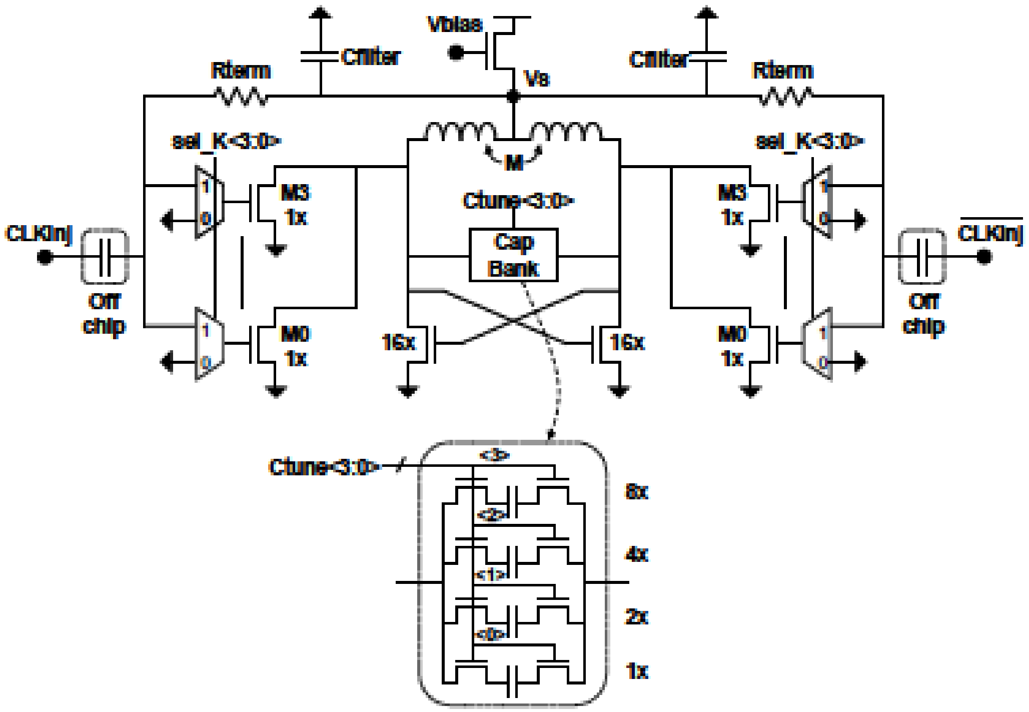
$$I_{inj} << I_{osc}$$

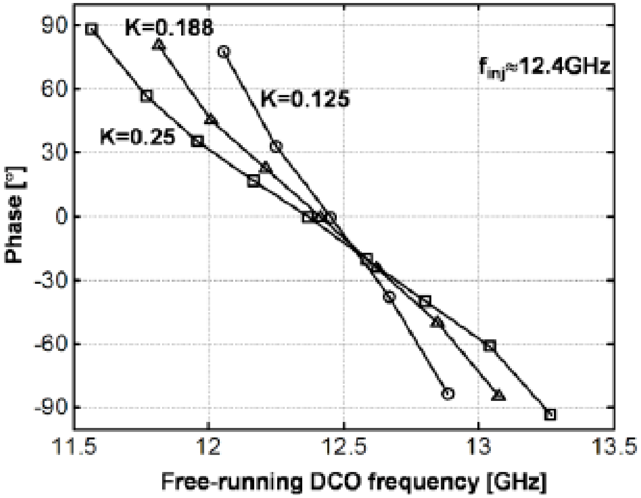
$$\omega_{\Delta,L} = \omega_0 - \omega_{inj} \approx \frac{\omega_0}{2Q} \cdot \frac{I_{inj}}{I_{osc}}$$

$$When: \omega_0 = 10GHz, Q = 5, K = \frac{I_{inj}}{I_{osc}} = 0.1$$

$$=> \omega_{\Delta,L} \approx 100MHz$$

Digital Controlled Oscillator (DCO) with Injection Locking





Shekhar, Sudip et al, “Strong Injection Locking in Low-Q LC Oscillators: Modeling and Application in a Forwarded-Clocked I/O Receiver”, IEEE JSSC, 2009.

The digitally controlled switch-capacitor bank tunes the free-running frequency of DCO to adjust the phase of the forwarded clock and also compensate for PVT.

Next Time

- Optical I/O