ECEN689: Special Topics in High-Speed Links Circuits and Systems Spring 2010

Lecture 27: PLL Circuits

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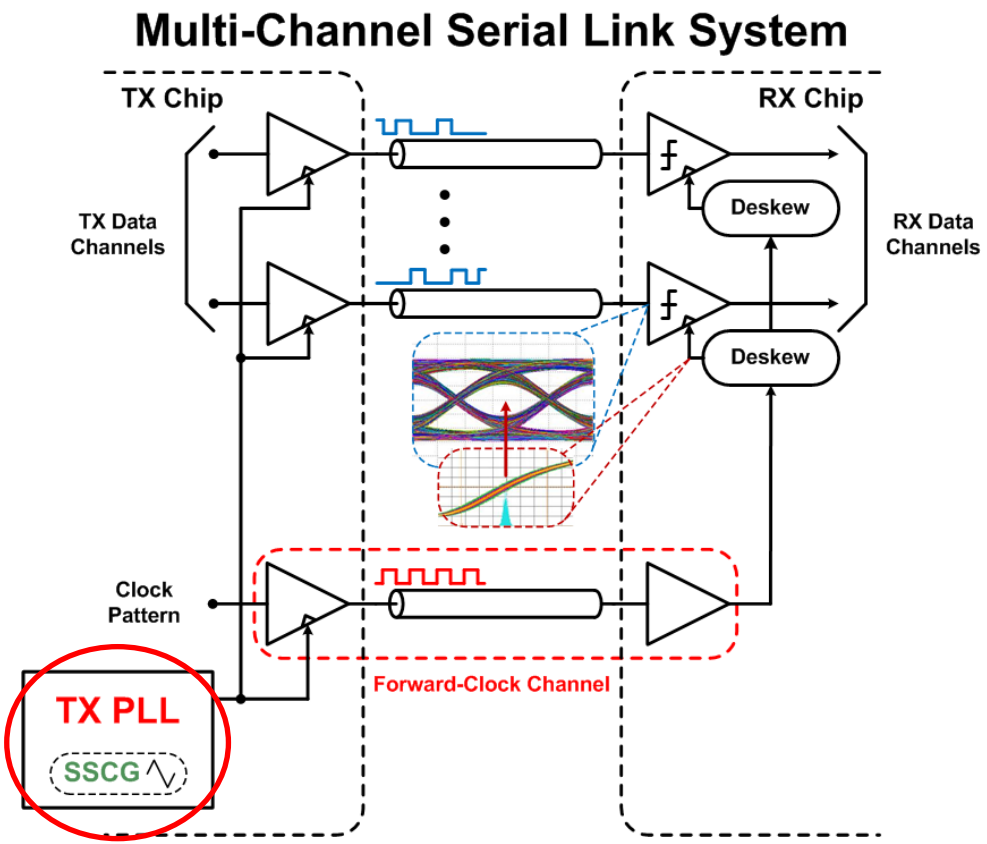
Announcements

- Project Preliminary Report #1 due now
- Exam 2 is still April 30
- Reading
  - Posted clocking papers
  - Website additional links has PLL and jitter tutorials
- Majority of today's material from Fischette tutorial and M. Mansuri's PhD thesis (UCLA)

Agenda

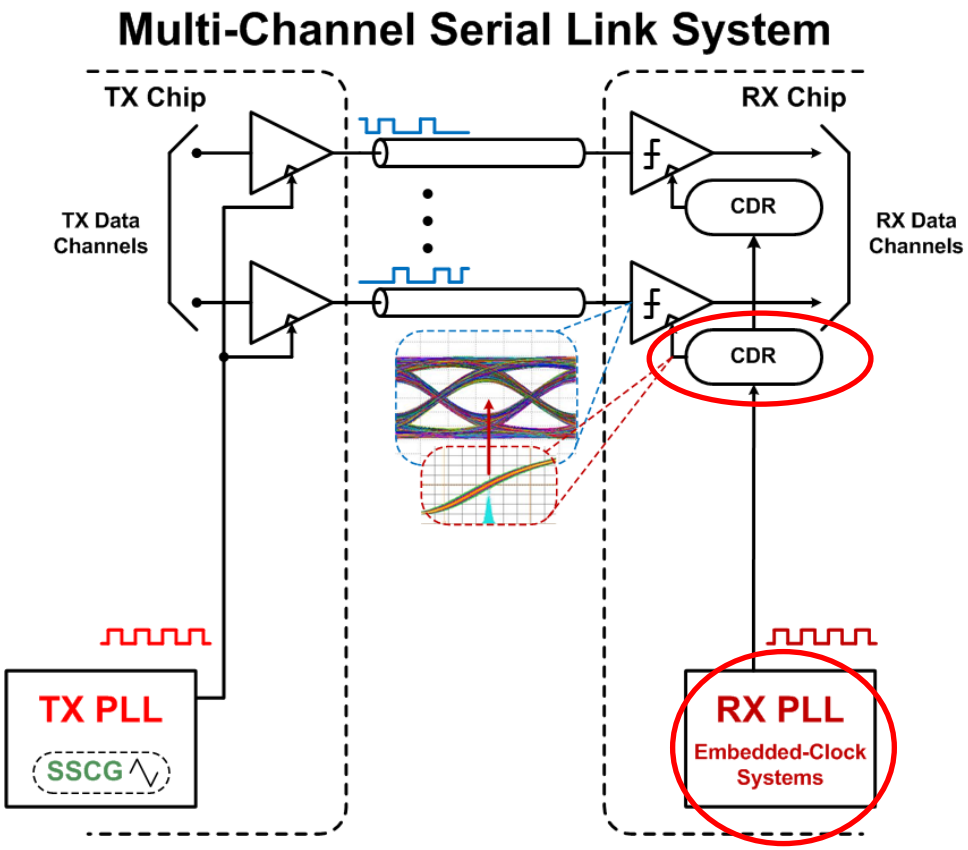
- PLL noise transfer functions
- PLL circuits

Forward Clock I/O Circuits



- TX PLL
- TX Clock Distribution
- Replica TX Clock Driver
- Channel
- Forward Clock Amplifier
- RX Clock Distribution
- De-Skew Circuit
  - DLL/PI
  - Injection-Locked Oscillator

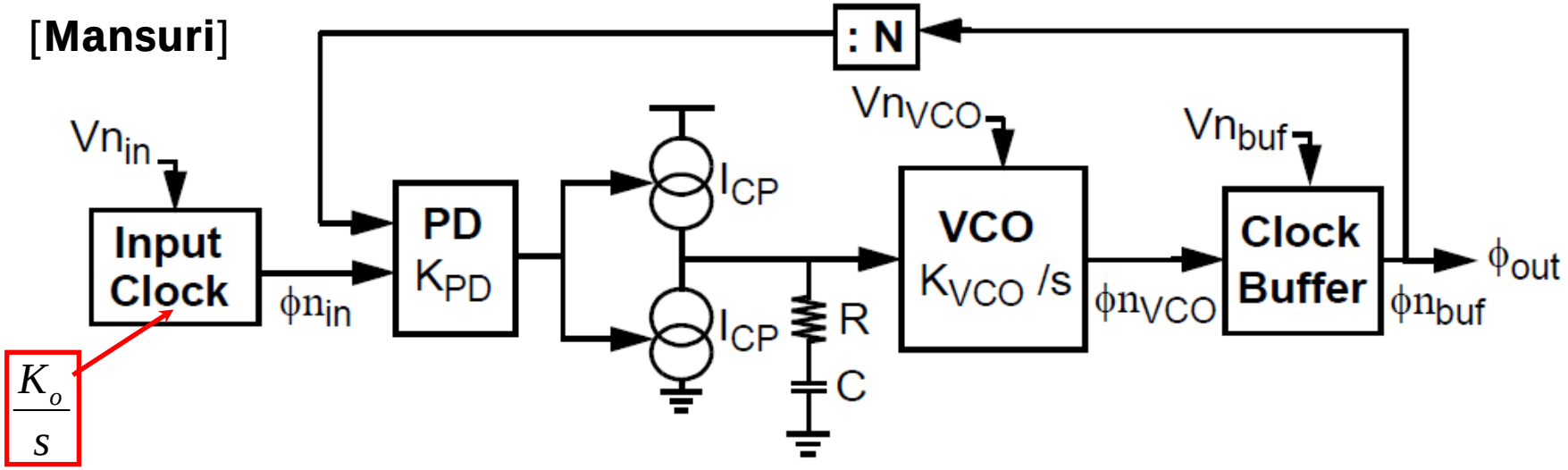
Embedded Clock I/O Circuits



- TX PLL
- TX Clock Distribution
- CDR
  - Per-channel PLL-based
  - Dual-loop w/ Global PLL &
    - Local DLL/PI
    - Local Phase-Rotator PLLs
    - Global PLL requires RX clock distribution to individual channels

Input Noise Transfer Function

[**Mansuri**]



Input Phase Noise:

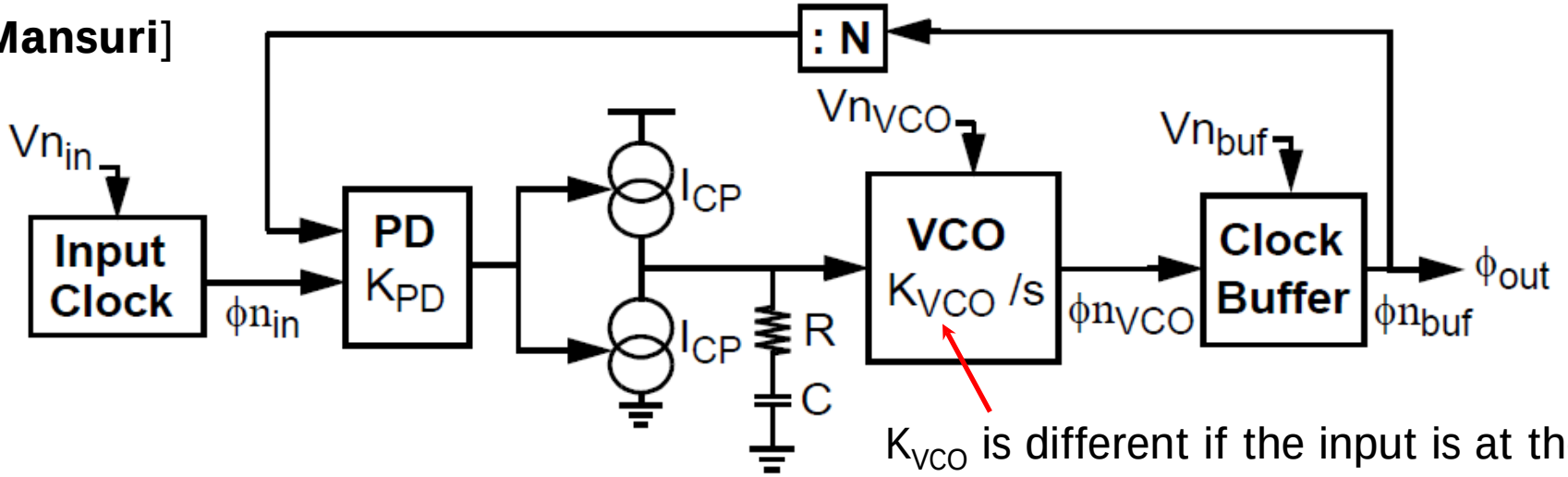
$$H_{n_{IN}}(s)=\frac{\phi_{out}}{\phi_{n_{IN}}}=\frac{K_{Loop}(RCs+1)}{s^2+\left(\frac{K_{Loop}}{N}\right)RCs+\frac{K_{Loop}}{N}}=\frac{N\left(2\zeta\omega_n s+\omega_n^2\right)}{s^2+2\zeta\omega_n s+\omega_n^2}$$

Voltage Noise on Input Clock Source:

$$T_{n_{IN}}(s)=\frac{\phi_{out}}{v_{n_{IN}}}=\left(\frac{\phi_{out}}{\phi_{n_{IN}}}\right)\left(\frac{K_o}{s}\right)=\frac{K_oK_{Loop}(RCs+1)}{s\left(s^2+\left(\frac{K_{Loop}}{N}\right)RCs+\frac{K_{Loop}}{N}\right)}$$

VCO Noise Transfer Function

[**Mansuri**]



K_{VCO} is different if the input is at the V_{cntrl} input (K_{VCO}) or supply (K_{Vdd})

VCO Phase Noise:

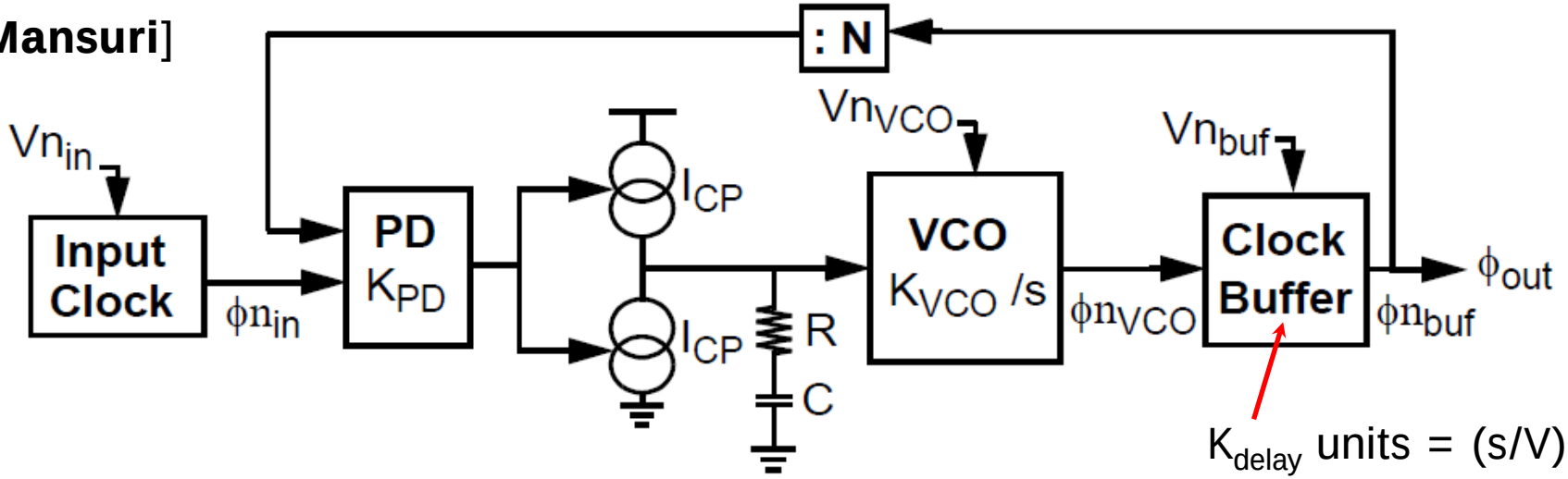
$$H_{n_{VCO}}(s)=\frac{\phi_{out}}{\phi_{n_{VCO}}}=\frac{s^2}{s^2+\left(\frac{K_{Loop}}{N}\right)RCs+\frac{K_{Loop}}{N}}=\frac{s^2}{s^2+2\zeta\omega_n s+\omega_n^2}$$

Voltage Noise on VCO Inputs:

$$T_{n_{VCO}}(s)=\frac{\phi_{out}}{v_{n_{VCO}}}=\left(\frac{\phi_{out}}{\phi_{n_{VCO}}}\right)\left(\frac{K_{VCO}}{s}\right)=\frac{K_{VCO}s}{s^2+\left(\frac{K_{Loop}}{N}\right)RCs+\frac{K_{Loop}}{N}}$$

Clock Buffer Noise Transfer Function

[**Mansuri**]

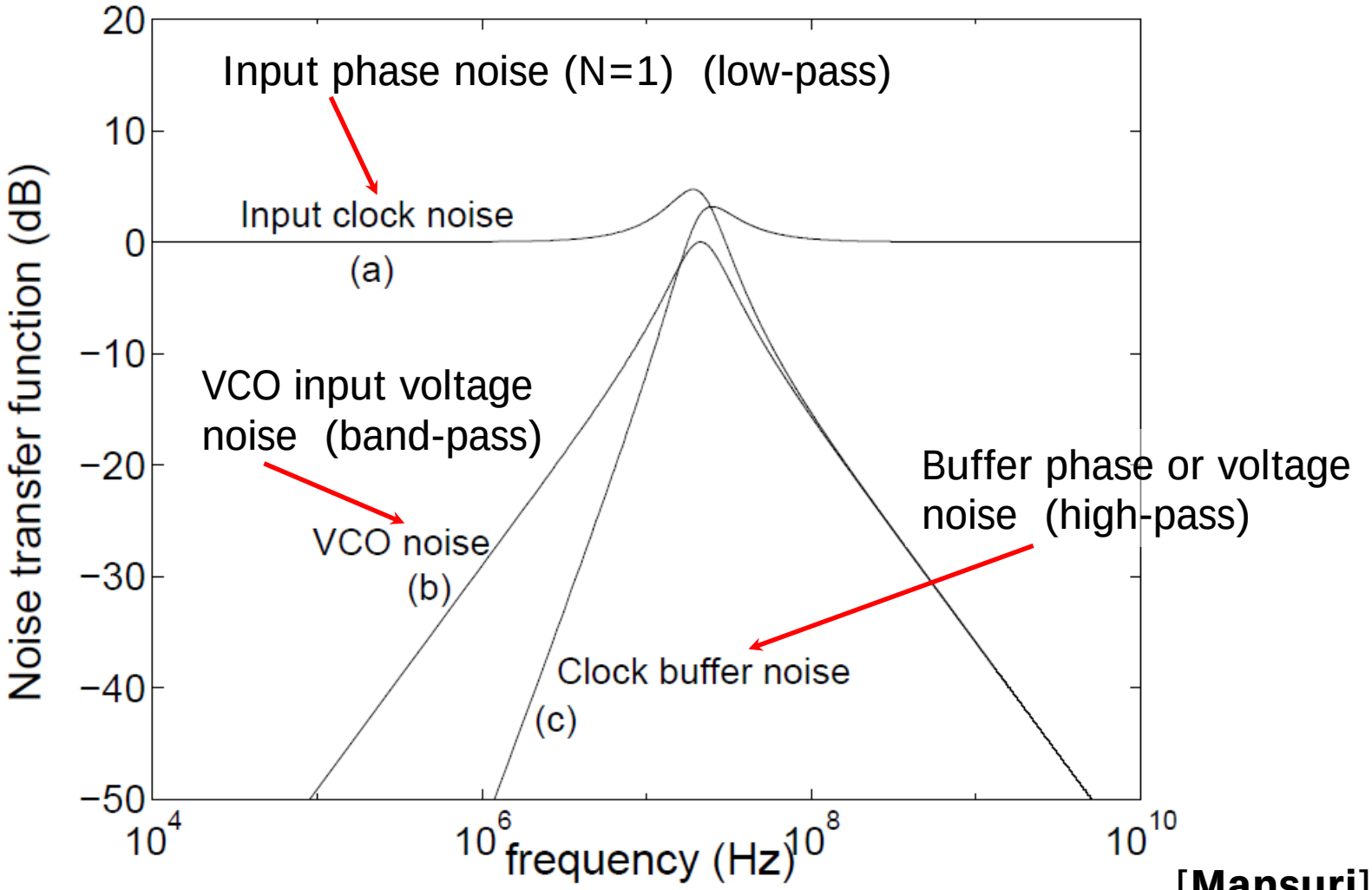


Output Phase Noise: $$H_{n_{buf}}(s)=\frac{\phi_{out}}{\phi_{n_{buf}}}=\frac{s^2}{s^2+\left(\frac{K_{Loop}}{N}\right)RCs+\frac{K_{Loop}}{N}}=\frac{s^2}{s^2+2\zeta\omega_n s+\omega_n^2}$$

Voltage Noise on Buffer Inputs:

$$T_{n_{buf}}(s)=\frac{\phi_{out}}{v_{n_{buf}}}=\left(\frac{\phi_{out}}{\phi_{n_{buf}}}\right)\left(\frac{K_{delay}\omega_{VCO}}{\frac{s}{\omega_{buf}}+1}\right)=\left(\frac{K_{delay}\omega_{VCO}}{\frac{s}{\omega_{buf}}+1}\right)\frac{s^2}{s^2+\left(\frac{K_{Loop}}{N}\right)RCs+\frac{K_{Loop}}{N}}\approx\frac{K_{delay}\omega_{VCO}s^2}{s^2+\left(\frac{K_{Loop}}{N}\right)RCs+\frac{K_{Loop}}{N}}$$

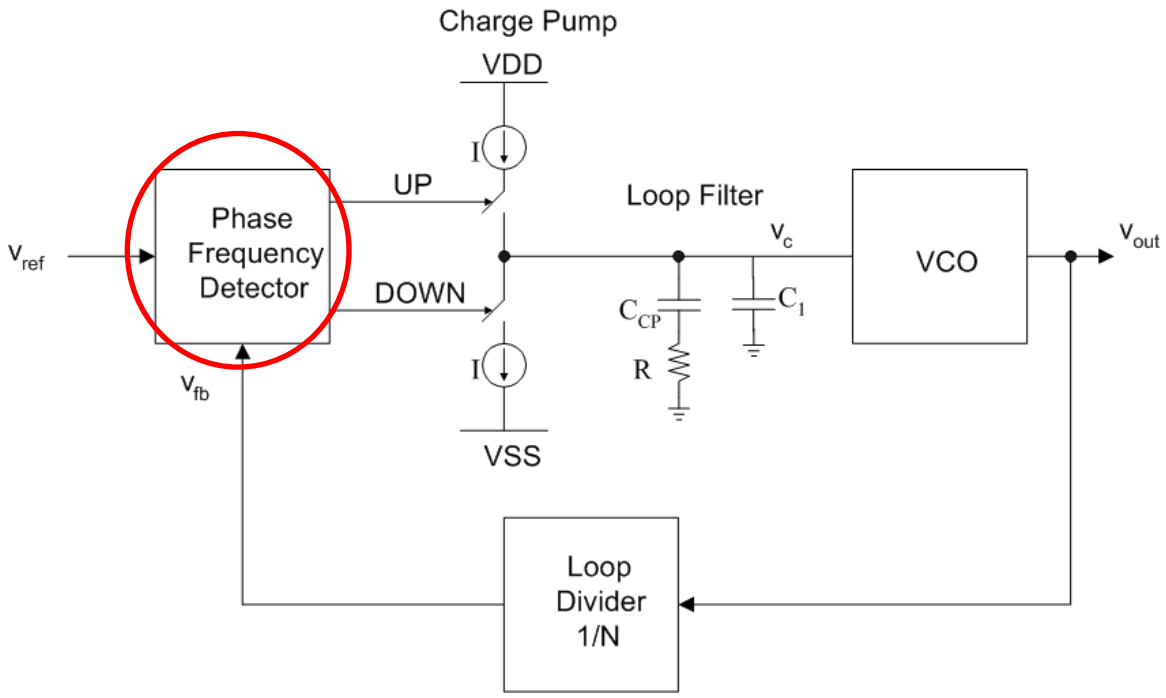
Noise Transfer Functions



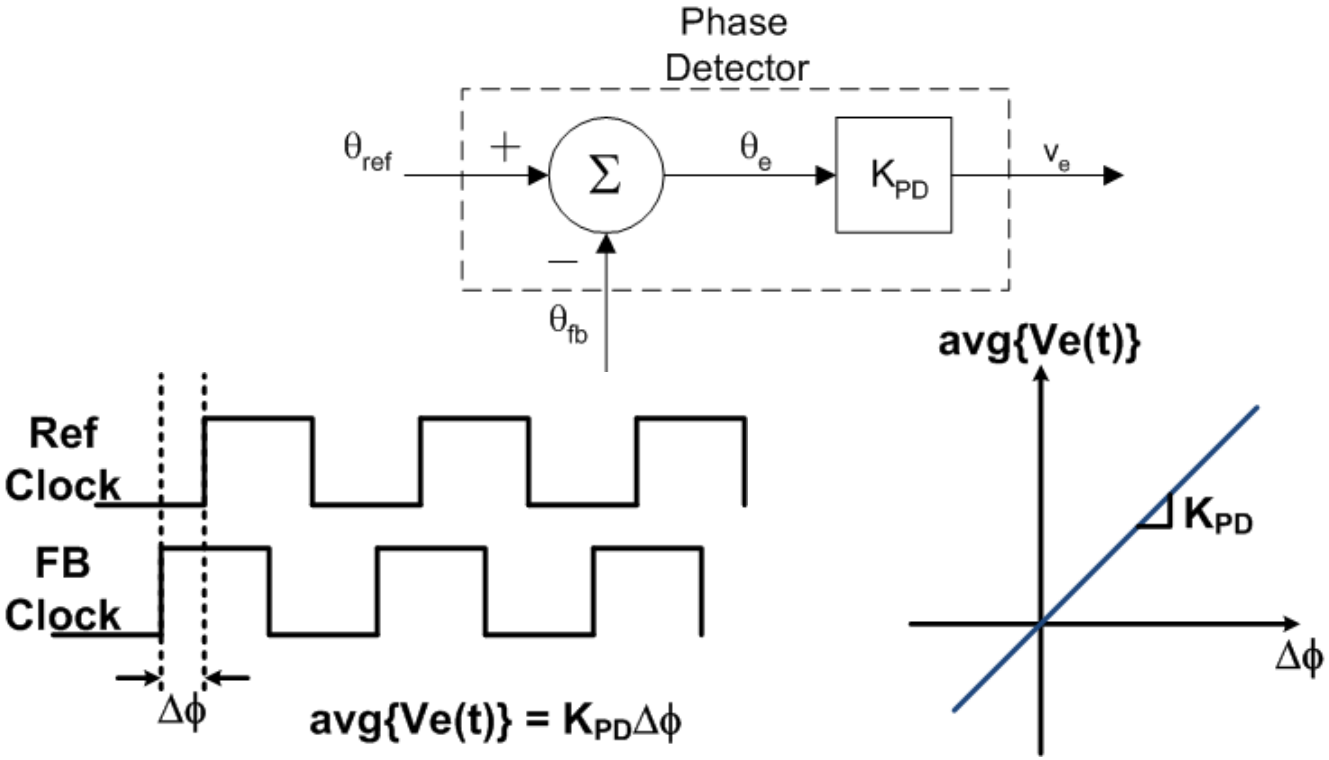
[**Mansuri**]

Charge-Pump PLL Circuits

- Phase Detector
- Charge-Pump
- Loop Filter
- VCO
- Divider

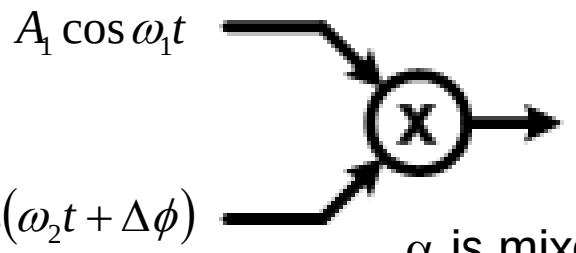


Phase Detector



- Detects phase difference between feedback clock and reference clock
- The loop filter will filter the phase detector output, thus to characterize phase detector gain, extract average output voltage (or current for charge-pump PLLs)
- Can be analog or digital

Analog Multiplier Phase Detector



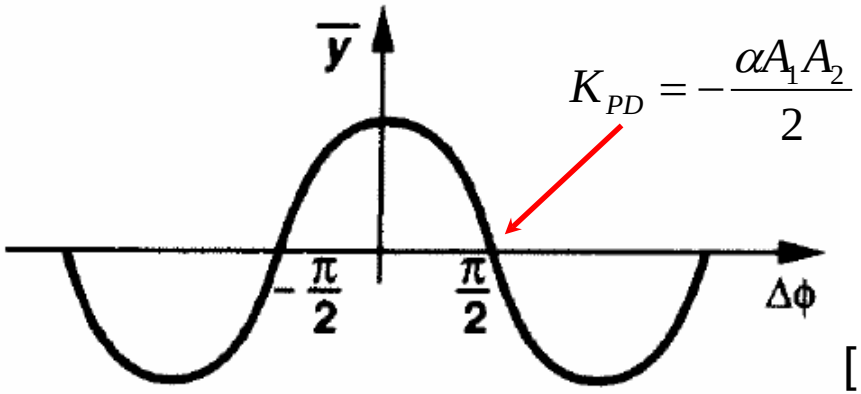
$$\frac{\alpha A_1 A_2}{2}\cos[(\omega_1+\omega_2)t+\Delta\phi]+\frac{\alpha A_1 A_2}{2}\cos[(\omega_1-\omega_2)t-\Delta\phi]$$

α is mixer gain

- If $\omega_1 = \omega_2$ and filtering out high-frequency term

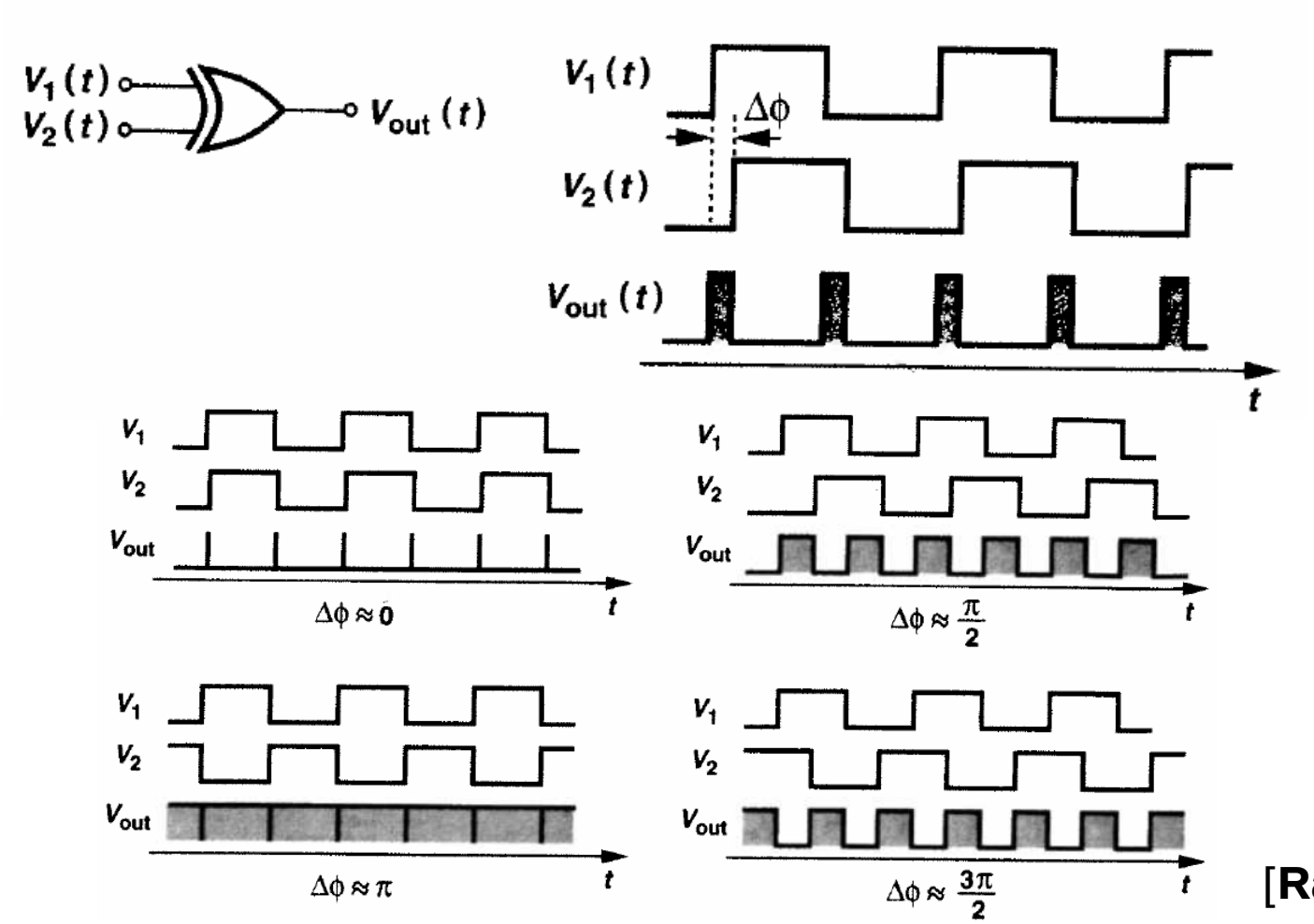
$$\overline{y(t)} = \frac{\alpha A_1 A_2}{2}\cos\Delta\phi$$

- Near $\Delta\phi$ lock region of $\pi/2$: $\overline{y(t)} \approx \frac{\alpha A_1 A_2}{2}\left(\frac{\pi}{2}-\Delta\phi\right)$



[**Razavi**]

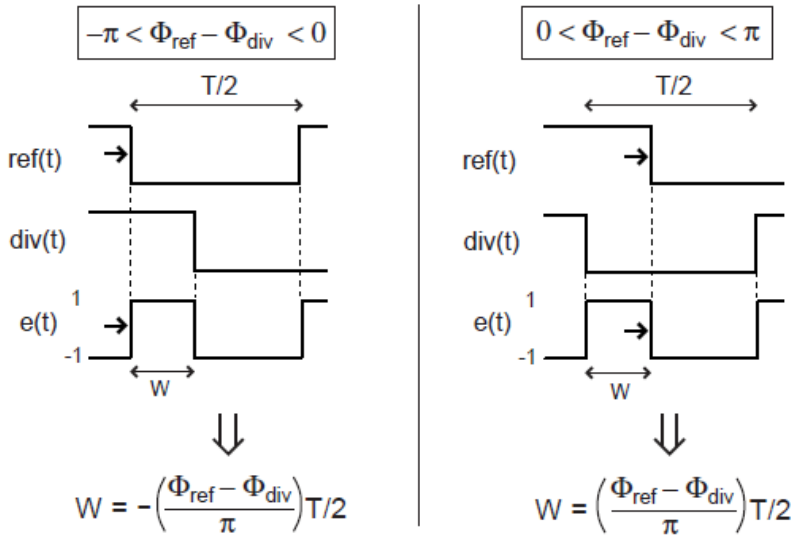
XOR Phase Detector



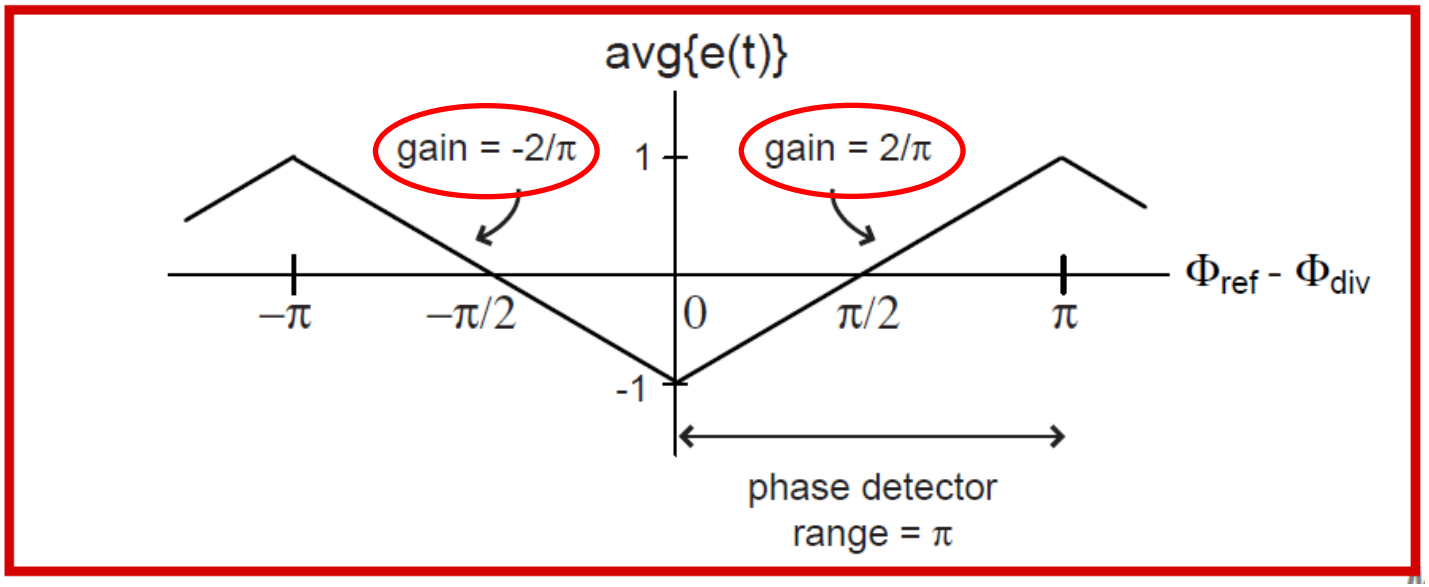
[**Razavi**]

- Sensitive to clock duty cycle

XOR Phase Detector

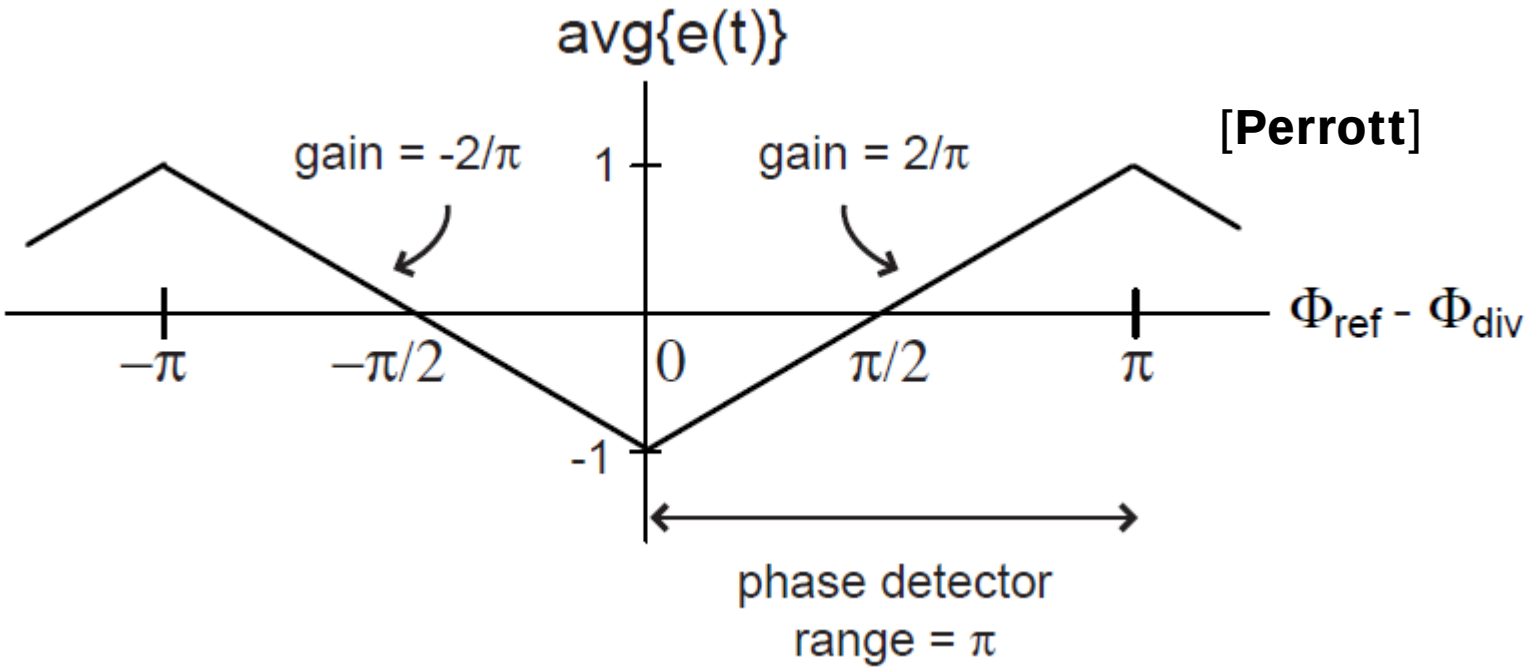


[Perrott]

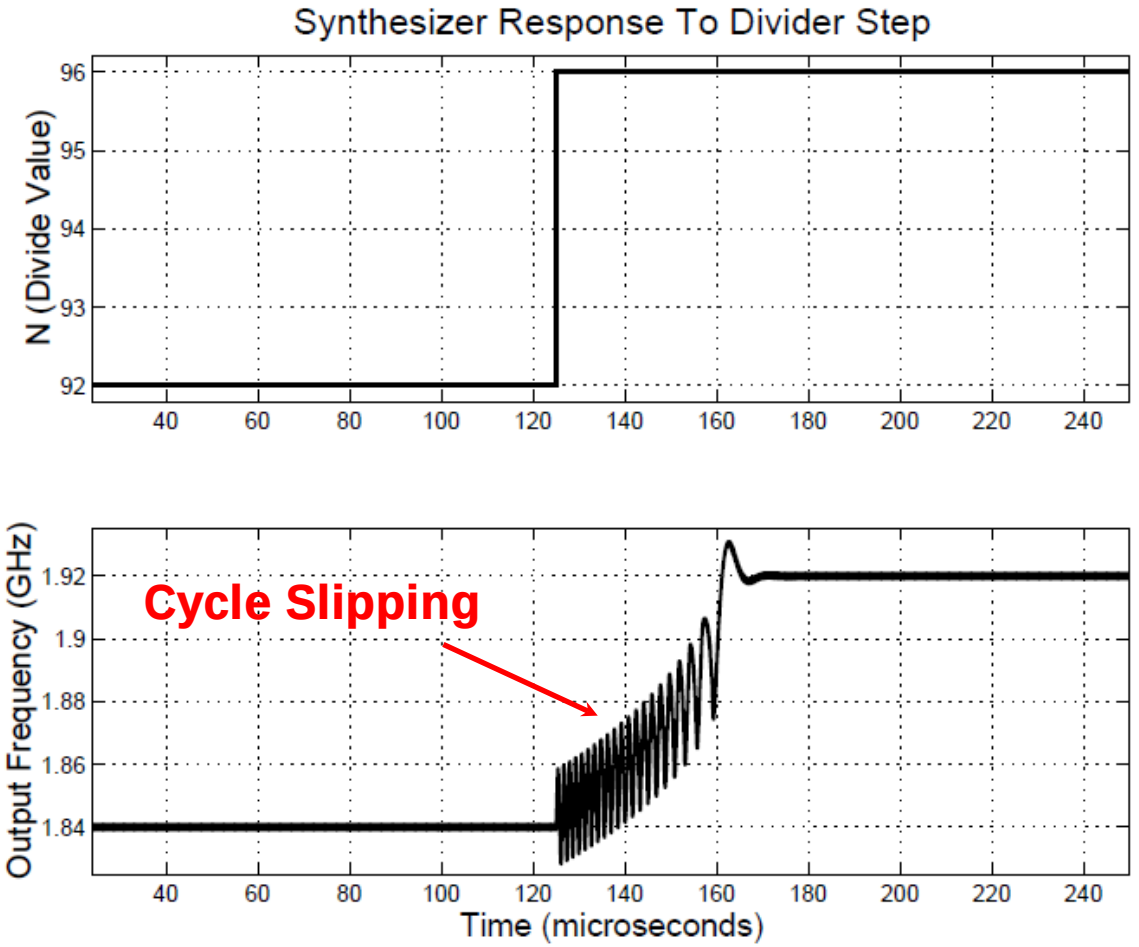


Cycle Slipping

- If there is a frequency difference between the input reference and PLL feedback signals the phase detector can jump between regions of different gain
  - PLL is no longer acting as a linear system



Cycle Slipping

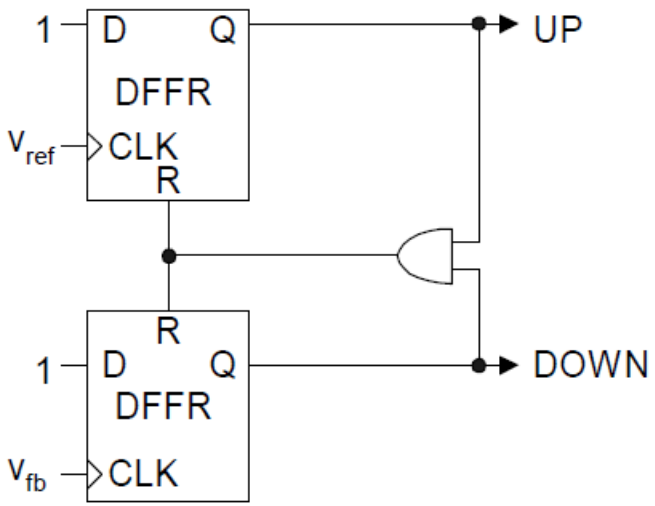


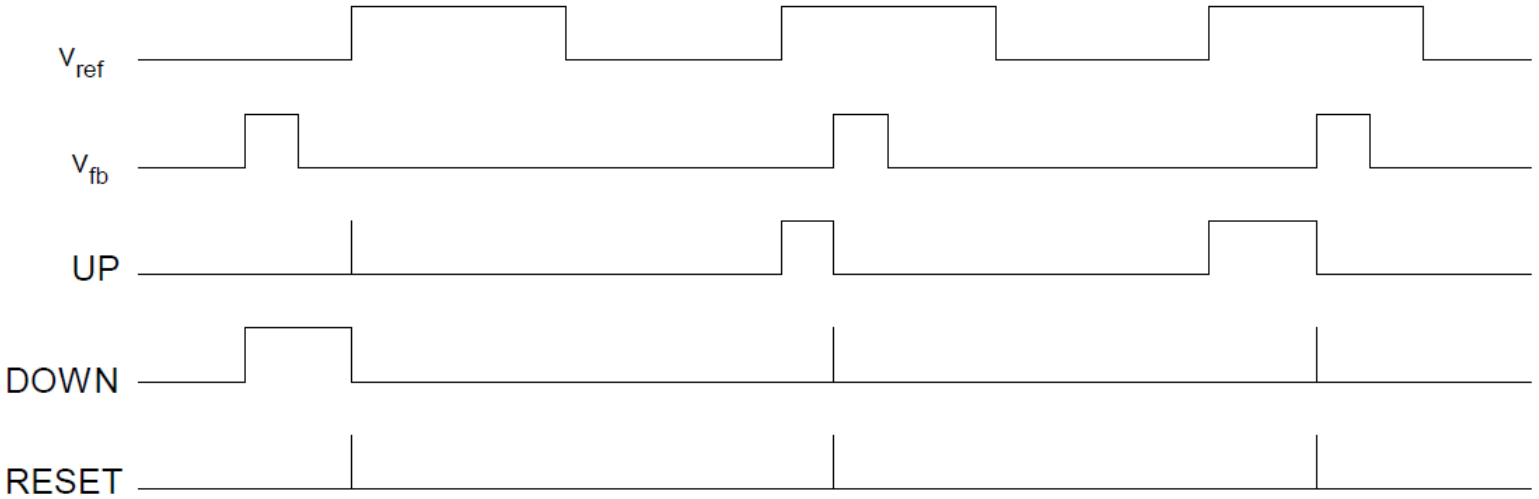
[**Perrott**]

- If frequency difference is too large the PLL may not lock

Phase Frequency Detector (PFD)

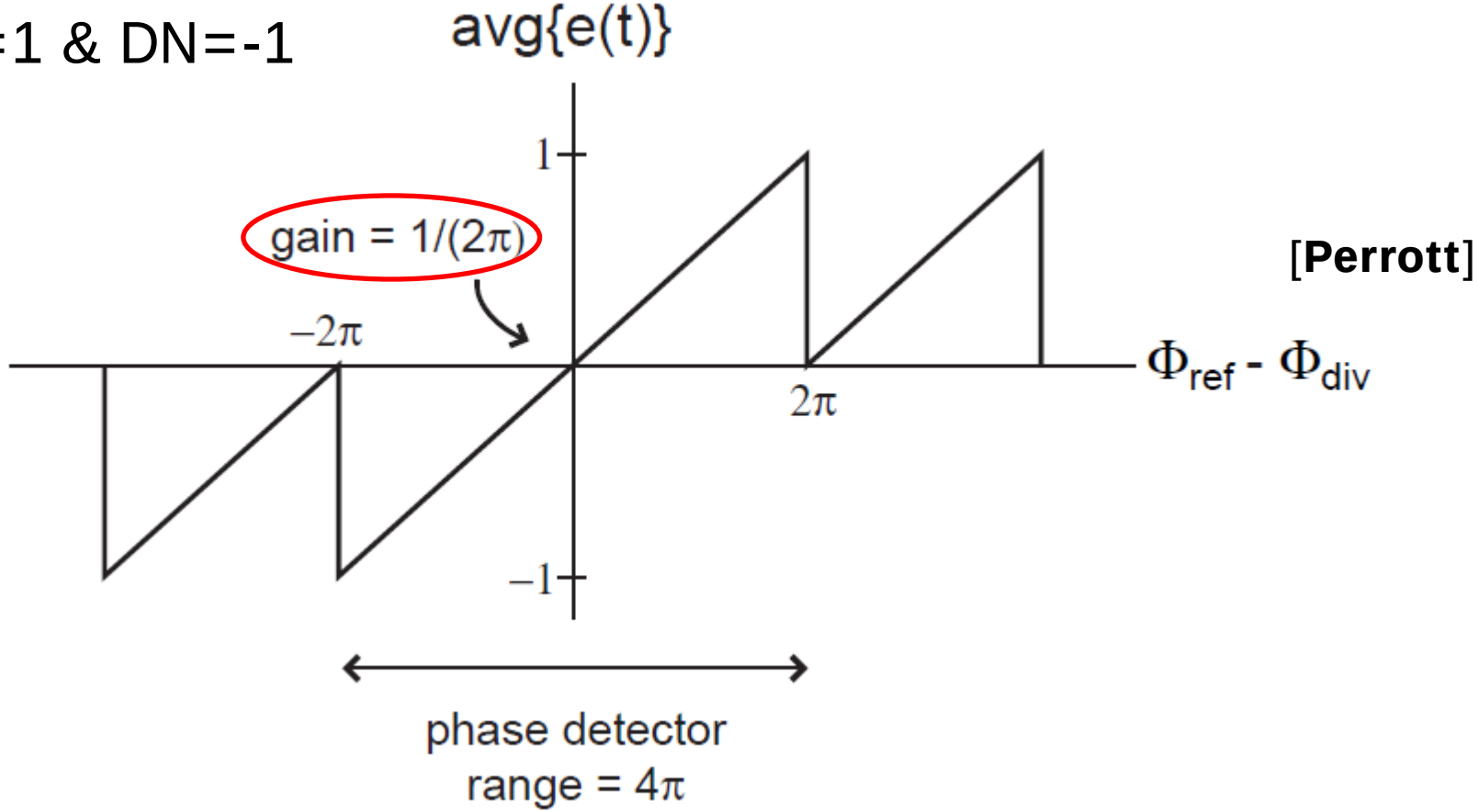
- Phase Frequency Detector allows for wide frequency locking range, potentially entire VCO tuning range
- 3-stage operation with UP and DOWN outputs
- Edge-triggered results in duty cycle insensitivity





PFD Transfer Characteristic

UP=1 & DN=-1

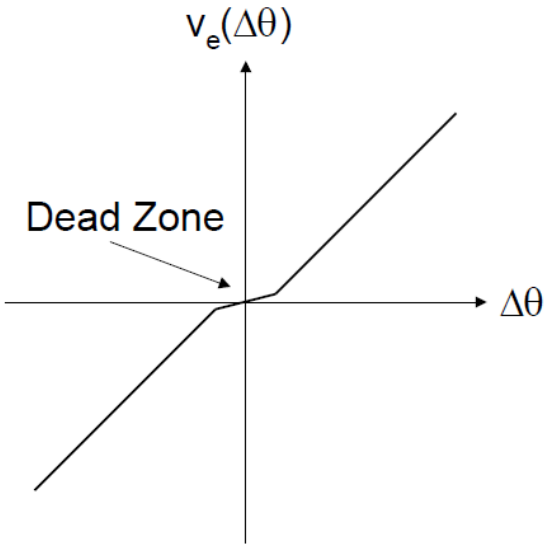


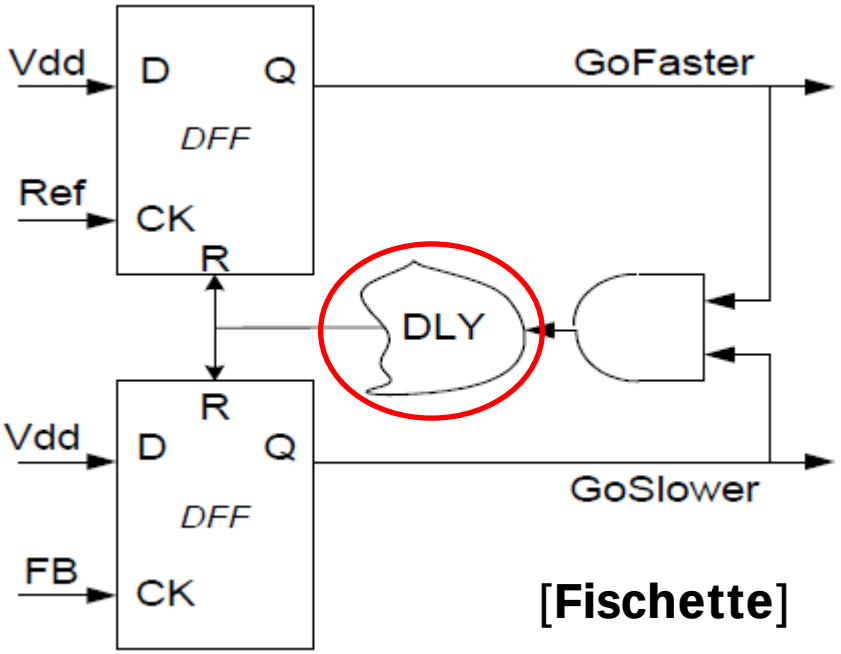
[**Perrott**]

- Constant slope and polarity asymmetry about zero phase allows for wide frequency range operation

PFD Deadzone

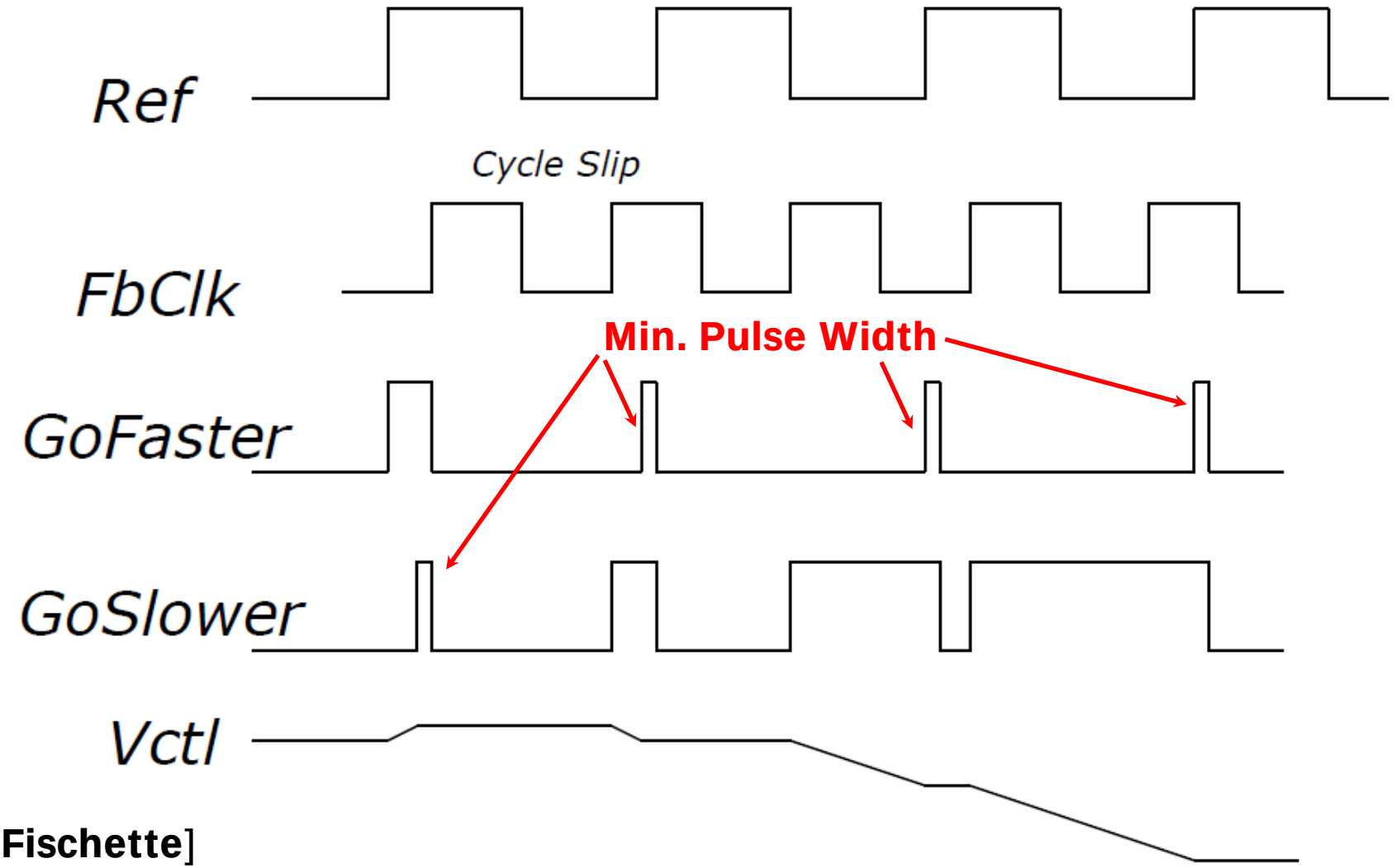
- If phase error is small, then short output pulses are produced by PFD
- Cannot effectively propagate these pulses to switch charge pump
- Results in phase detector “dead zone” which causes low loop gain and increased jitter
- Solution is to add delay in PFD reset path to force a minimum UP and DOWN pulse length





[**Fischette**]

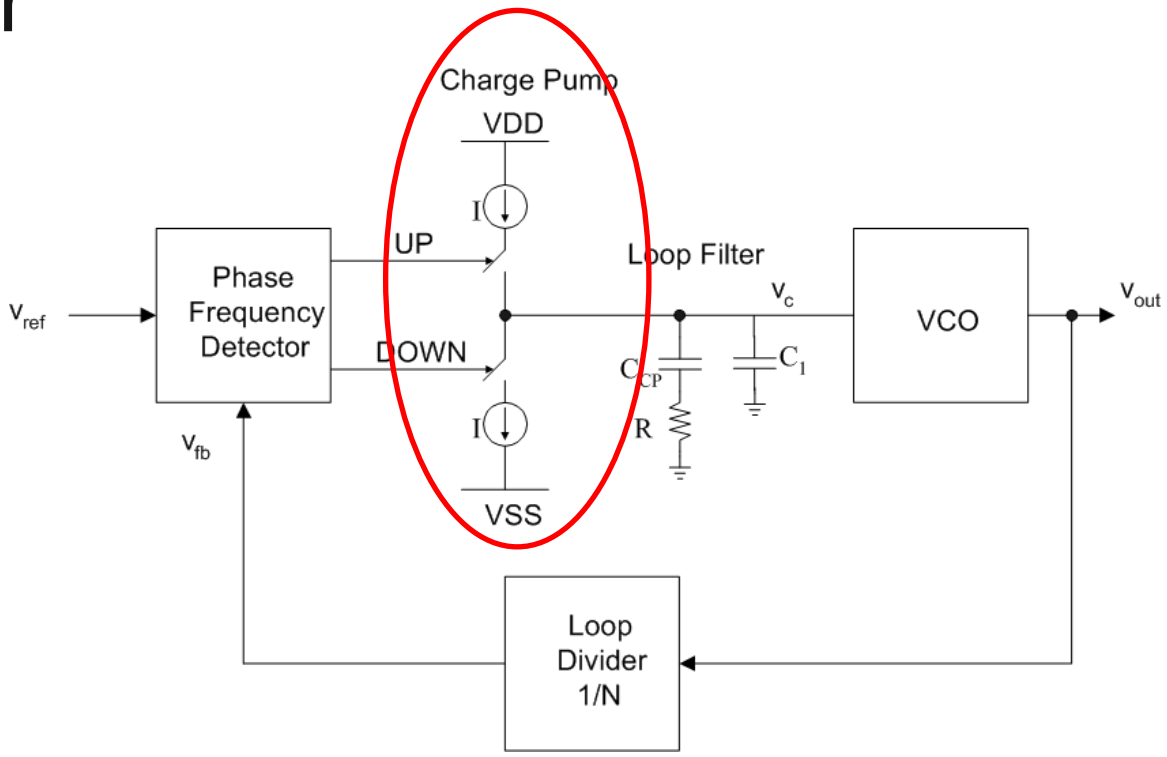
PFD Operation



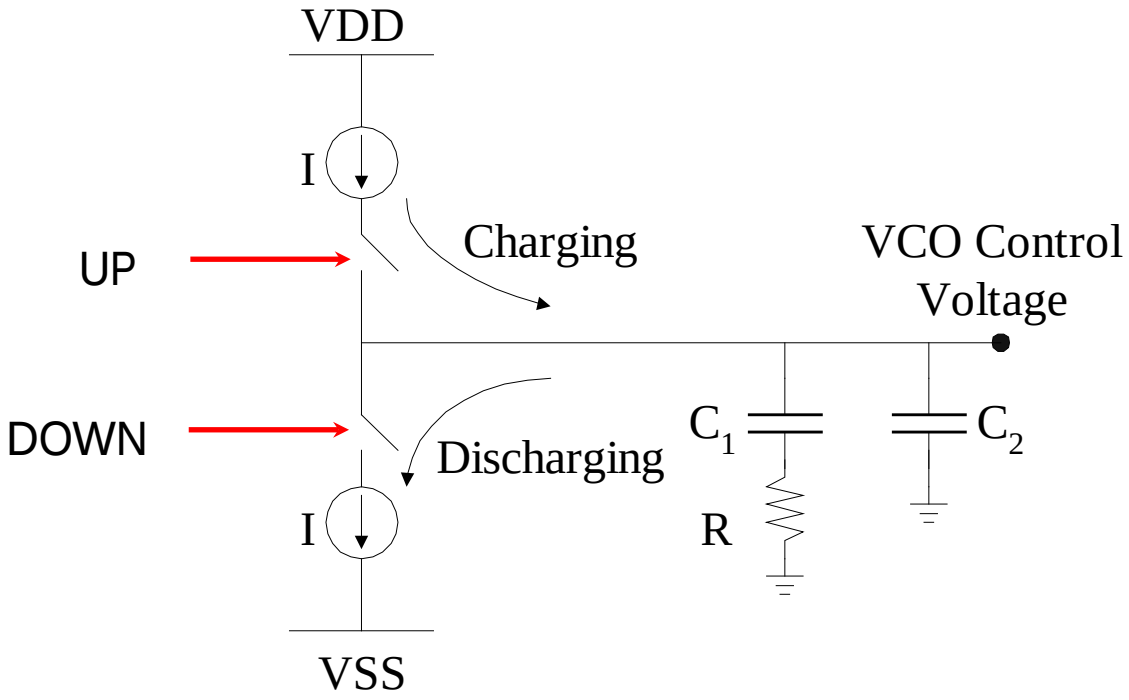
[**Fischette**]

Charge-Pump PLL Circuits

- Phase Detector
- Charge-Pump
- Loop Filter
- VCO
- Divider



Charge Pump

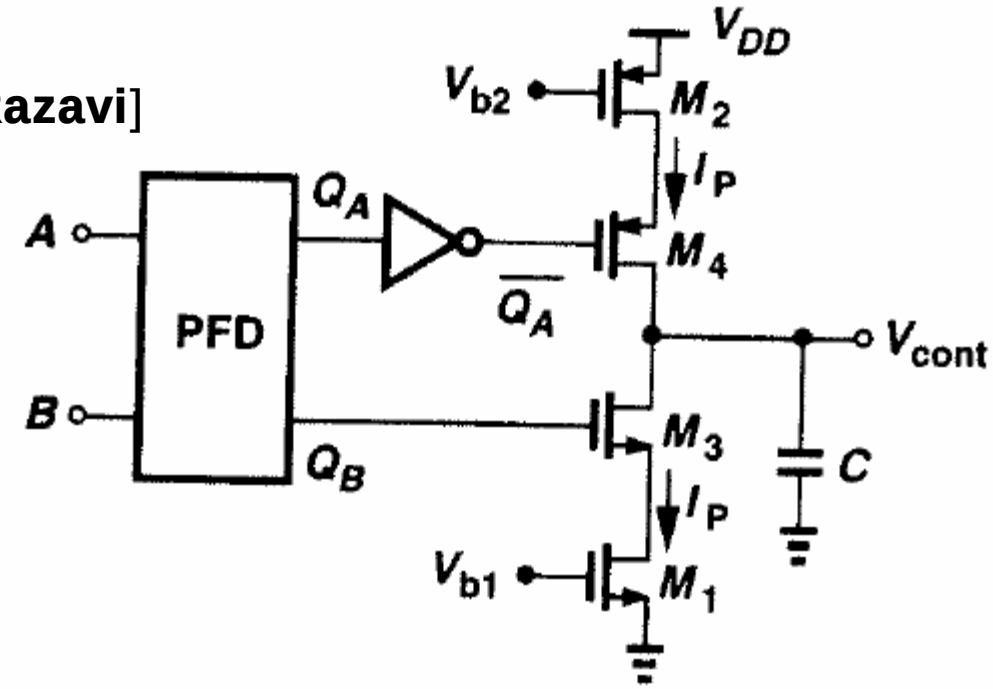


- Converts PFD output signals to charge
- Charge is proportional to PFD pulse widths

PFD-CP Gain: $\left(\frac{1}{2\pi}\right) I_{CP}$

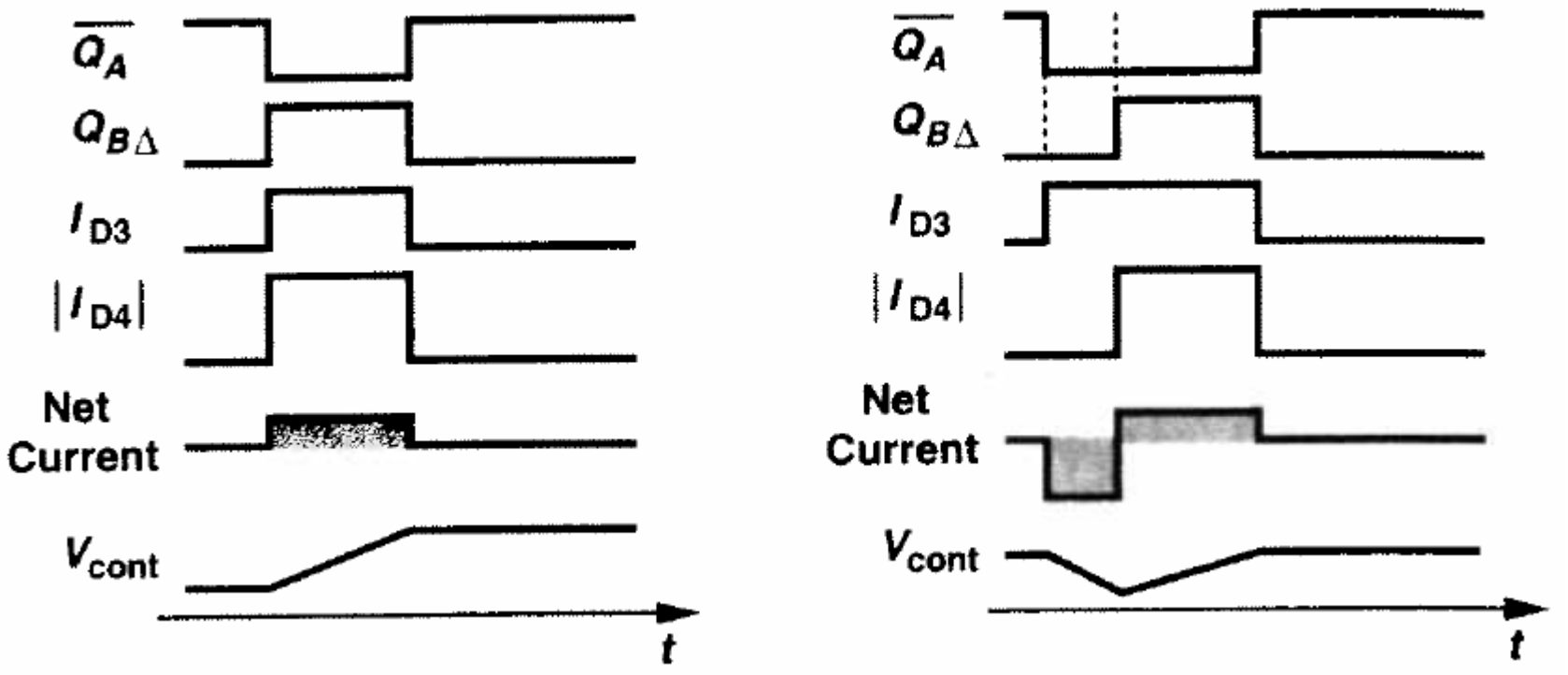
Simple Charge Pump

[**Razavi**]



- Issues
  - Switch resistance can vary Vctrl due to body effect
  - Charge injection from switches onto Vctrl
  - Charge sharing between current source drain nodes and Vctrl

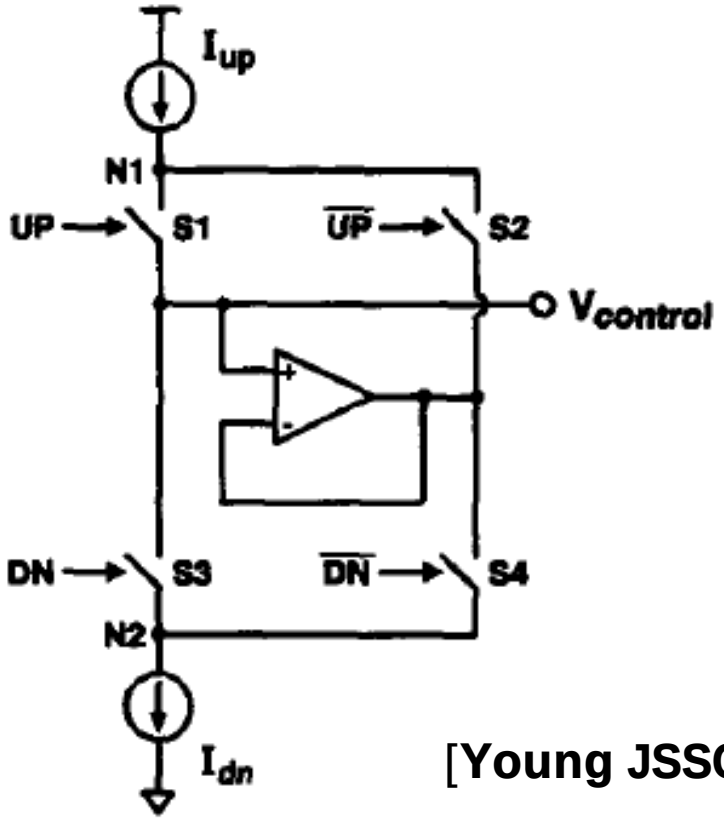
Charge Pump Mismatch



[**Razavi**]

- PLL will lock with static phase error
- Extra “ripple” on Vctrl
  - Results in frequency domain spurs at the reference clock frequency offset from the carrier

Charge Pump w/ Improved Matching

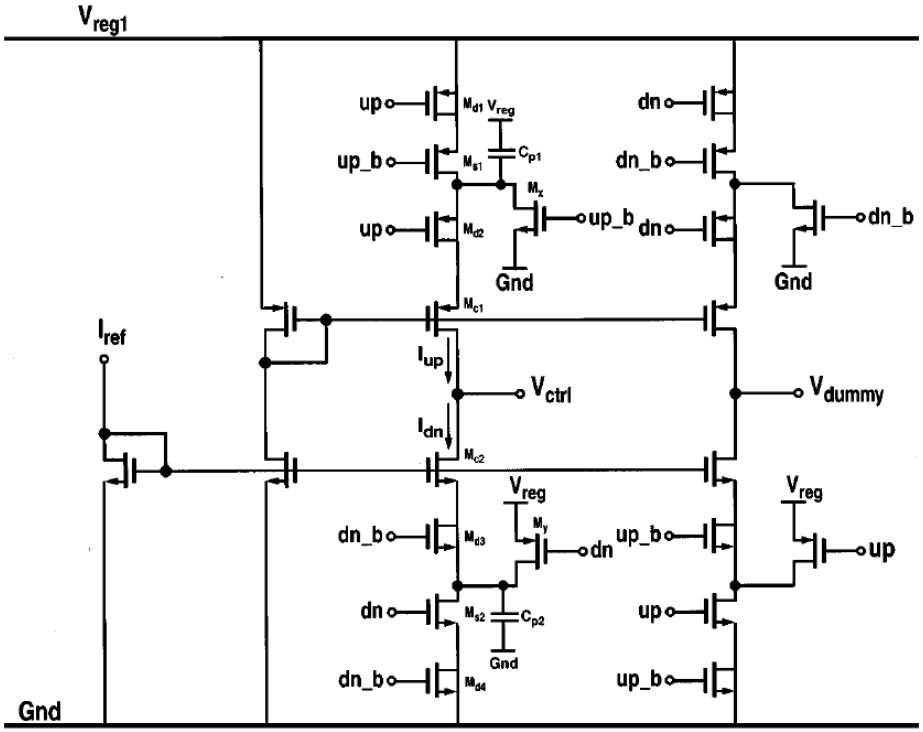


[**Young JSSC 1992**]

- Amplifier keeps current source Vds voltages constant resulting in reduced transient current mismatch

Charge Pump w/ Reversed Switches

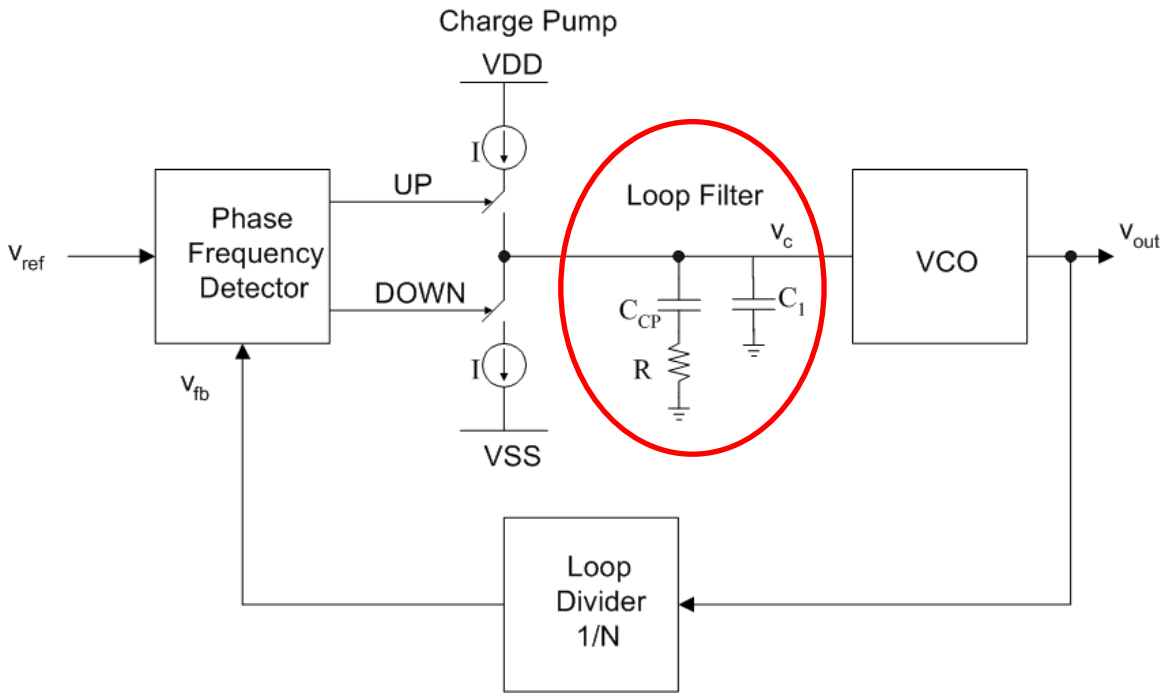
- Swapping switches reduces charge injection
  - MOS caps (Md1-4) provide extra charge injection cancellation
- Helper transistors Mx and My quickly turn-off current source
- Dummy brand helps to match PFD loading



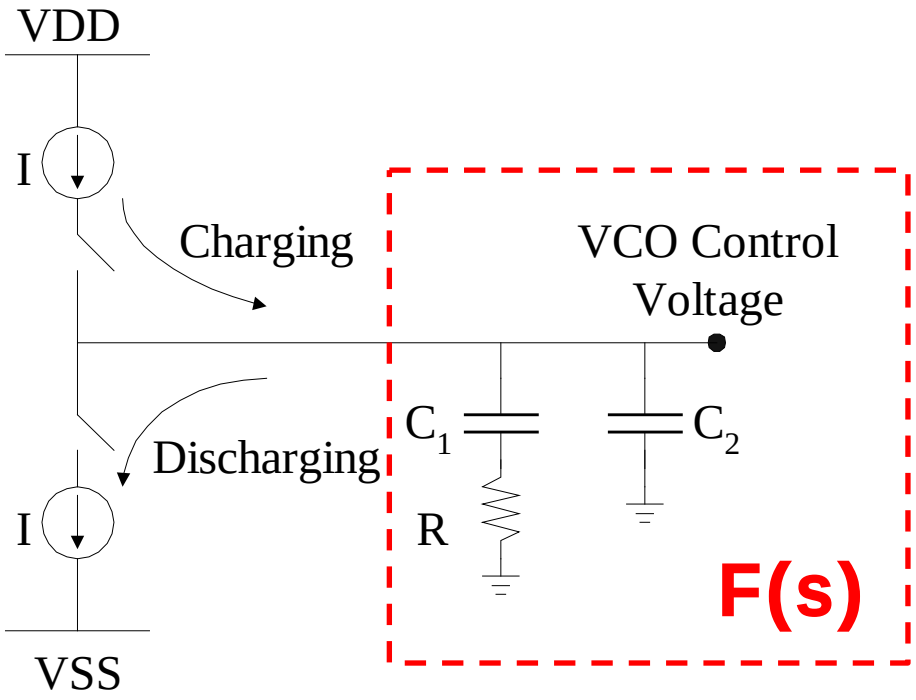
[**Ingino JSSC 2001**]

Charge-Pump PLL Circuits

- Phase Detector
- Charge-Pump
- Loop Filter
- VCO
- Divider



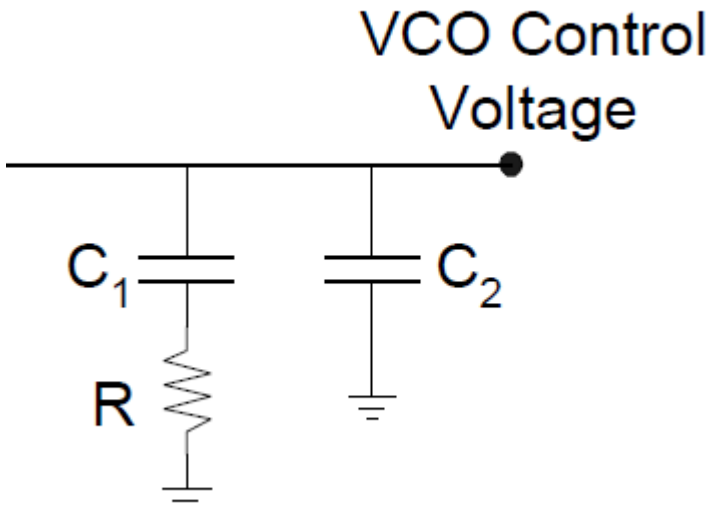
Loop Filter



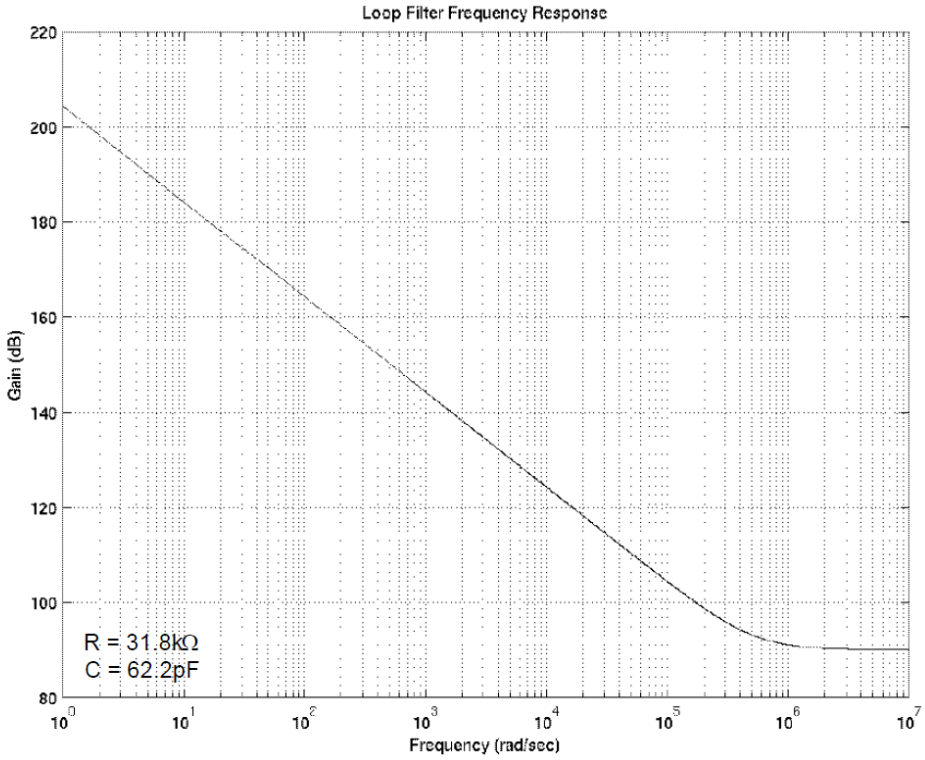
- Lowpass filter extracts average of phase detector error pulses

Loop Filter Transfer Function

- Neglecting secondary capacitor, C_2

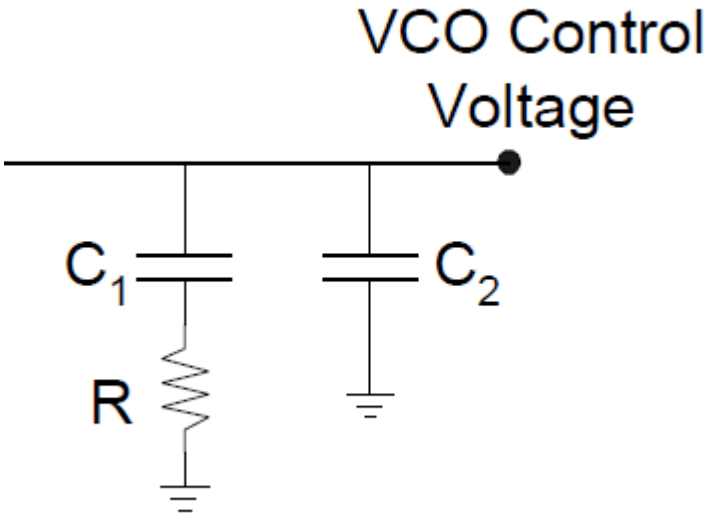


$$F(s) = \frac{V_c(s)}{I_e(s)} = \frac{R\left(s + \frac{1}{RC_1}\right)}{s}$$

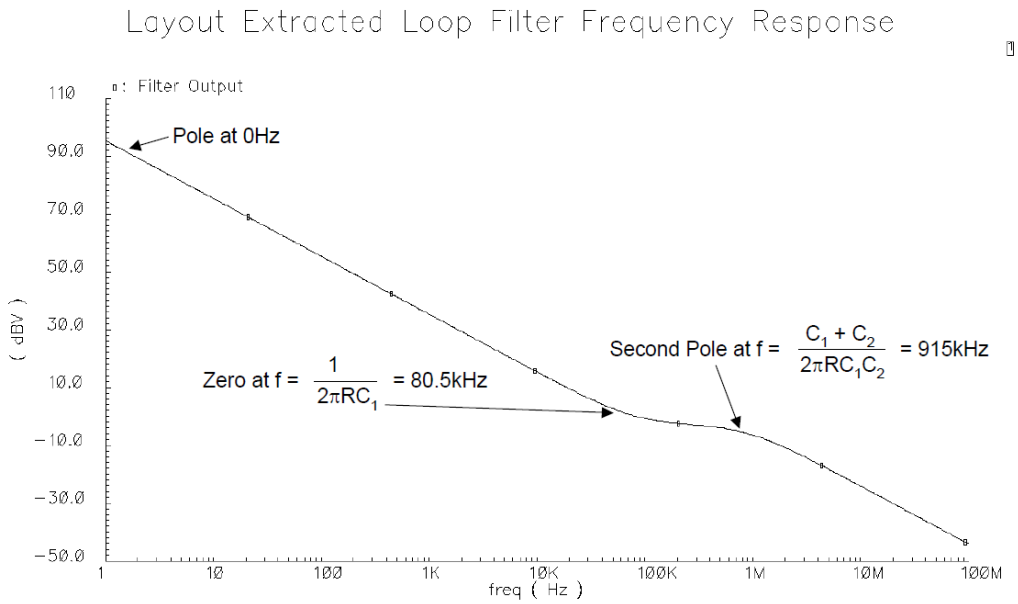


Loop Filter Transfer Function

- With secondary capacitor, C_2

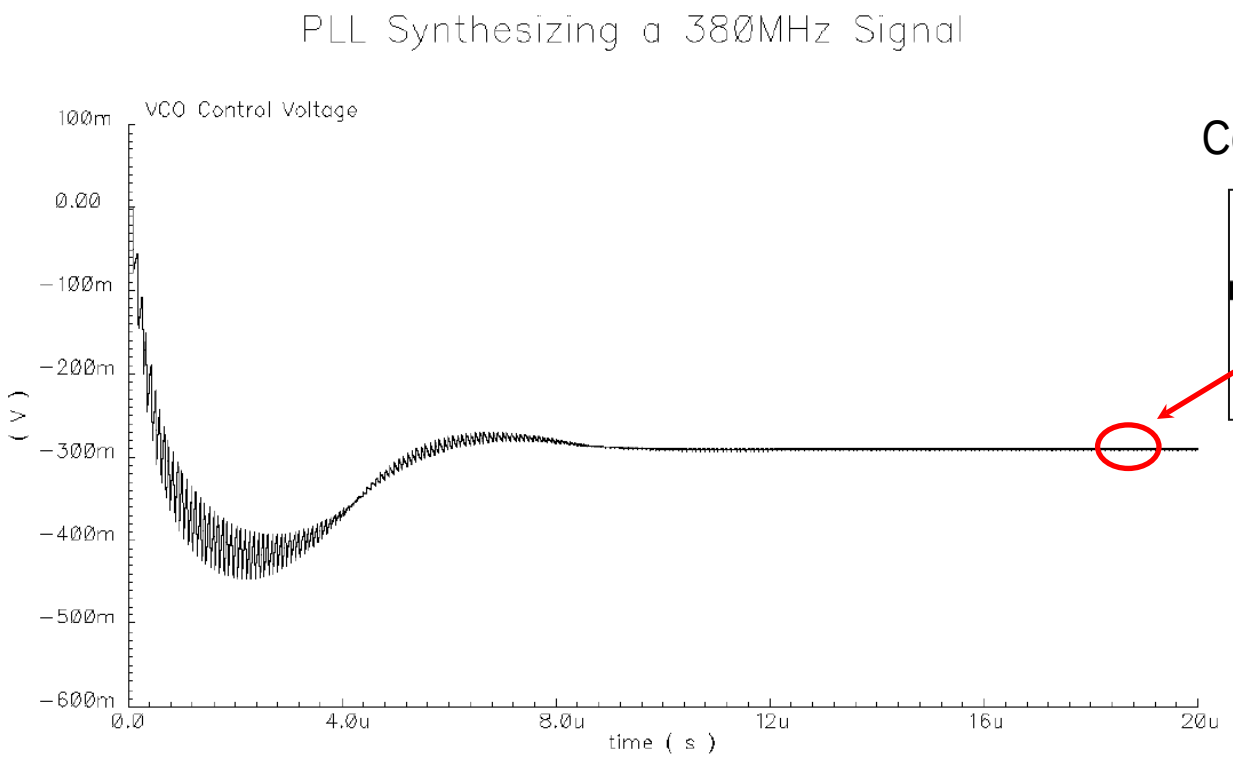


$$Z(s) = \frac{\frac{1}{C_2}\left(s + \frac{1}{RC_1}\right)}{s^2 + \frac{s(C_1 + C_2)}{RC_1C_2}}$$

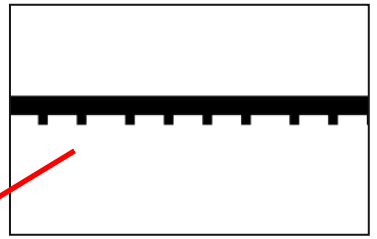


Why have C2?

- Secondary capacitor smoothes control voltage ripple
- Can't make too big or loop will go unstable
  - $C_2 < C_1/10$ for stability
  - $C_2 > C_1/50$ for low jitter



Control Voltage Ripple

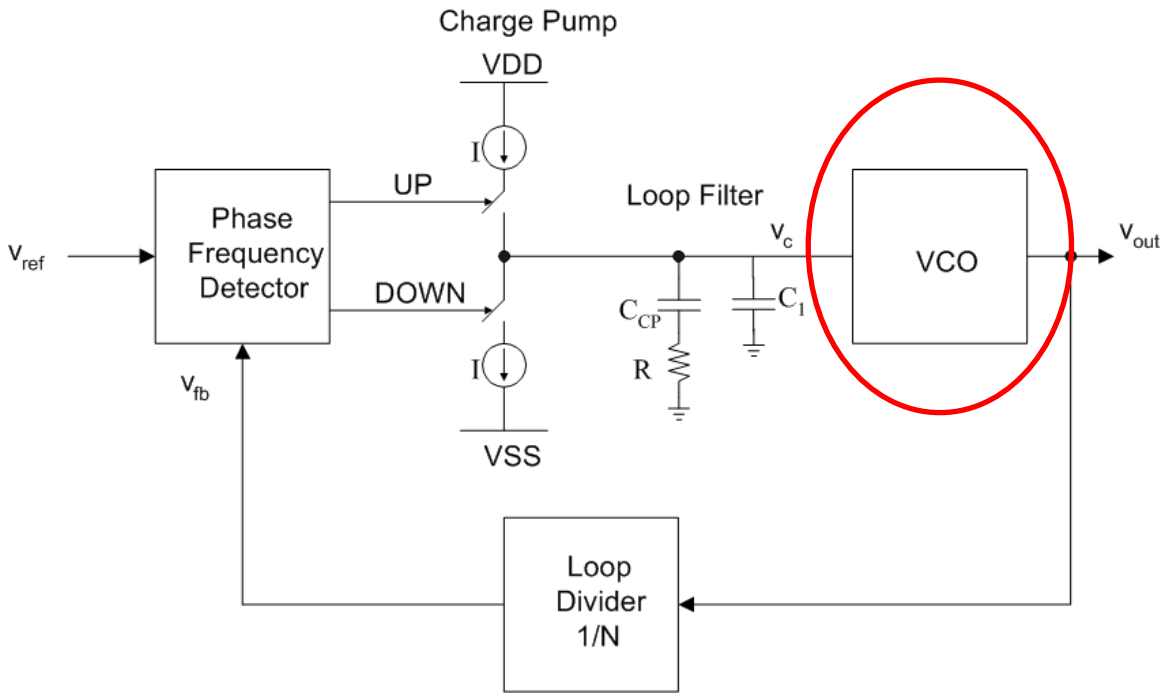


Filter Capacitors

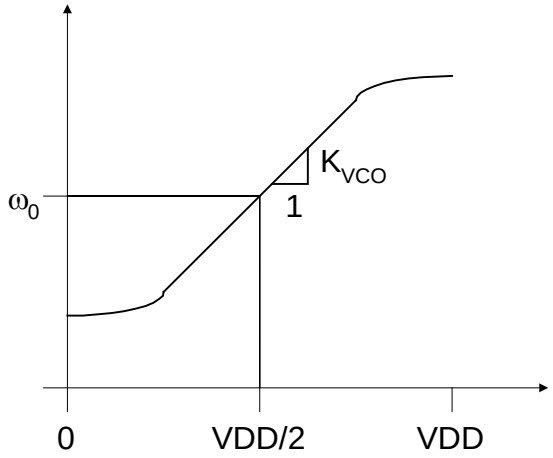
- To minimize area, we would like to use highest density caps
- Thin oxide MOS cap gate leakage can be an issue
  - Similar to adding a non-linear parallel resistor to the capacitor
  - Leakage is voltage and temperature dependent
  - Will result in excess phase noise and spurs
- Metal caps or thick oxide caps are a better choice
  - Trade-off is area
- Metal cap density can be < 1/10 thin oxide caps
- Filter cap frequency response can be relatively low, as PLL loop bandwidths are typically 1-50MHz

Charge-Pump PLL Circuits

- Phase Detector
- Charge-Pump
- Loop Filter
- VCO
- Divider



Voltage-Controlled Oscillator

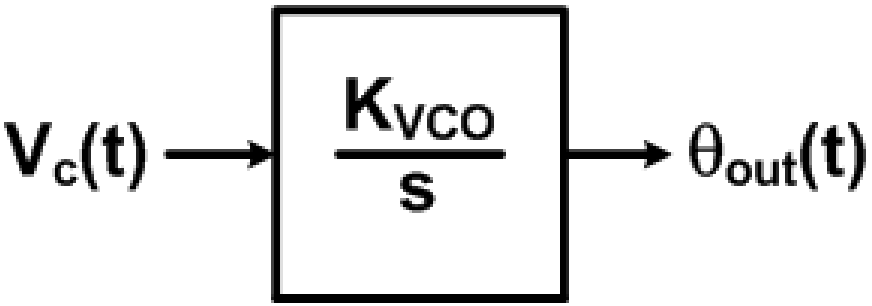


$$\omega_{out}(t) = \omega_0 + \Delta\omega_{out}(t) = \omega_0 + K_{VCO} v_c(t)$$

- Time-domain phase relationship

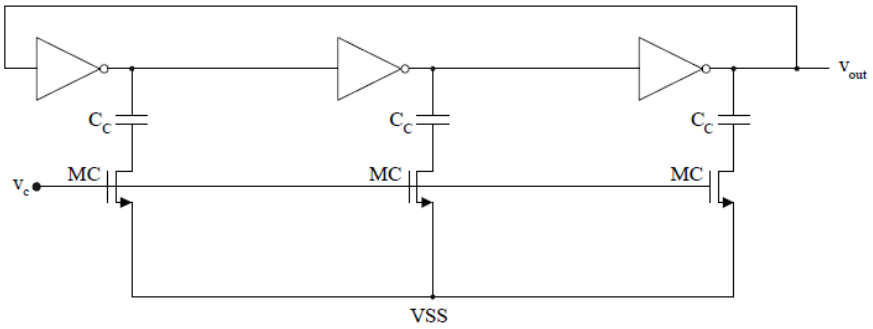
$$\theta_{out}(t) = \int \Delta\omega_{out}(t)\mathrm{dt} = K_{VCO} \int v_c(t)\mathrm{dt}$$

Laplace Domain Model

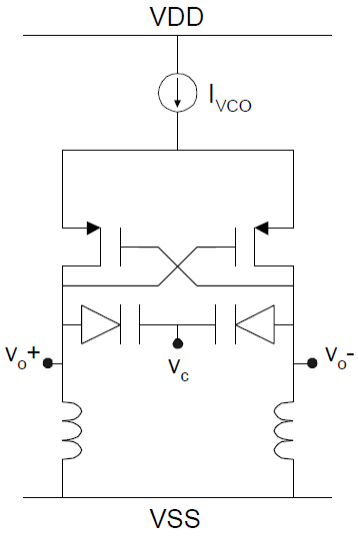


Voltage-Controlled Oscillators (VCO)

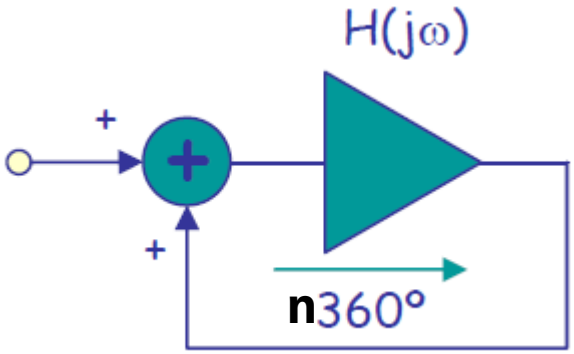
- Ring Oscillator
  - Easy to integrate
  - Wide tuning range (5x)
  - Higher phase noise



- LC Oscillator
  - Large area
  - Narrow tuning range (20-30%)
  - Lower phase noise



Barkhausen's Oscillation Criteria



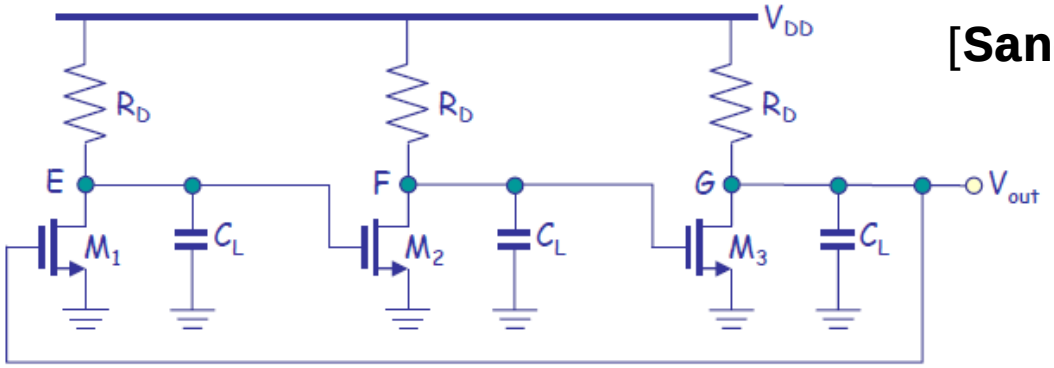
[**Sanchez**]

Closed-loop transfer function: $\frac{H(j\omega)}{1-H(j\omega)}$

- Sustained oscillation occurs if $H(j\omega)=1$
- 2 conditions:
  - Gain = 1 at oscillation frequency ω_0
  - Total phase shift around loop is n360° at oscillation frequency ω_0

Ring Oscillator Example

[Sanchez]



Three-stage ring oscillator

$$H(s) = -\frac{A_0^3}{\left(1+\frac{s}{\omega_0}\right)^3}$$

$$\omega_{osc} = \sqrt{3}\omega_0$$

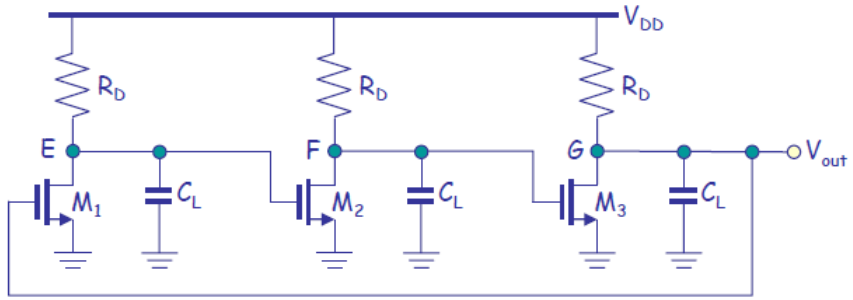
$$\tan^{-1}\frac{\omega_{osc}}{\omega_o} = 60^\circ$$

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{-A_0^3}{(1+s/\omega_0)^3}}{1+\frac{A_0^3}{(1+s/\omega_0)^3}} = \frac{-A_0^3}{(1+s/\omega_0)^3 + A_0^3}$$

$$\frac{A_0^3}{\left[\sqrt{1+\left(\frac{\omega_{osc}}{\omega_0}\right)^2}\right]^3} = 1$$

$$A_0 = 2$$

Ring Oscillator Example



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[**Sanchez**]

- 4-stage oscillator
  - A0 = sqrt(2)
  - Phase shift = 45
- Easier to make a larger-stage oscillator oscillate, as it requires less gain and phase shift per stage

Next Time

- PLL wrap-up
- CDRs