ECEN689: Special Topics in High-Speed Links Circuits and Systems Spring 2010

Lecture 25: Clocking Architectures

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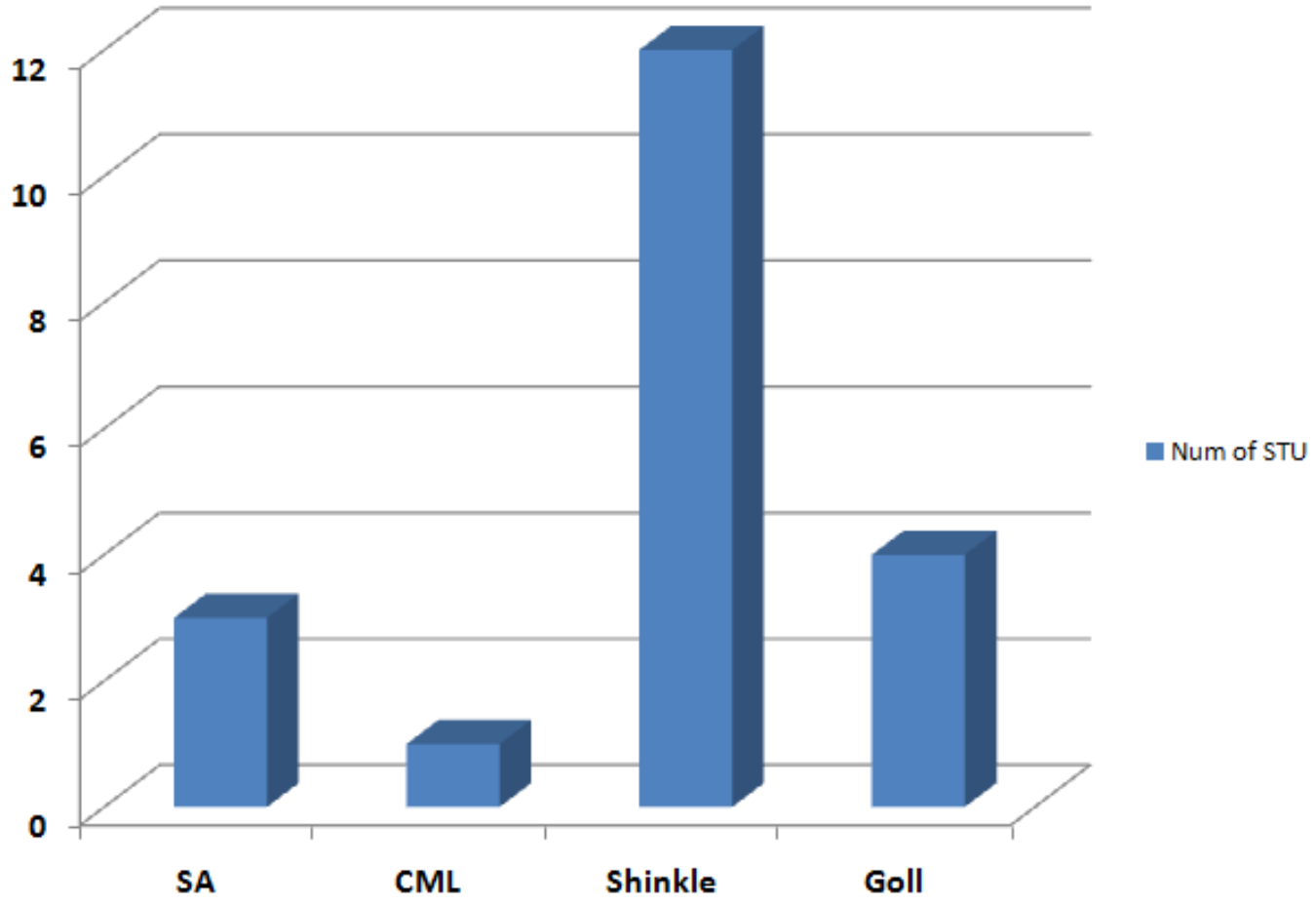
Announcements

- Project Preliminary Report #1 due April 16 (in class)
- Exam 2 is April 30
- Reading
  - Will post some clocking papers

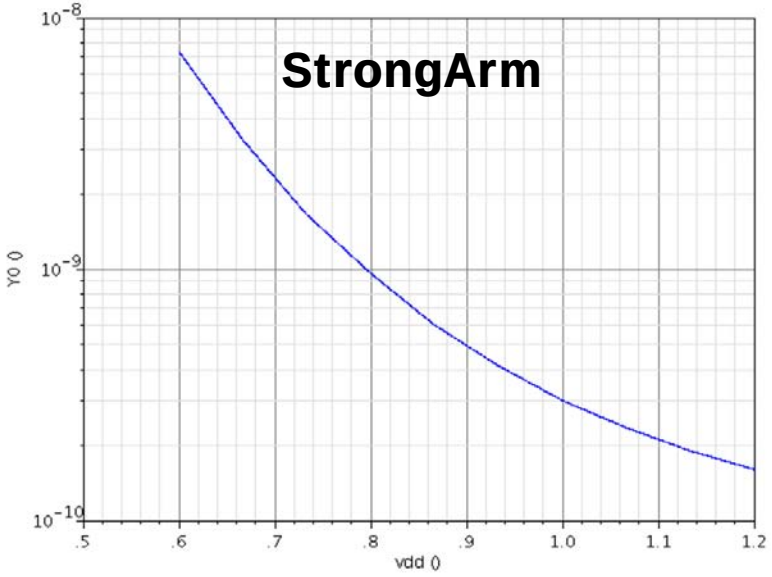
Agenda

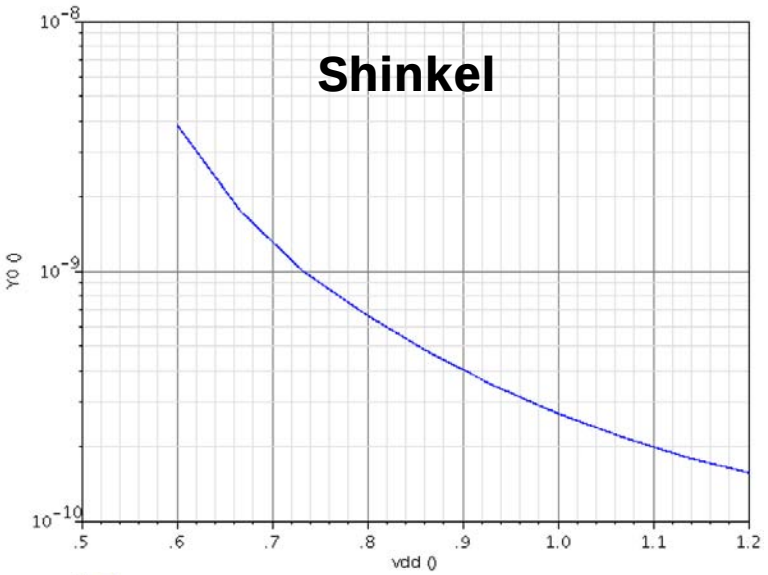
- Project Overview
- HW5 Discussion
- Clocking Architectures

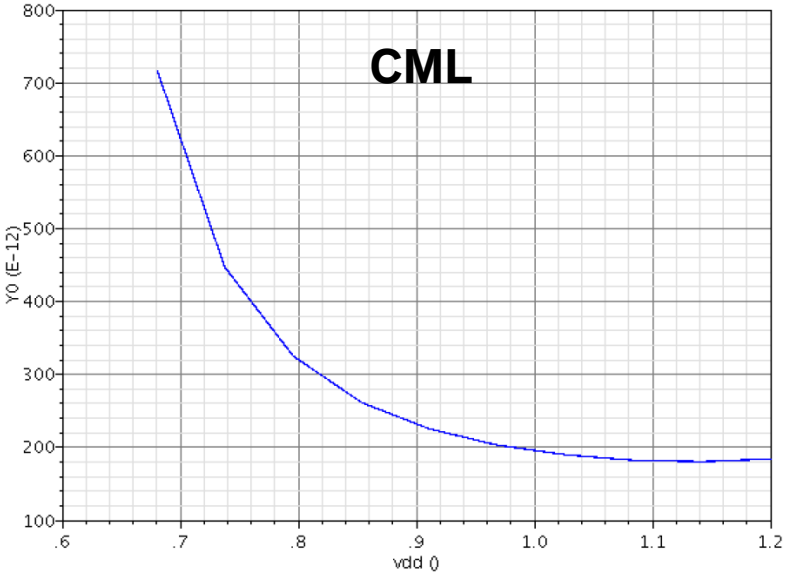
HW5 Comparator Survey

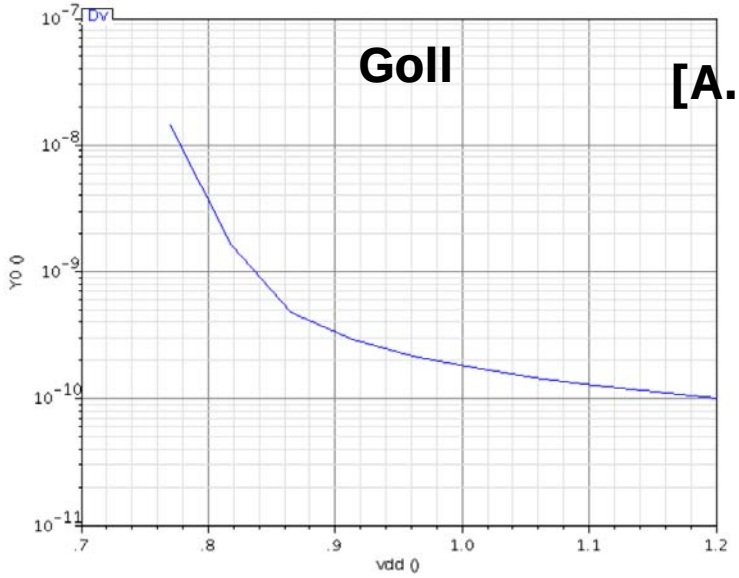


HW5 Comparator Delay vs VDD





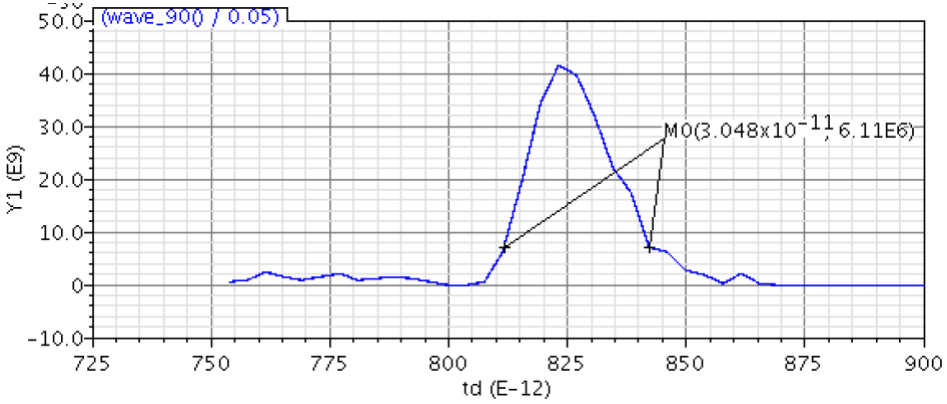




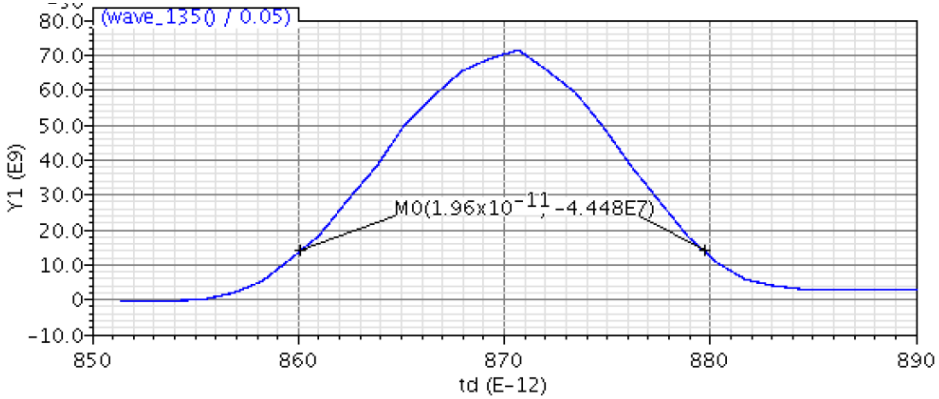
[A. Amin]

HW5 Comparator ISF

StrongArm: 30ps



Shinkel: 20ps



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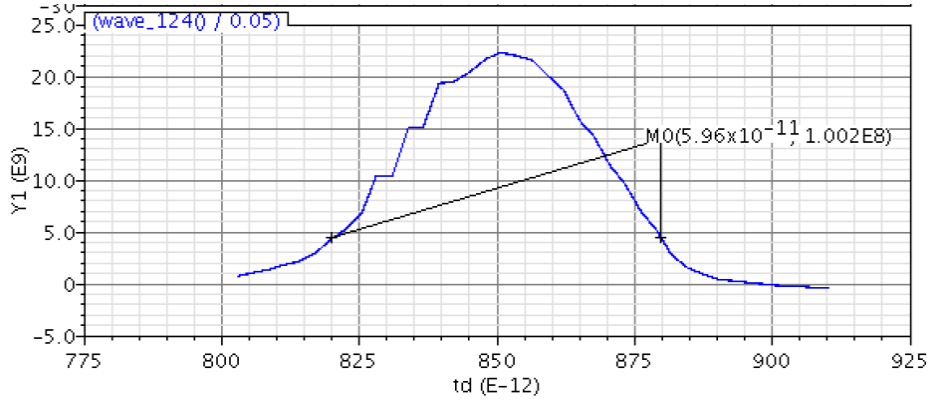
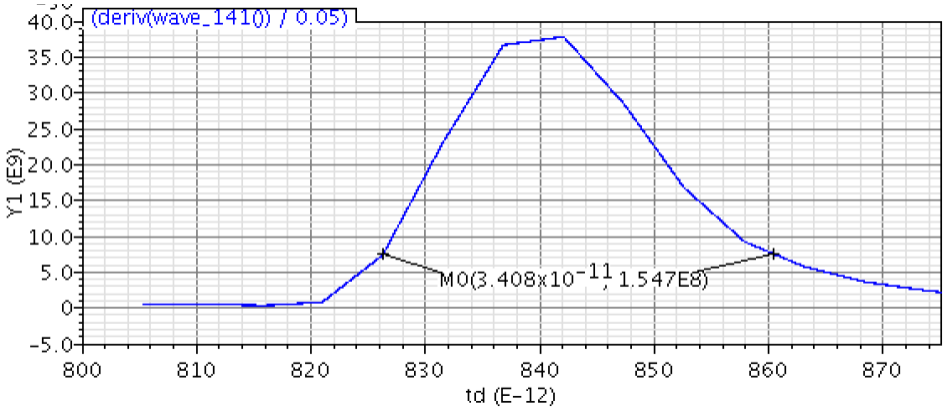
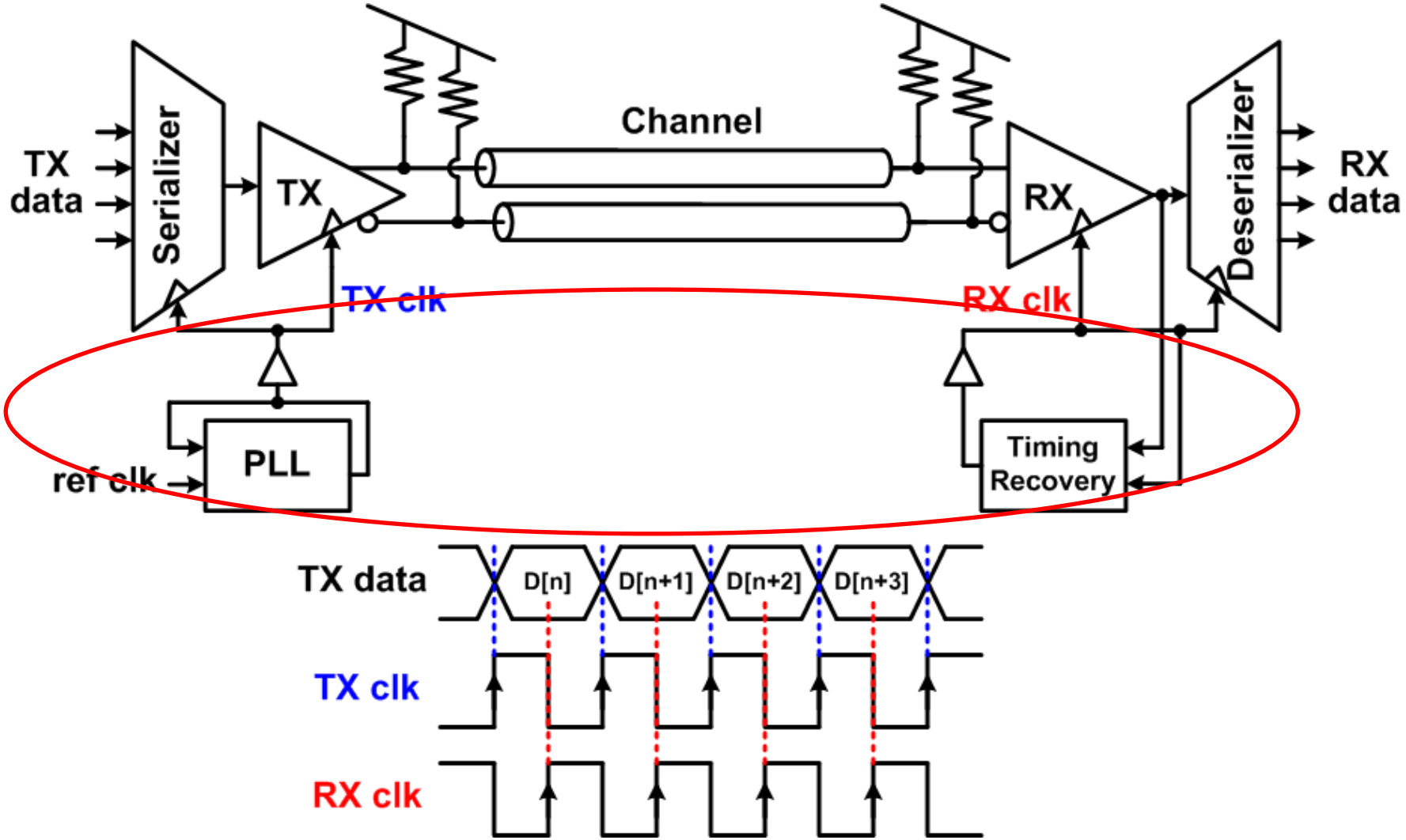
CML: 60ps



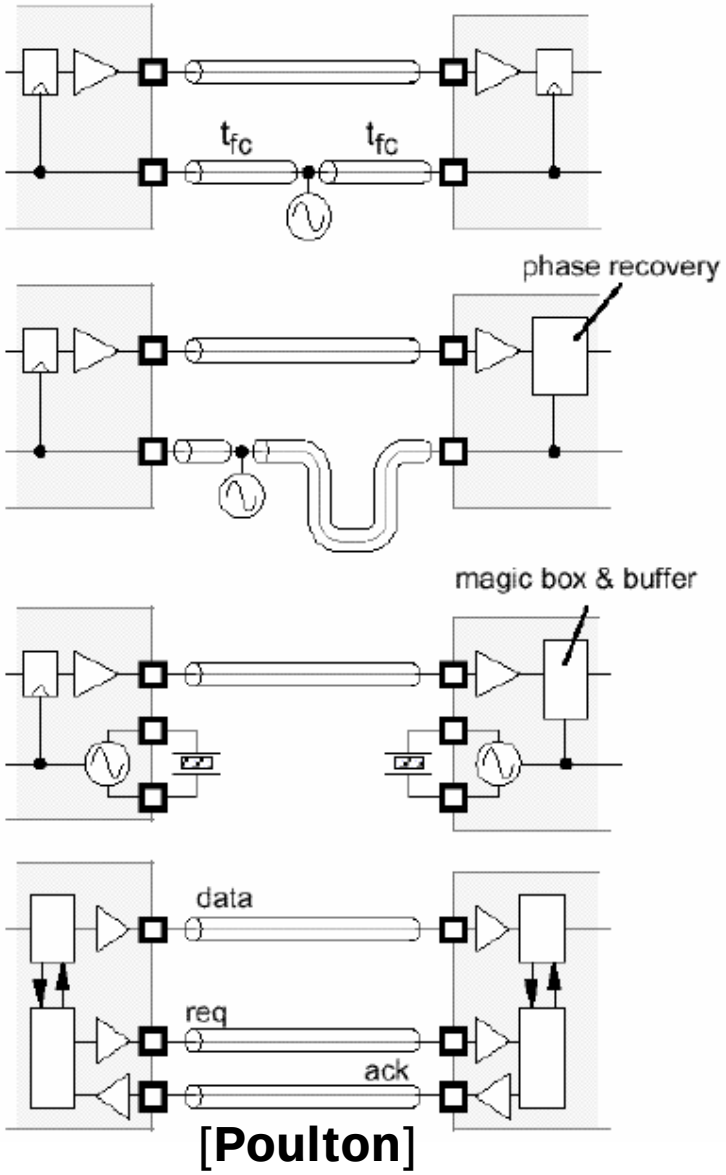
Goll: 34ps



High-Speed Electrical Link System



Clocking Terminology



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Synchronous

- Every chip gets same frequency AND phase
- Used in low-speed busses

Mesochronous

- Same frequency, but unknown phase
- Requires phase recovery circuitry
  - Can do with or without full CDR
- Used in fast memories, internal system interfaces, MAC/Packet interfaces

Plesiochronous

- Almost the same frequency, resulting in slowly drifting phase
- Requires CDR
- Widely used in high-speed links

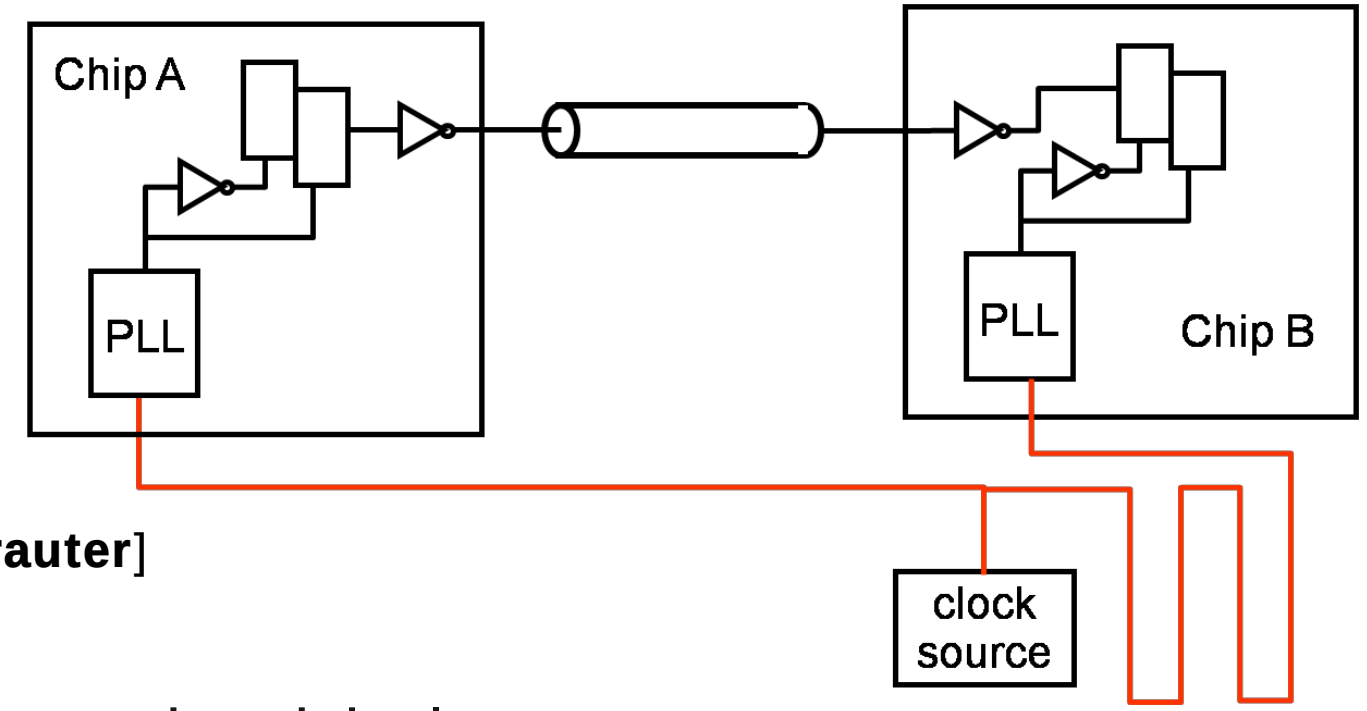
Asynchronous

- No clocks at all
- Request/acknowledge handshake procedure
- Used in embeddded systems, Unix, Linux

I/O Clocking Architectures

- Three basic I/O architectures
  - Common Clock (Synchronous)
  - Forward Clock (Source Synchronous)
  - Embedded Clock (Clock Recovery)
- These I/O architectures are used for varying applications that require different levels of I/O bandwidth
- A processor may have one or all of these I/O types
- Often the same circuitry can be used to emulate different I/O schemes for design reuse

Common Clock I/O Architecture



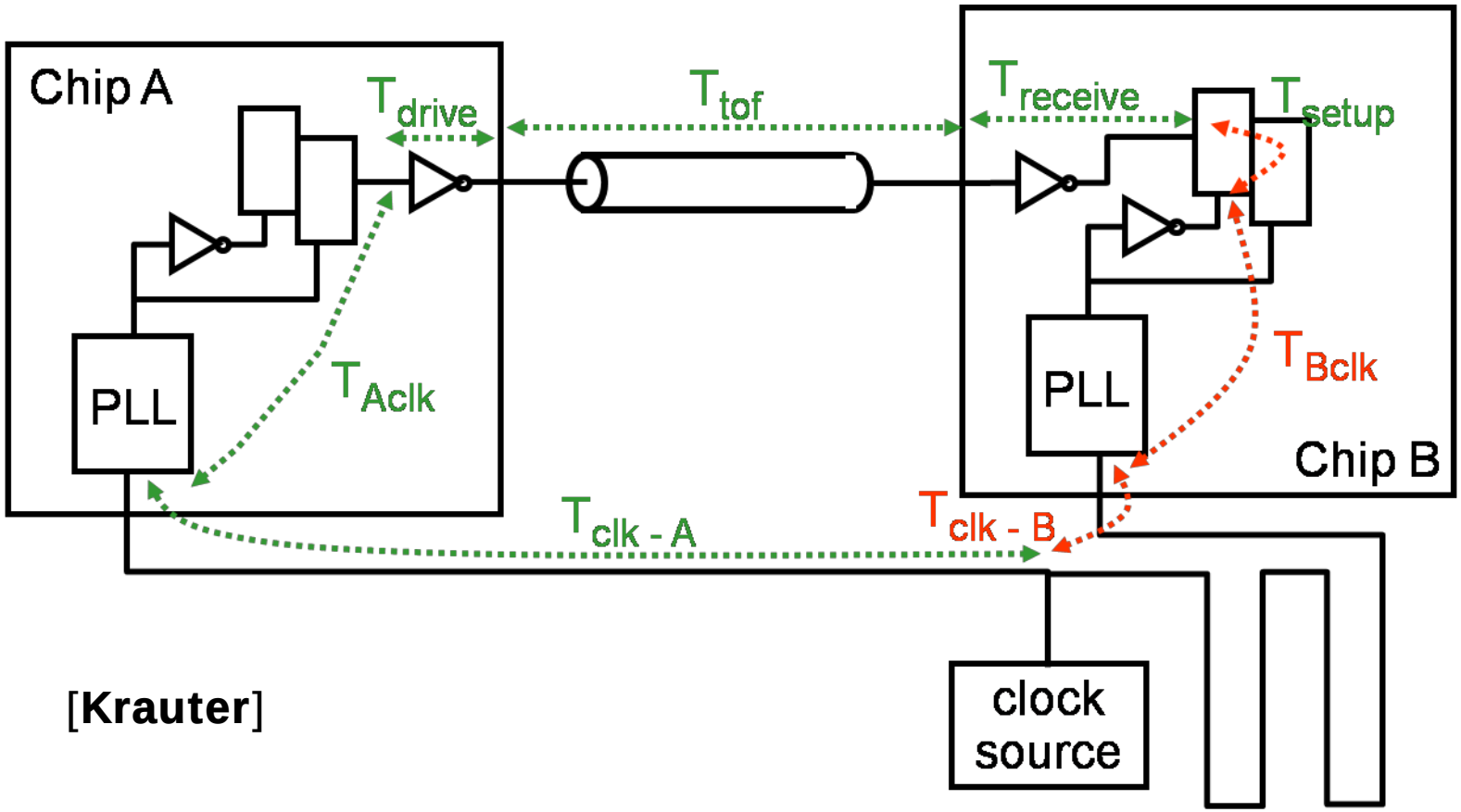
[**Krauter**]

- Common in original computer systems
- Synchronous system
- Common bus clock controls chip-to-chip transfers
- Requires equal length routes to chips to minimize clock skew
- Data rates typically limited to ~100Mb/s

Common Clock I/O Cycle Time

Cycle time to meet setup time

$$\max(T_{clk-A}+T_{Aclk}+T_{drive}+T_{tof}+T_{receive}+T_{setup}) - \min(T_{Bclk}-T_{clk-B}) < T_{cycle}$$



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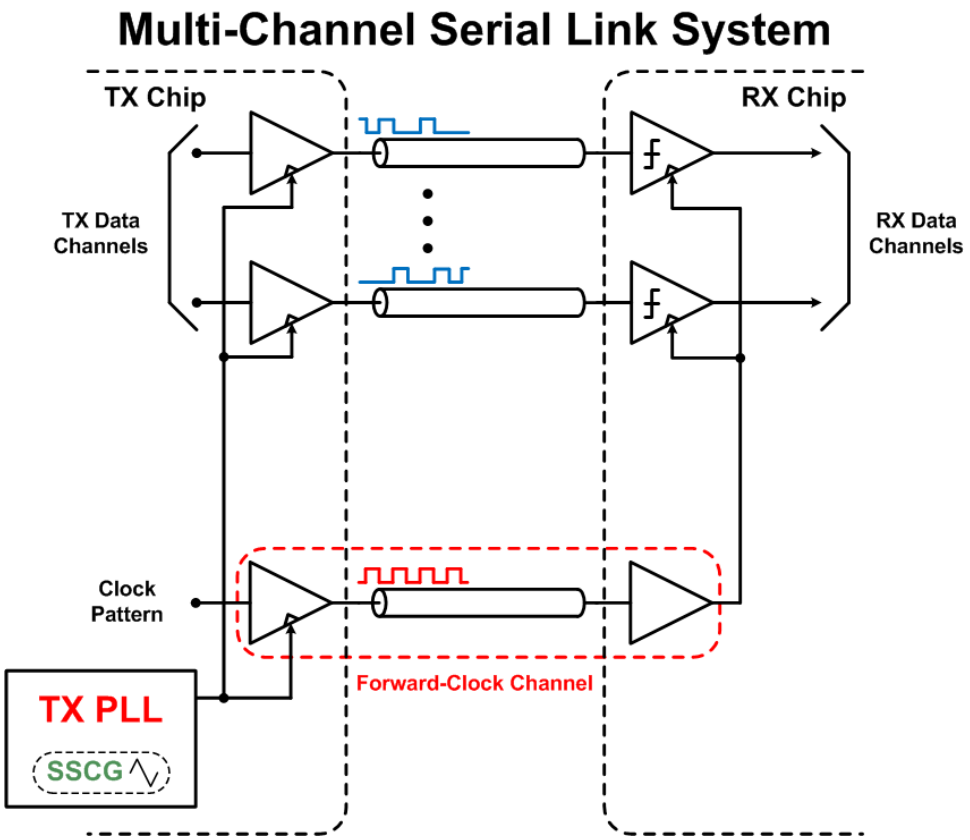
Common Clock I/O Limitations

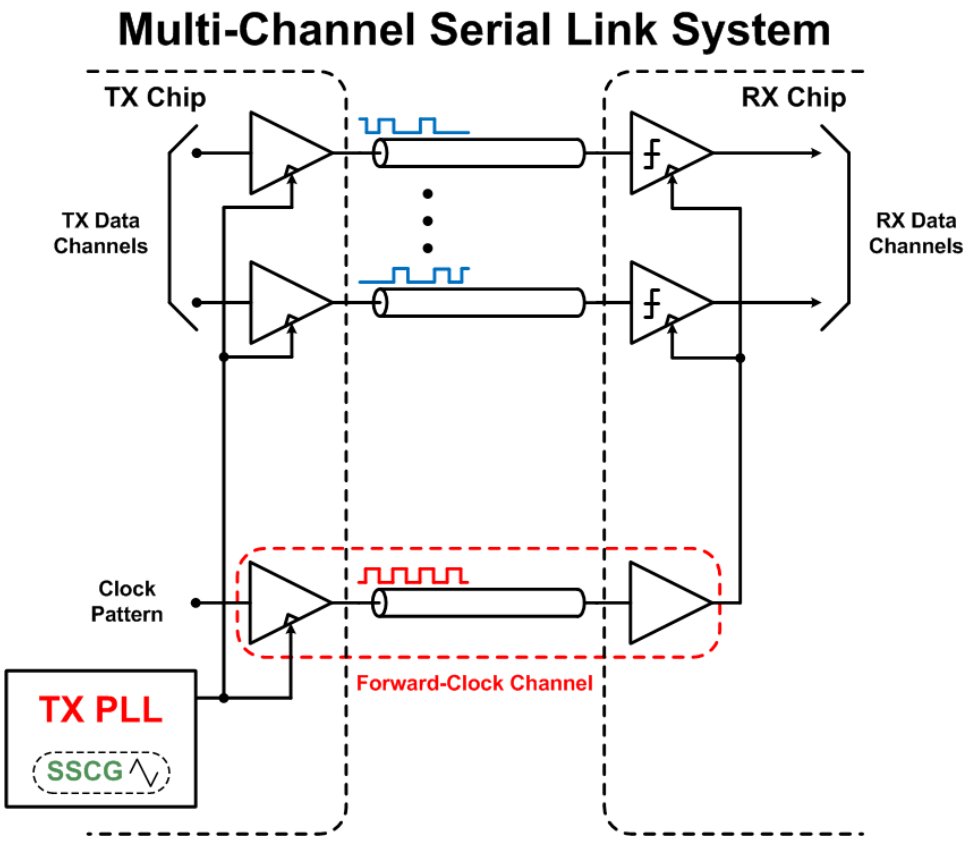
- Difficult to control clock skew and propagation delay
- Need to have tight control of absolute delay to meet a given cycle time
- Sensitive to delay variations in on-chip circuits and board routes
- Hard to compensate for delay variations due to low correlation between on-chip and off-chip delays
- While commonly used in on-chip communication, offers limited speed in I/O applications

Forward Clock I/O Architecture



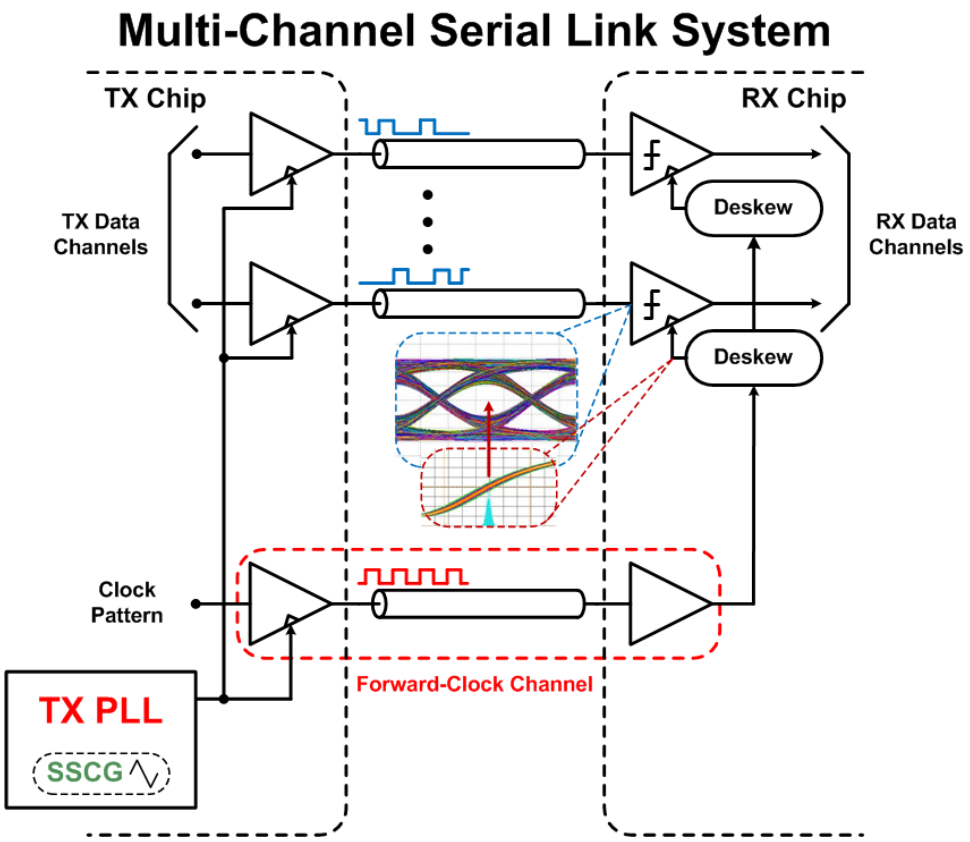
- Common high-speed reference clock is forwarded from TX chip to RX chip
  - Mesochronous system
- Used in processor-memory interfaces and multi-processor communication
  - Intel QPI
  - Hypertransport
- Requires one extra clock channel
- “Coherent” clocking allows low-to-high frequency jitter tracking
- Need good clock receive amplifier as the forwarded clock is attenuated by the channel

Forward Clock I/O Limitations



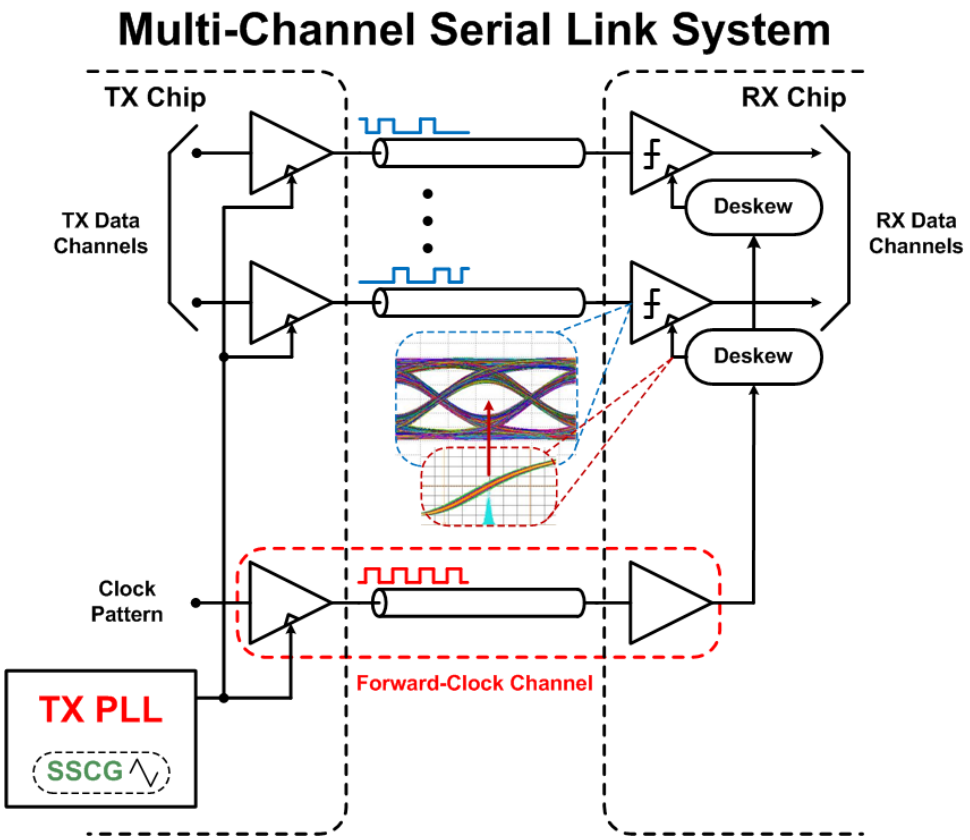
- Clock skew can limited forward clock I/O performance
  - Driver strength and loading mismatches
  - Interconnect length mismatches
- Low pass channel causes jitter amplification
- Duty-Cycle variations of forwarded clock

Forward Clock I/O De-Skew



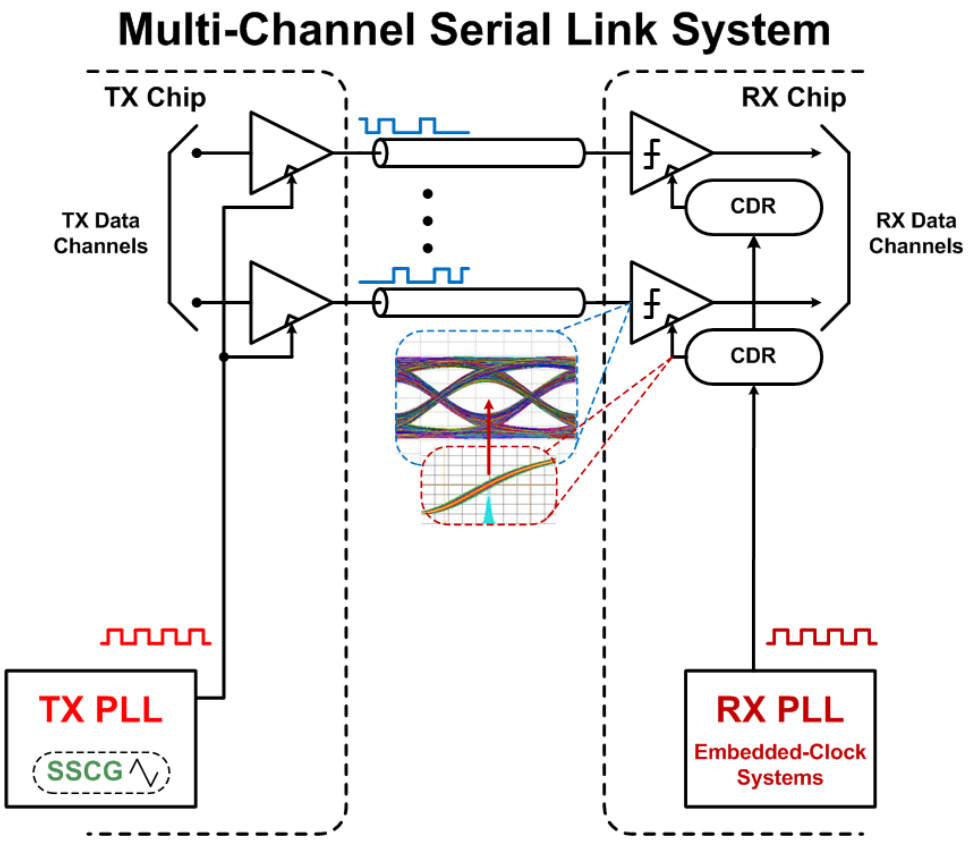
- Per-channel de-skew allows for significant data rate increases
- Sample clock adjusted to center clock on the incoming data eye
- Implementations
  - Delay-Locked Loop and Phase Interpolators
  - Injection-Locked Oscillators
- Phase Acquisition can be
  - BER based – no additional input phase samplers
  - Phase detector based implemented with additional input phase samplers periodically powered on

Forward Clock I/O Circuits



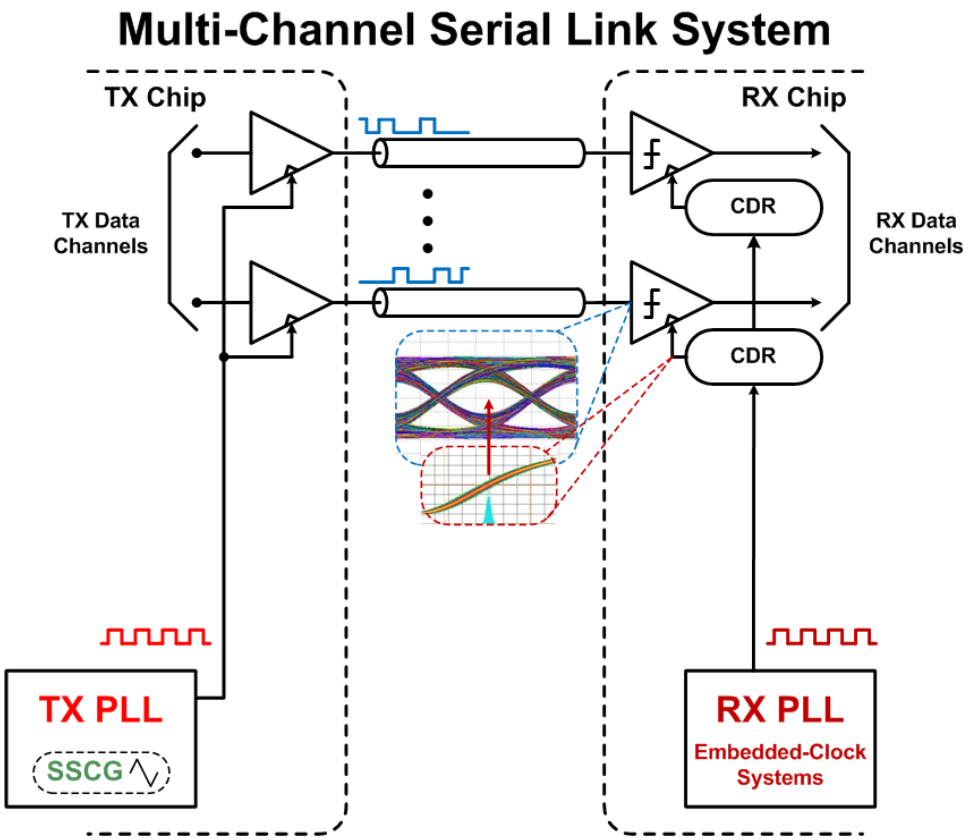
- TX PLL
- TX Clock Distribution
- Replica TX Clock Driver
- Channel
- Forward Clock Amplifier
- RX Clock Distribution
- De-Skew Circuit
  - DLL/PI
  - Injection-Locked Oscillator

Embedded Clock I/O Architecture



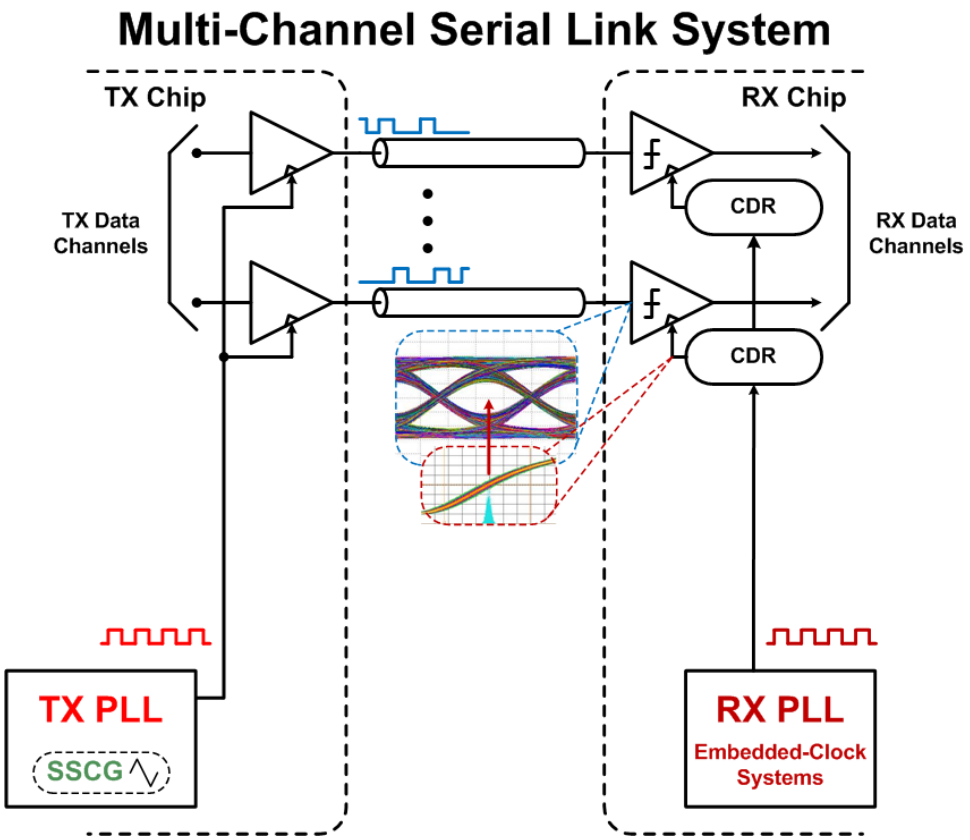
- Can be used in mesochronous or plesiochronous systems
- Clock frequency and optimum phase position are extracted from incoming data stream
- Phase detection continuously running
- CDR Implementations
  - Per-channel PLL-based
  - Dual-loop w/ Global PLL &
    - Local DLL/PI
    - Local Phase-Rotator PLLs

Embedded Clock I/O Limitations



- Jitter tracking limited by CDR bandwidth
  - Technology scaling allows CDRs with higher bandwidths which can achieve higher frequency jitter tracking
- Generally more hardware than forward clock implementations
  - Extra input phase samplers

Embedded Clock I/O Circuits



- TX PLL
- TX Clock Distribution
- CDR
  - Per-channel PLL-based
  - Dual-loop w/ Global PLL &
    - Local DLL/PI
    - Local Phase-Rotator PLLs
    - Global PLL requires RX clock distribution to individual channels

Next Time

- PLL