ECEN689: Special Topics in High-Speed Links Circuits and Systems Spring 2010

Lecture 24: Jitter Budget & Stateye

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Announcements

- HW6 due now
- Exam 2 will be April 30
- Reading
  - Stateye Theory Paper

Agenda

- System Jitter Budget Example
- Stateye Demo
- Project Overview

System Jitter Budget

- For a system to achieve a minimum BER performance

$$UI \geq DJ_{\delta\delta}(sys) + Q_{BER}\sigma_{RMS}(sys)$$

- The convolution of the individual deterministic jitter components is approximated by linear addition of the terms

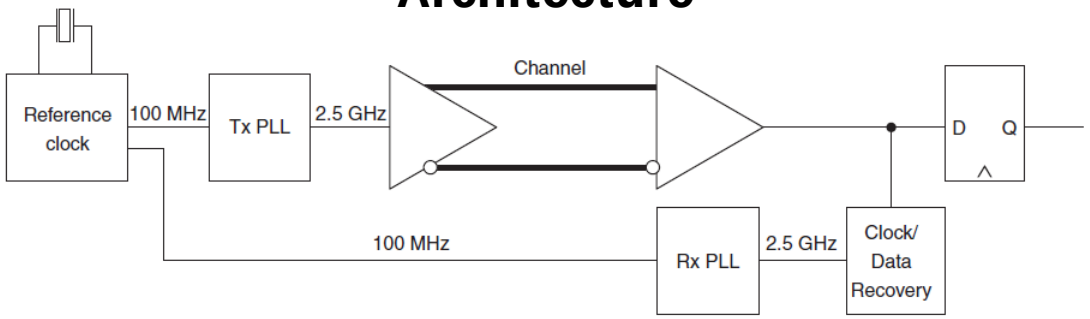
$$DJ_{\delta\delta}(sys) = \sum_i DJ_{\delta\delta}(i)$$

- The convolution of the individual random jitter components results in a root-sum-of-squares system rms value

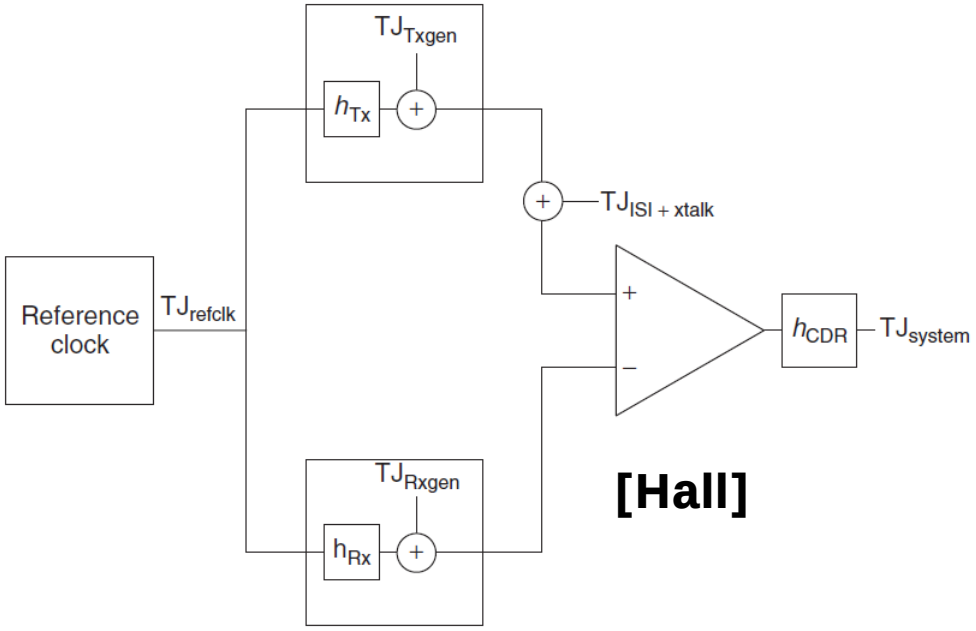
$$\sigma_{RMS}(sys) = \sqrt{\sum_i \sigma_{RMS}^2(i)}$$

Jitter Budget Example – PCI Express System

Architecture



Jitter Model



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Jitter Budget Example – PCI Express System

$$DJ_{\delta\delta}(sys) = DJ_{\delta\delta}(TX) + DJ_{\delta\delta}(channel) + DJ_{\delta\delta}(RX) + DJ_{\delta\delta}(clock)$$

$$\sigma_{RMS}(sys) = \sqrt{\sigma^2_{RMS}(TX) + \sigma^2_{RMS}(channel) + \sigma^2_{RMS}(RX) + \sigma^2_{RMS}(clock)}$$

TABLE 13-2. PCI Express 2.5-Gb/s Jitter Budget at 10^{-12} BER

Component	Term	σ_{RJ} (ps)	$DJ_{\delta\delta}$ (ps)	TJ (ps)
Reference clock	TJ_{clock}	4.7	41.9	108
Transmitter	TJ_{TX}	2.8	60.6	100
Channel	$TJ_{channel}$	0	90	90
Receiver	TJ_{Rx}	2.8	120.6	147
Linear TJ				458
RSS TJ	6.15 * 14.069 =	86.5	313.1	399.6

TABLE 13-1. Q_{BER} as a Function of the Bit Error Rate

BER	Q_{BER}	BER	Q_{BER}	BER	Q_{BER}
1×10^{-3}	6.180	1×10^{-10}	12.723	1×10^{-17}	16.987
1×10^{-4}	7.438	1×10^{-11}	13.412	1×10^{-18}	17.514
1×10^{-5}	8.530	1×10^{-12}	14.069	1×10^{-19}	18.026
1×10^{-6}	9.507	1×10^{-13}	14.698	1×10^{-20}	18.524
1×10^{-7}	10.399	1×10^{-14}	15.301	1×10^{-21}	19.010
1×10^{-8}	11.224	1×10^{-15}	15.882	1×10^{-22}	19.484
1×10^{-9}	11.996	1×10^{-16}	16.444	7.7×10^{-24}	20.000

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Stateye Overview

Project Overview

Next Time

- Timing Circuits