# ECEN689: Special Topics in High-Speed Links Circuits and Systems
# Spring 2012

## Lecture 1: Introduction


Sam Palermo

Analog & Mixed-Signal Center

Texas A&M University

# Class Topics

- System and design issues relevant to high-speed electrical (and optical) signaling
- Channel properties
  - Modeling, measurements, communication techniques
- High-Speed link circuits
  - Drivers, receivers, equalizers, timing systems
- Link system design
  - Modeling and performance metrics
- Link system examples

# Administrative

- Instructor:
  - Sam Palermo
  - 315E WERC Bldg., 845-4114, spalermo@ece.tamu.edu
  - Office hours: TR 9:00am-10:30pm
- Lectures: MW 5:45pm-7:00am, ZACH 223A
- Lab: R 4:00pm-5:50pm, ZACH 203
  - Lab begins second week
- Class web page
  - http://www.ece.tamu.edu/~spalermo/ecen689.html

# Class Material

- Textbook: Class Notes and Technical Papers
- Key References
  - *Digital Systems Engineering*, W. Dally and J. Poulton, Cambridge University Press, 1998.
  - *Advanced Signal Integrity for High-Speed Digital Designs,* S. H. Hall and H. L. Heck, John Wiley & Sons, 2009.
  - *High-Speed Digital Design: A Handbook of Black Magic*, H. Johnson & M. Graham, Prentice Hall, 1993.
  - *Design of Integrated Circuits for Optical Communications*, B. Razavi, McGraw-Hill, 2003.
- Class notes
  - Will hand out hard copies in class

# Grading

- Exams (50%)
  - Two midterm exams (25% each)
- Homework & Labs (25%)
  - Labs (Prelab + Report) and homeworks weighted equally
  - Collaboration is allowed, but independent simulations and write-ups
  - Need to setup CADENCE simulation environment
  - Due at beginning of class
  - No late homework will be graded
- Final Project (25%)
  - Groups of 1-2 students
  - Report and PowerPoint presentation required

# Prerequisites

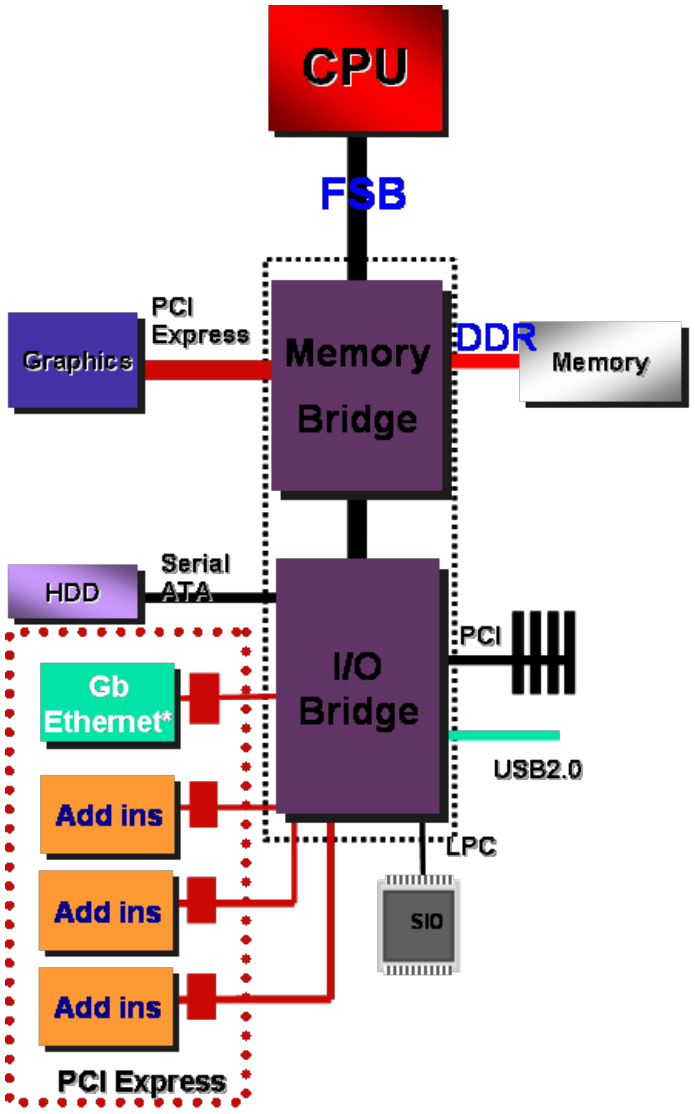
- This is a circuits AND systems class
- Circuits
  - ECEN474 or approval of instructor
  - Basic knowledge of CMOS gates, flops, etc...
  - Circuit simulation experience (HSPICE, Spectre)
- Systems
  - Basic knowledge of s- and z-transforms
  - Basic digital communication knowledge
  - MATLAB experience

# Simulation Tools

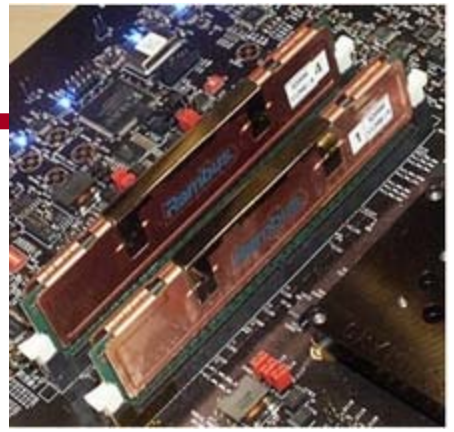
- Matlab
- Stateye (Statistical BER link analysis)
- Cadence
- 90nm CMOS device models
  - Can use other technology models if they are a 90nm or more advanced CMOS node
- Other tools, schematic, layout, etc... are optional

# Desktop Computer I/O Architecture

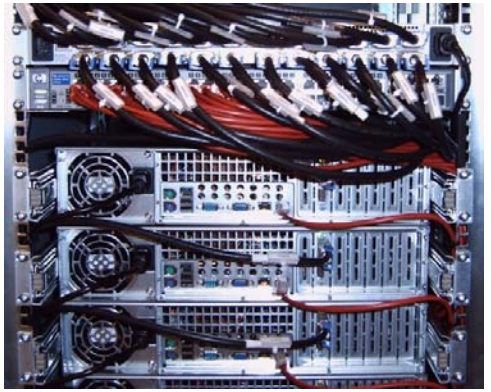
- Many high-speed I/O interfaces
- Key bandwidth bottleneck points are memory (FSB) and graphics interfaces (PCIe)
- Near-term architectures
  - Integrated memory controller with serial I/O (>5Gb/s) to memory
  - Increasing PCIe from 2.5Gb/s (Gen1) to 8Gb/s (Gen3)
- Other serial I/O systems
  - Multi-processor systems
  - Routers



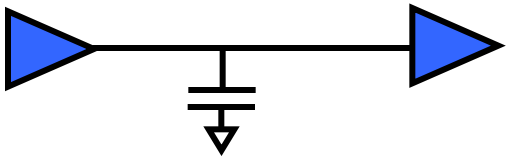
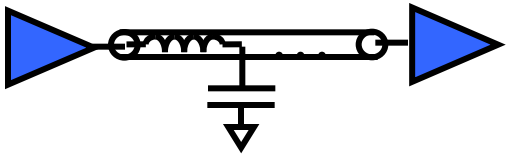
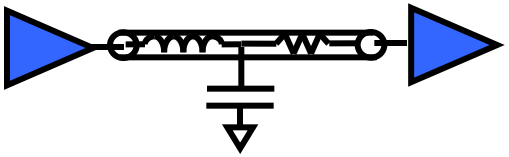
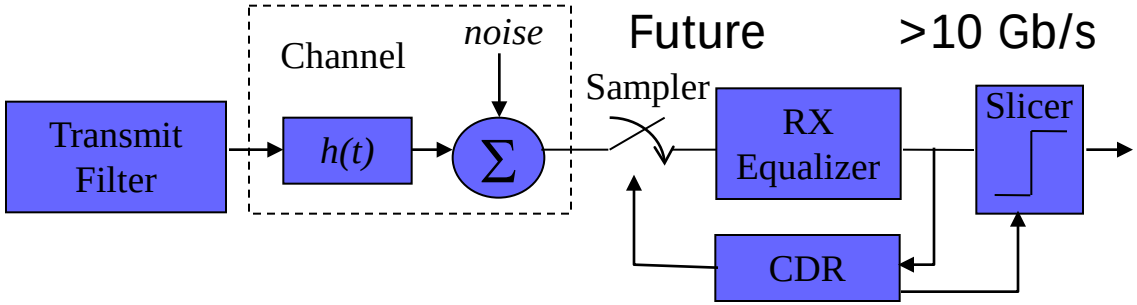
# Serial Link Applications



- Processor-to-memory
  - RDRAM (1.6Gbps), XDR DRAM (7.2Gbps), XDR2 DRAM (12.8Gbps)
- Processor-to-peripheral
  - PCIe (2.5, 5, 8Gbps), Infiniband (10Gbps), USB3 (4.8Gbps)
- Processor-to-processor
  - Intel QPI (6.4Gbps), AMD Hypertransport (6.4Gbps)
- Storage
  - SATA (6Gbps), Fibre Channel (20Gbps)
- Networks
  - LAN: Ethernet (1, 10Gbps)
  - WAN: SONET (2.5, 10, 40Gbps)
  - Backplane Routers: (2.5 – 12.5Gbps)



# Chip-to-Chip Signaling Trends

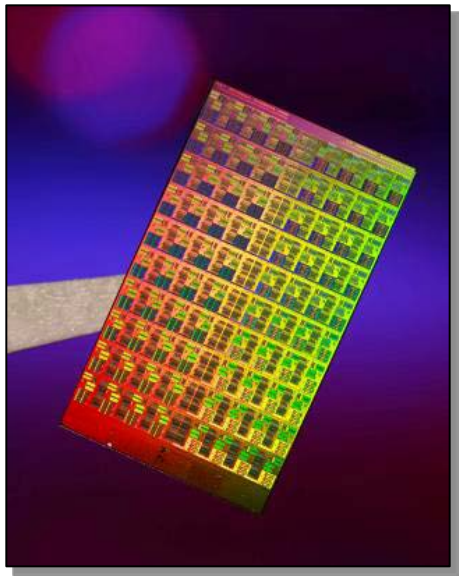
| | Decade | Speeds | Transceiver Features |
|---|---|---|---|
| Lumped capacitance  | 1980's | >10Mb/s | Inverter out, inverter in |
| Transmission line  | 1990's | >100Mb/s | Termination<br>Source-synchronous clk. |
| Lossy transmission line  | 2000's | >1 Gb/s | Pt-to-pt serial streams<br>Pre-emphasis equalization |
|   | Future | >10 Gb/s | Adaptive Equalization,<br>Advanced low power clk.<br>Alternate channel materials |

Slide Courtesy of Frank O'Mahony & Brian Casper, Intel

# Increasing I/O Bandwidth Demand

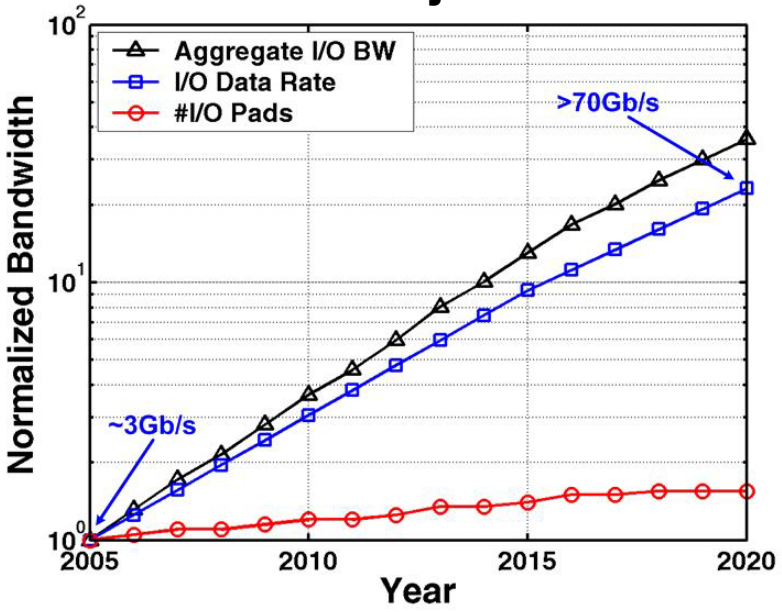
- Single ⇒ Multi ⇒ Many-Core μProcessors
- Tera-scale many-core processors will aggressively drive aggregate I/O rates

Intel Teraflop Research Chip



- 80 processor cores
- On-die mesh interconnect network w/ >2Tb/s aggregate bandwidth
- 100 million transistors
- 275mm$^2$

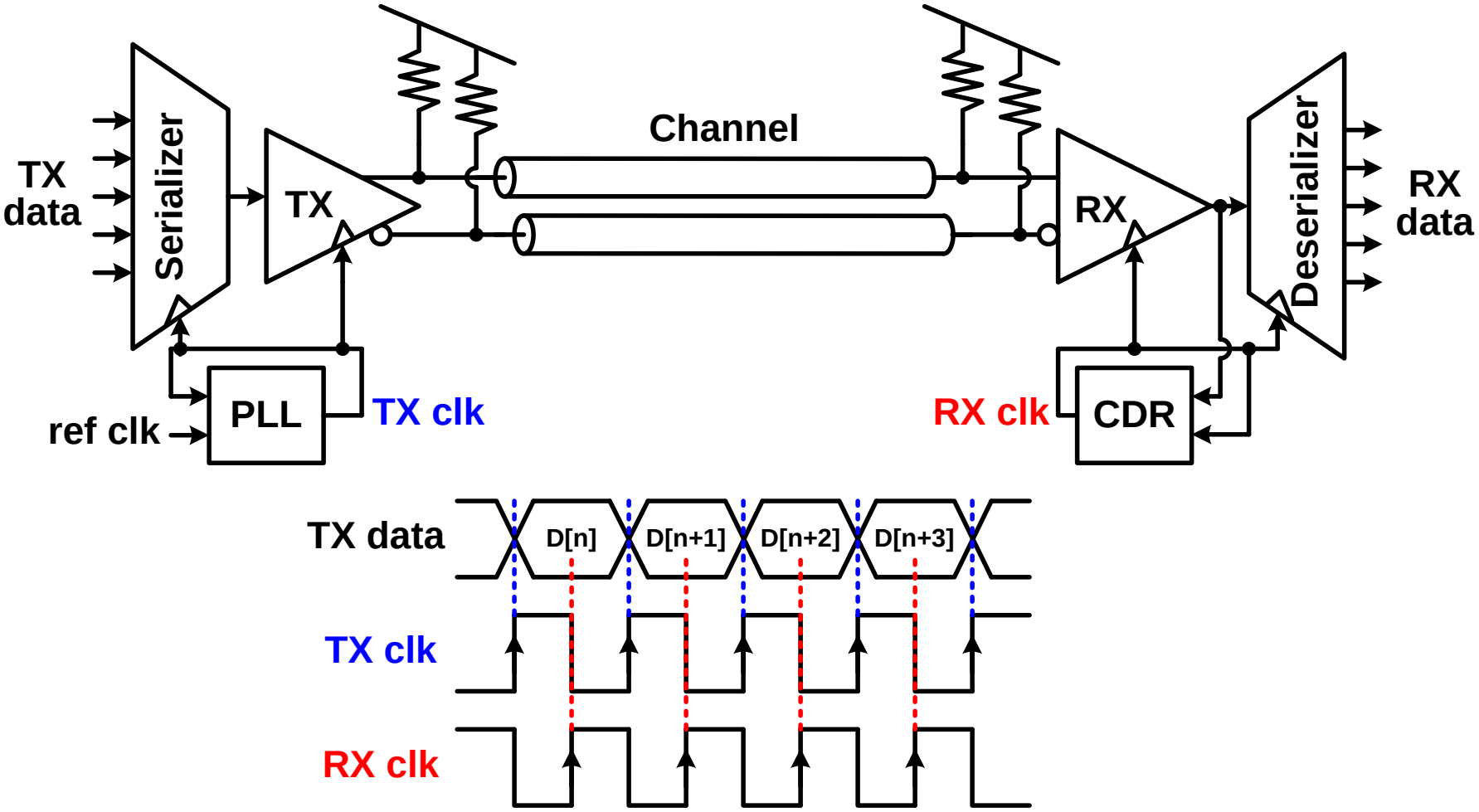
**ITRS Projections***



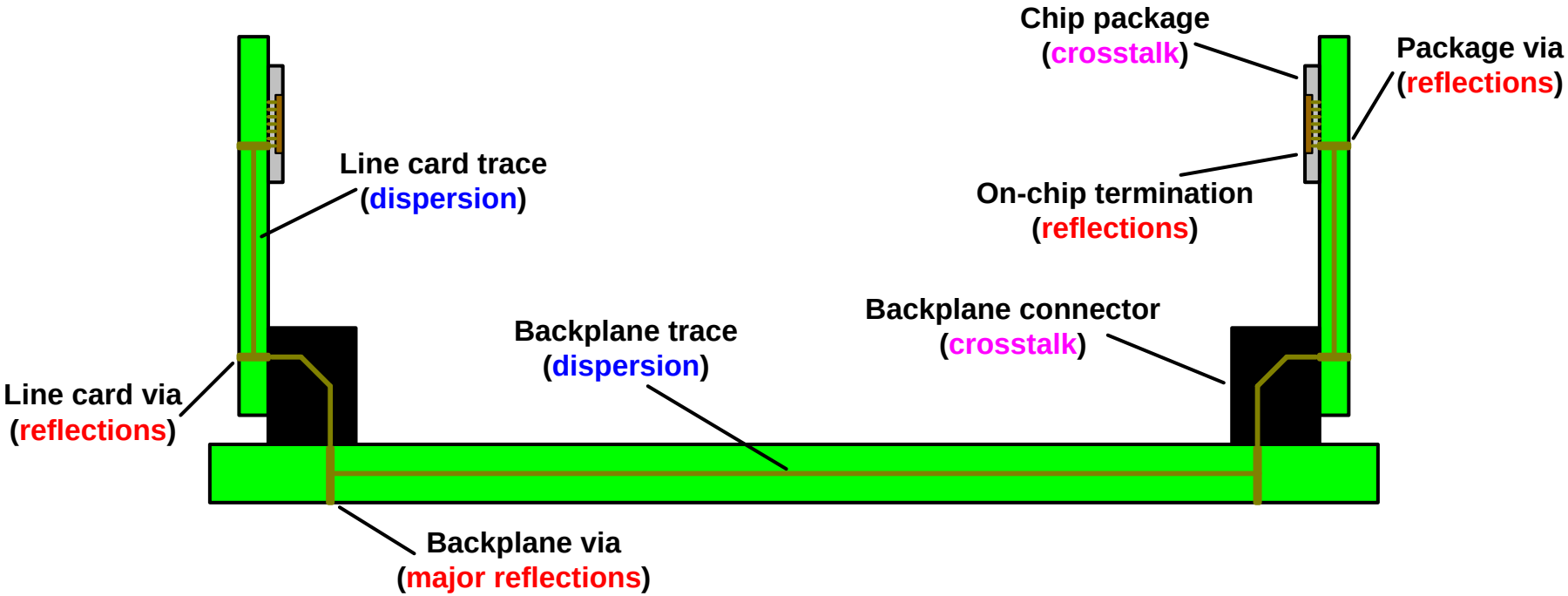

S. Vangal *et al*, "An 80-Tile Sub-100W TeraFLOPS Processor in 65nm CMOS," *JSSC*, 2008.

*2006 International Technology Roadmap for Semiconductors

# High-Speed Electrical Link System

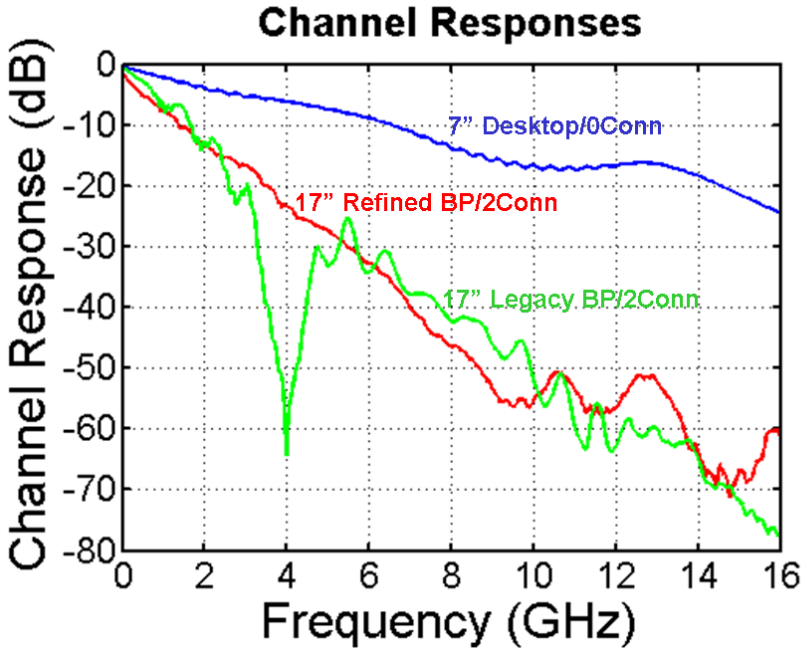


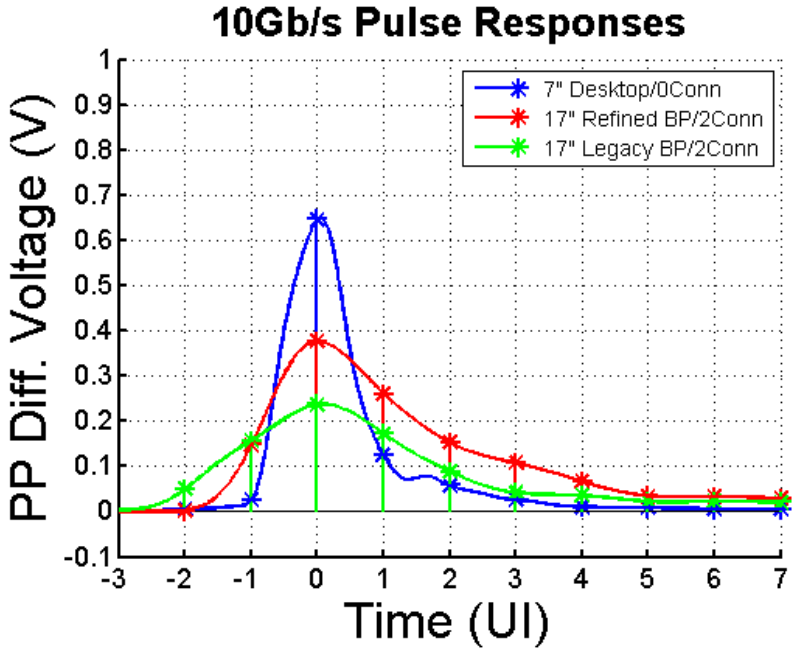
# Electrical Backplane Channel

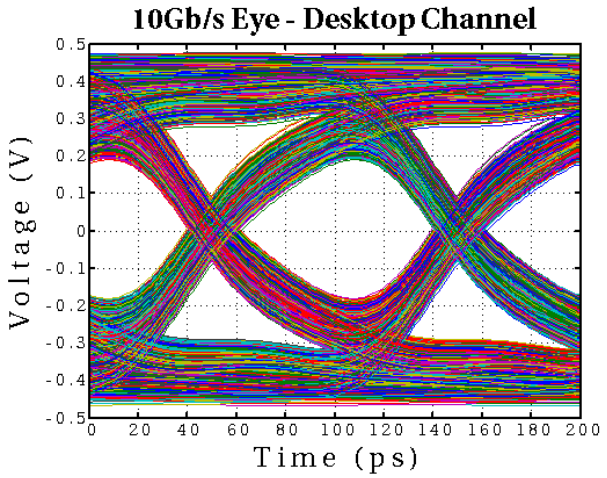


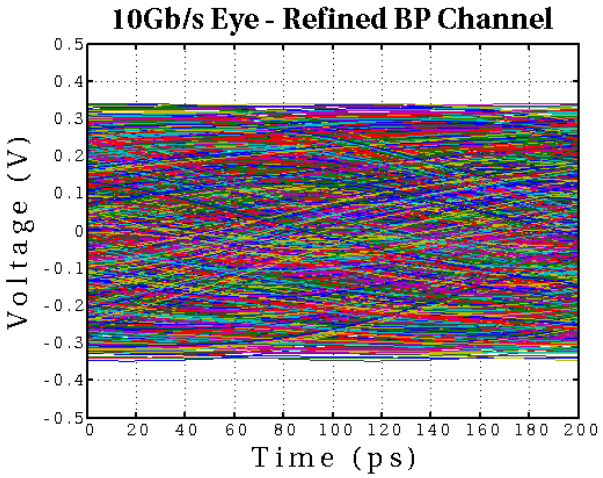

- Frequency dependent loss
  - Dispersion & reflections
- Co-channel interference
  - Far-end (FEXT) & near-end (NEXT) crosstalk

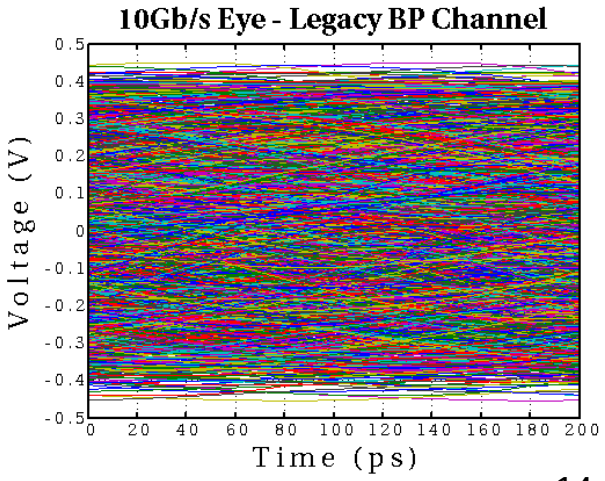
# Channel Performance Impact



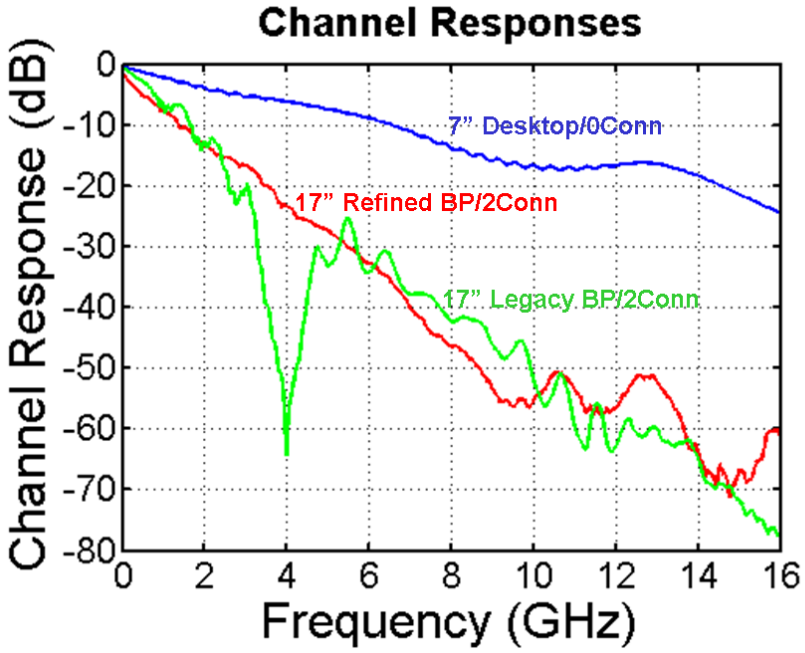



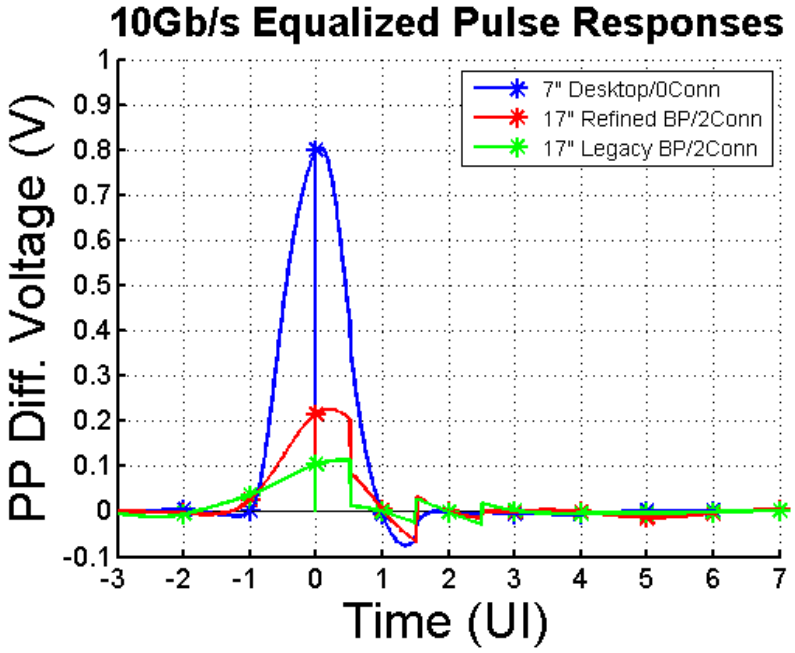



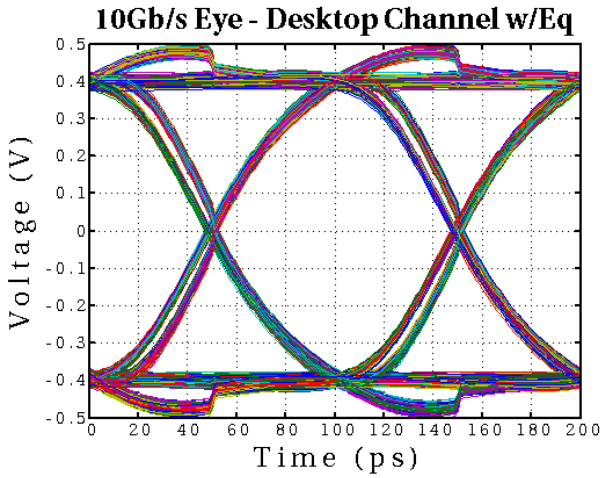



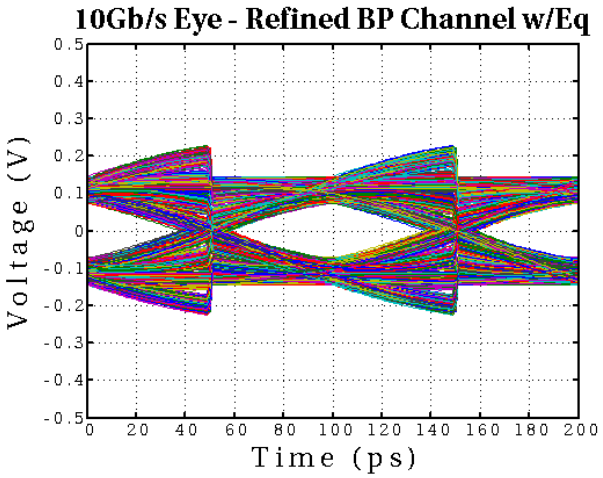



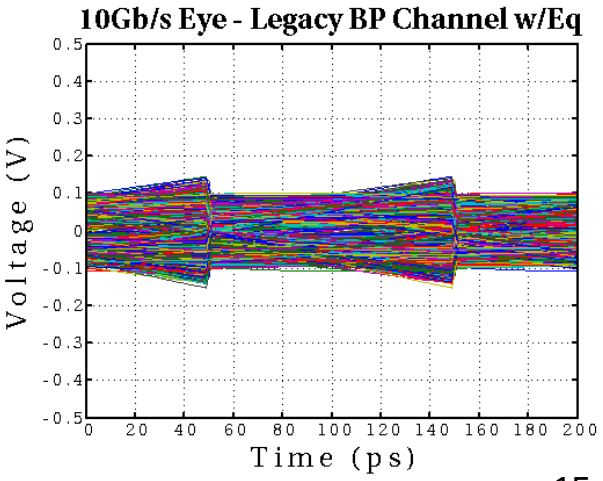
# Channel Performance Impact



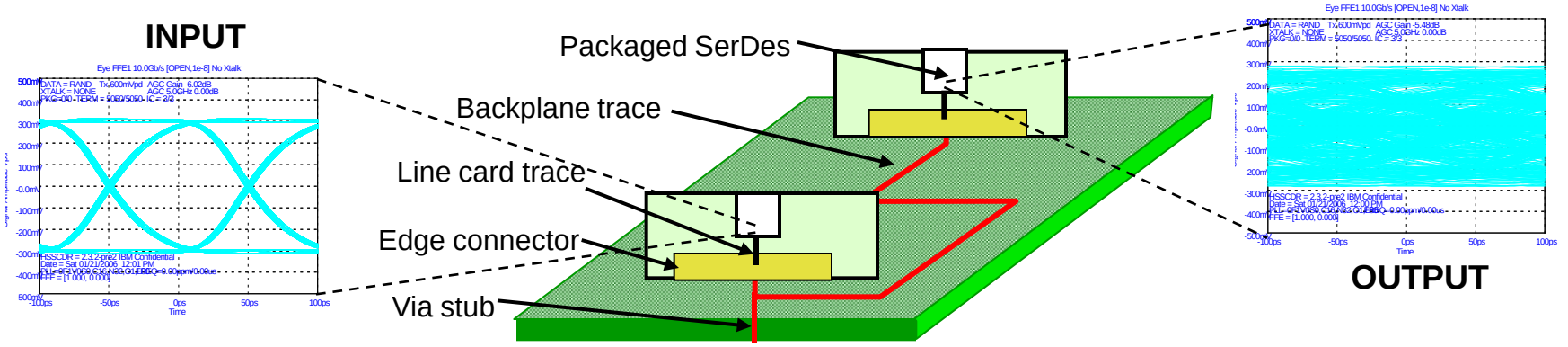
# Backplane Link Example

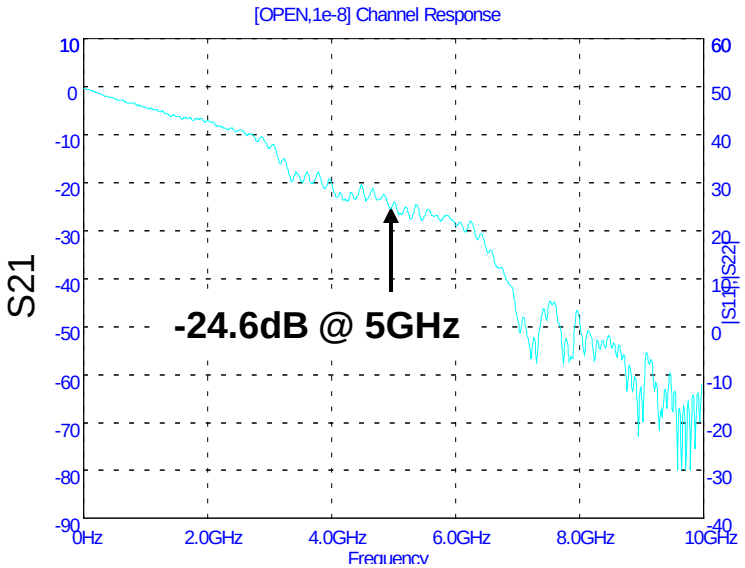
## A 10Gb/s 5-tap DFE / 4-Tap FFE Transceiver in 90nm CMOS Technology

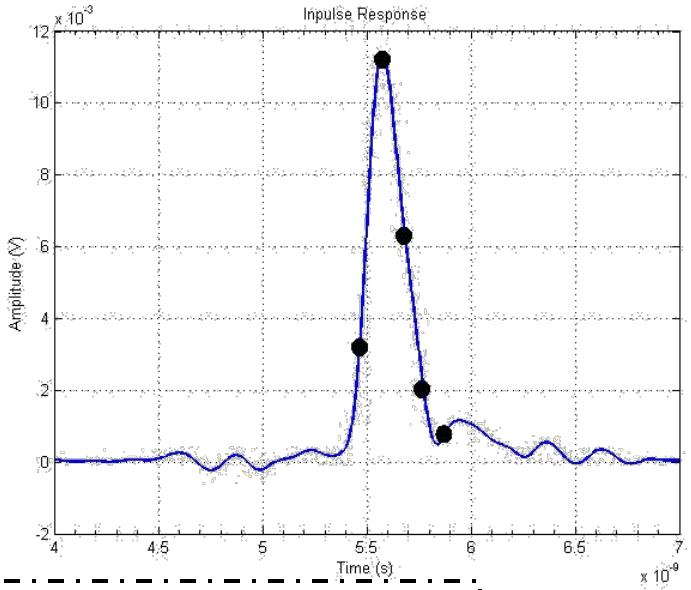
Mounir Meghelli, Sergey Rylov, John Bulzacchelli, Woogeun Rhee, Alexander Rylyakov, Herschel Ainspan, Ben Parker, Michael Beakes, Aichin Chung, Troy Beukema, Petar Pepeljugoski, Lei Shan, Young Kwark, Sudhir Gowda and Dan Friedman

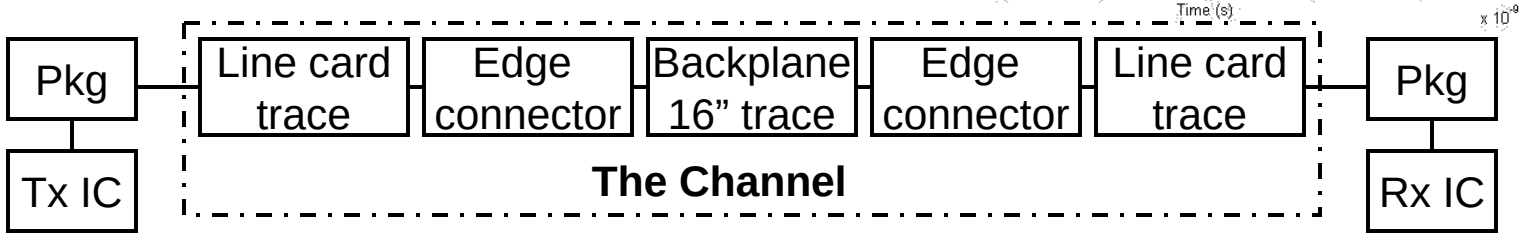
IBM T. J. Watson Research Center, Yorktown Heights, NY

# Transmission Channel Impairments




**[Meghelli (IBM) ISSCC 2006]**

# 10Gb/s SerDes Main Features

- Tx with 1 baud-spaced 4-tap FFE
- Rx with 5-tap adaptive DFE and digital clock recovery
- LC-VCO based PLL for low noise clock generation
- 90nm CMOS technology

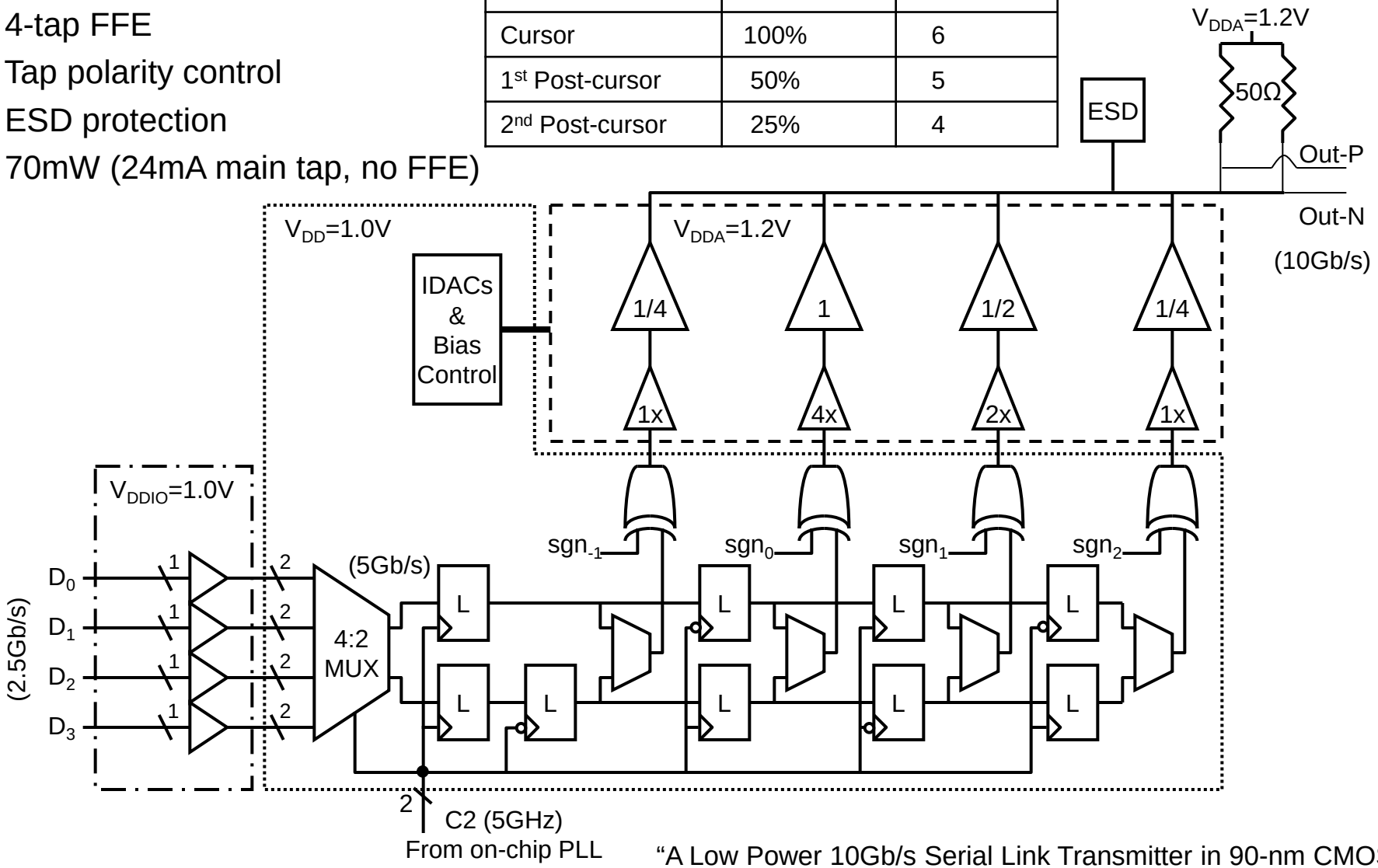
**[Meghelli (IBM) ISSCC 2006]**

# Transmitter Architecture

**Key Features:**

- Half-rate CML design
- 4-tap FFE
- Tap polarity control
- ESD protection
- 70mW (24mA main tap, no FFE)

| FFE Taps | Full Scale | DAC bits |
|---|---|---|
| Pre-cursor | 25% | 4 |
| Cursor | 100% | 6 |
| 1st Post-cursor | 50% | 5 |
| 2nd Post-cursor | 25% | 4 |

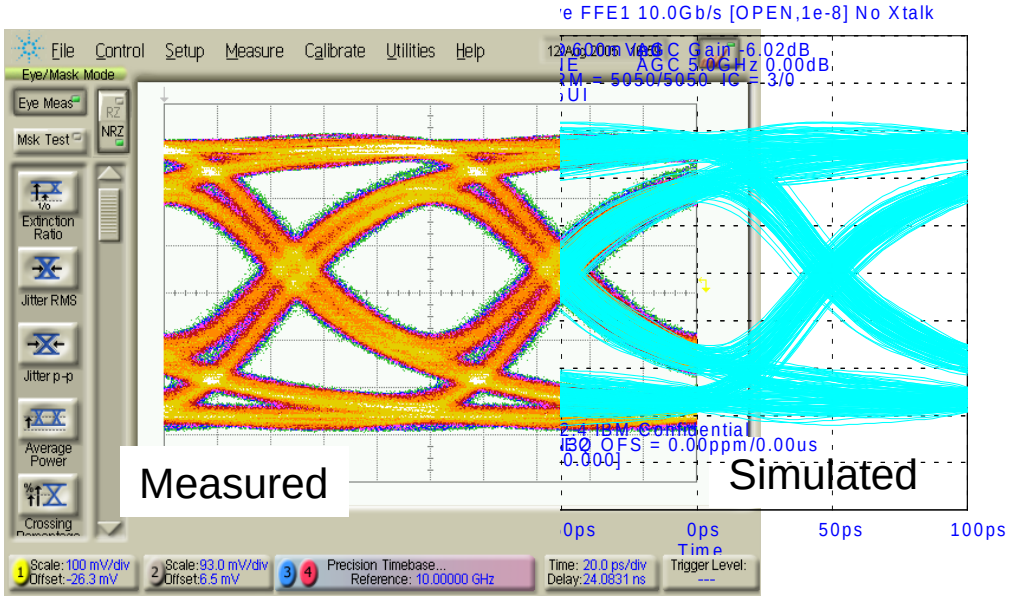



**[Meghelli (IBM) ISSCC 2006]**

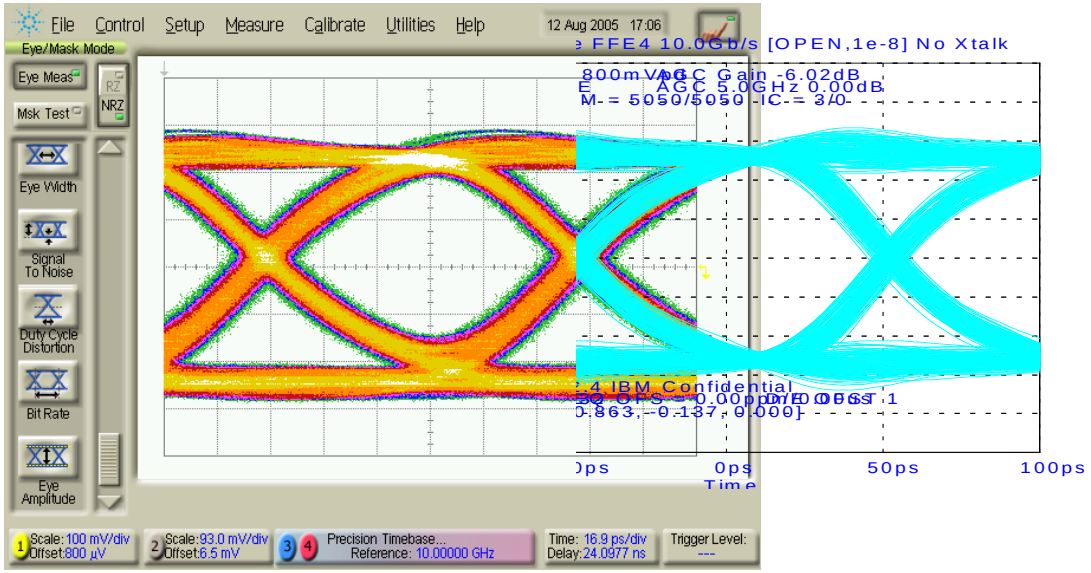
"A Low Power 10Gb/s Serial Link Transmitter in 90-nm CMOS"
A. Rylyakov et al., CSICS 2005

# Tx Output Eye Diagram @ 10Gb/s

**No FFE, 24mA on main tap**

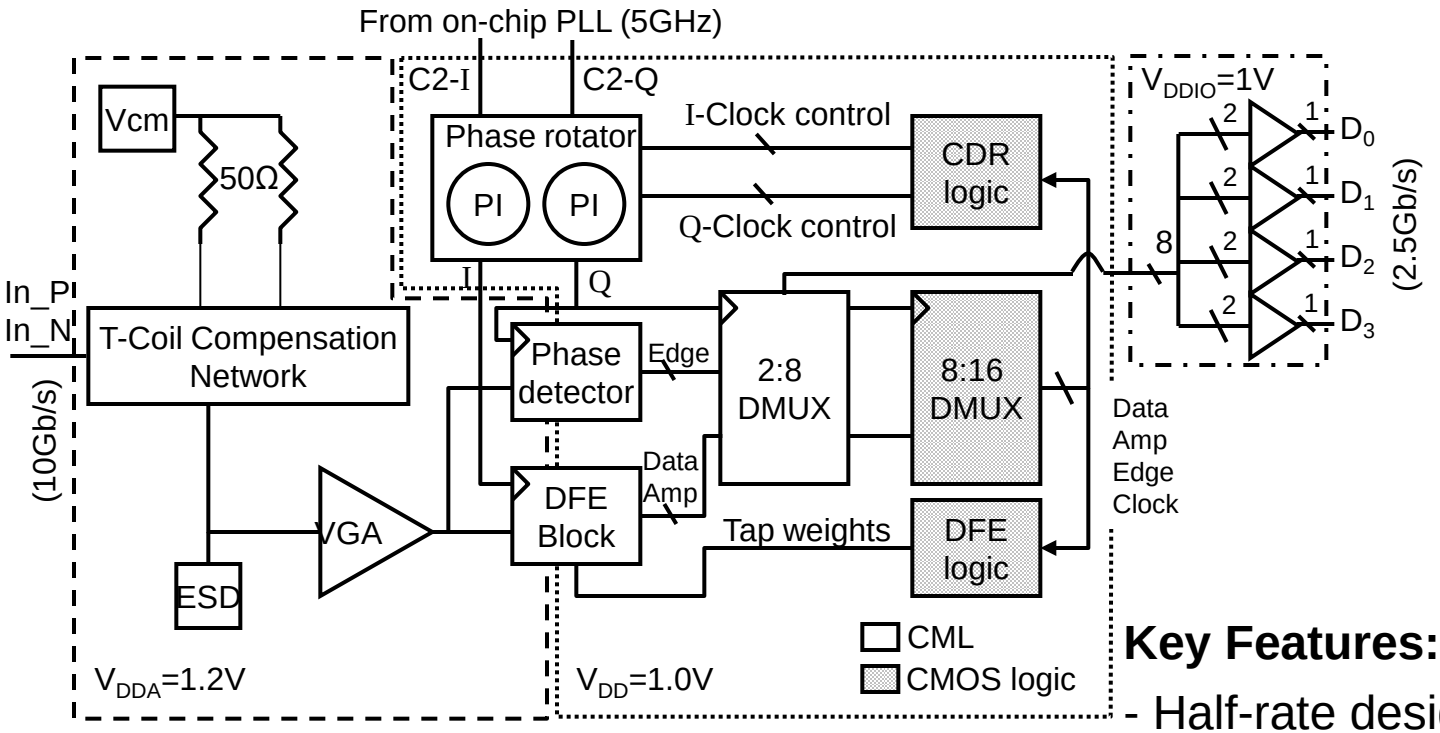



**FFE 4=[0, 85%, -15%, 0, 0]**




**[Meghelli (IBM) ISSCC 2006]**

# Receiver Architecture

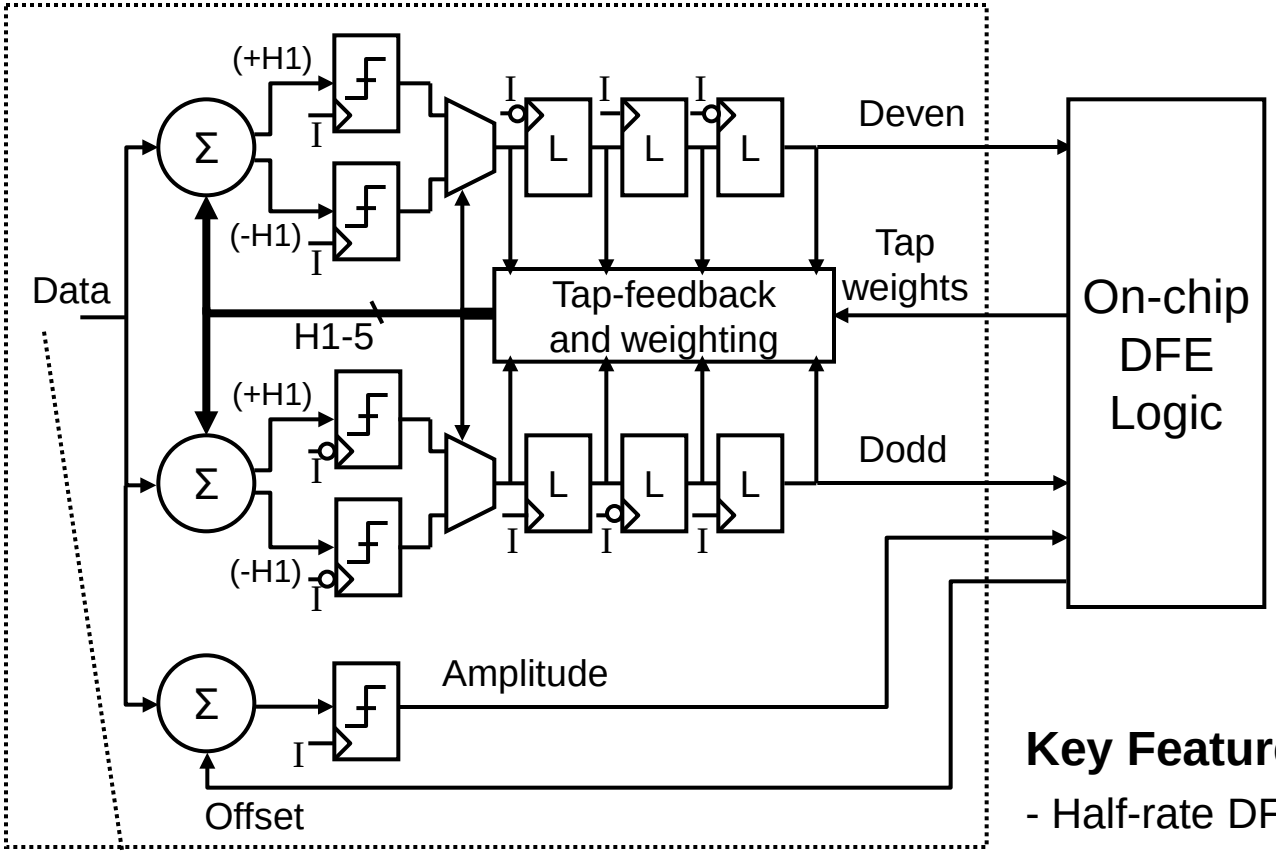


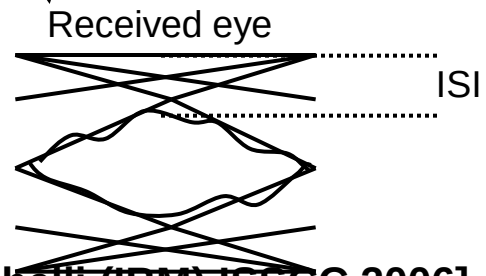

**Key Features:**

- Half-rate design
- 5-tap continuously adaptive DFE
- Variable gain amplifier
- Digital CDR
- ESD protection (HBM & CDM)
- 130mW (with DFE and CDR logic)

**[Meghelli (IBM) ISSCC 2006]**

# DFE Approach



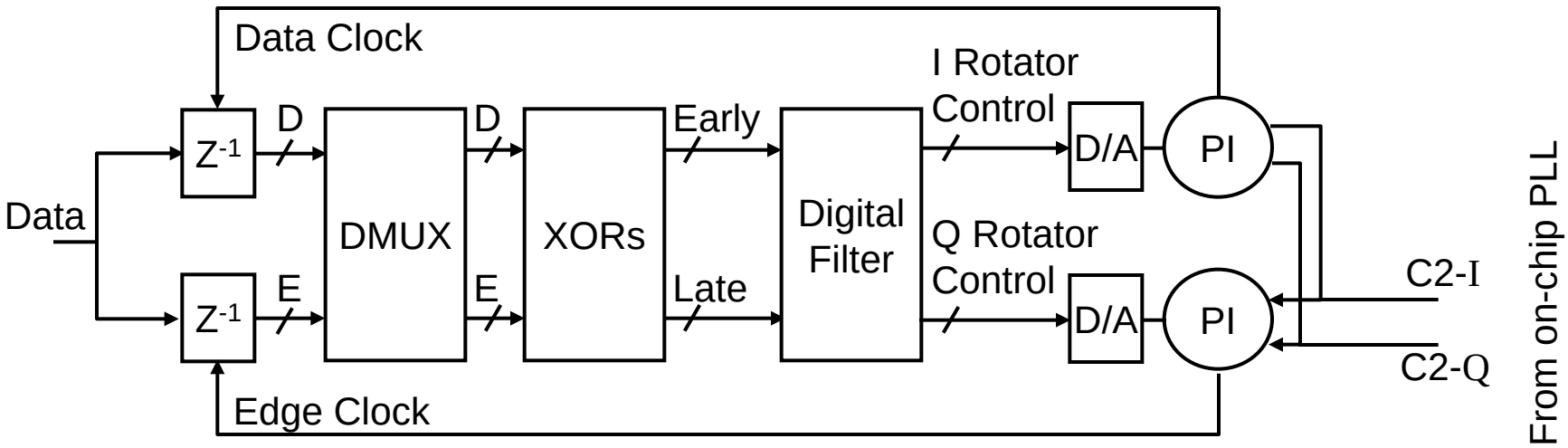

| DFE Taps | Resolution |
|---|---|
| H1 | 6 bits |
| H2 | 5 bits |
| H3, H4, H5 | 4 bits |

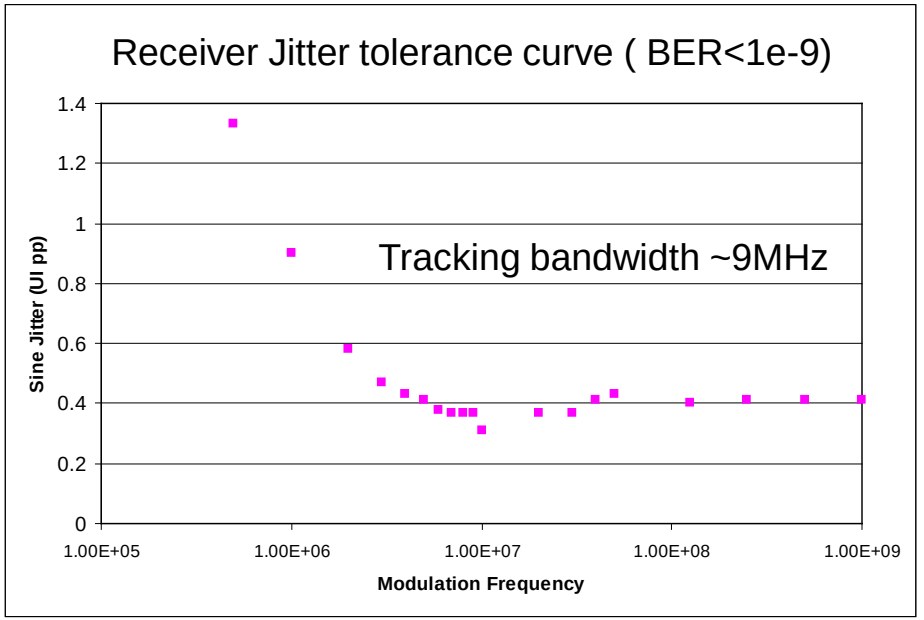
**Key Features:**

- Half-rate DFE with H1 speculation and dynamic H2-H5 feedback allows 2UI for settling
- DFE algorithm maximizes vertical eye opening at the data slicing instant
- Offset adjustment at all the slicer inputs

**[Meghelli (IBM) ISSCC 2006]**

# CDR Loop



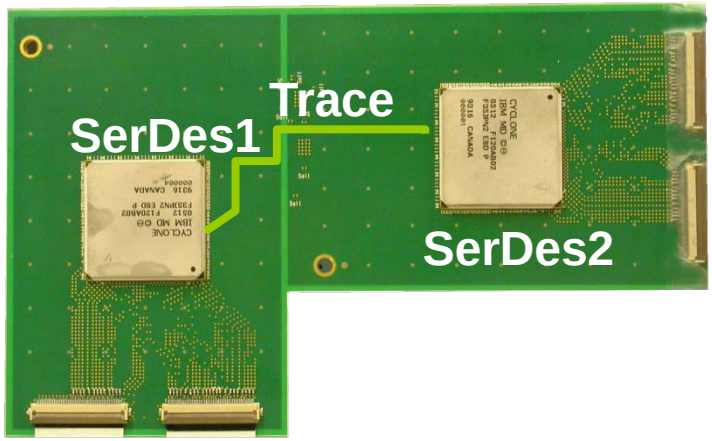



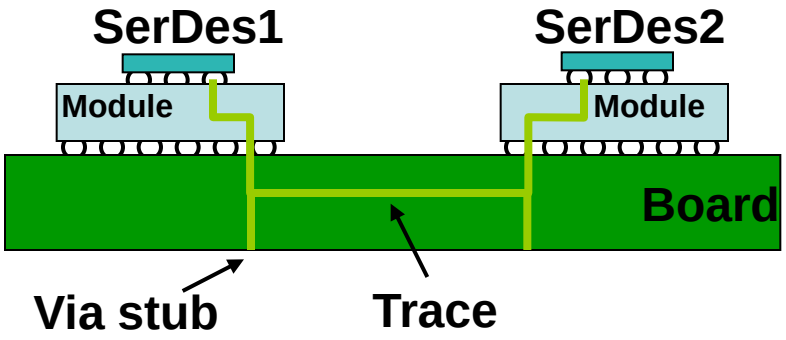

**Key Features:**

- Fully digital loop
- Can handle up to +/- 4000ppm frequency offset
- Independent I,Q control

**[Meghelli (IBM) ISSCC 2006]**

# Chip-to-Chip Link Experiments



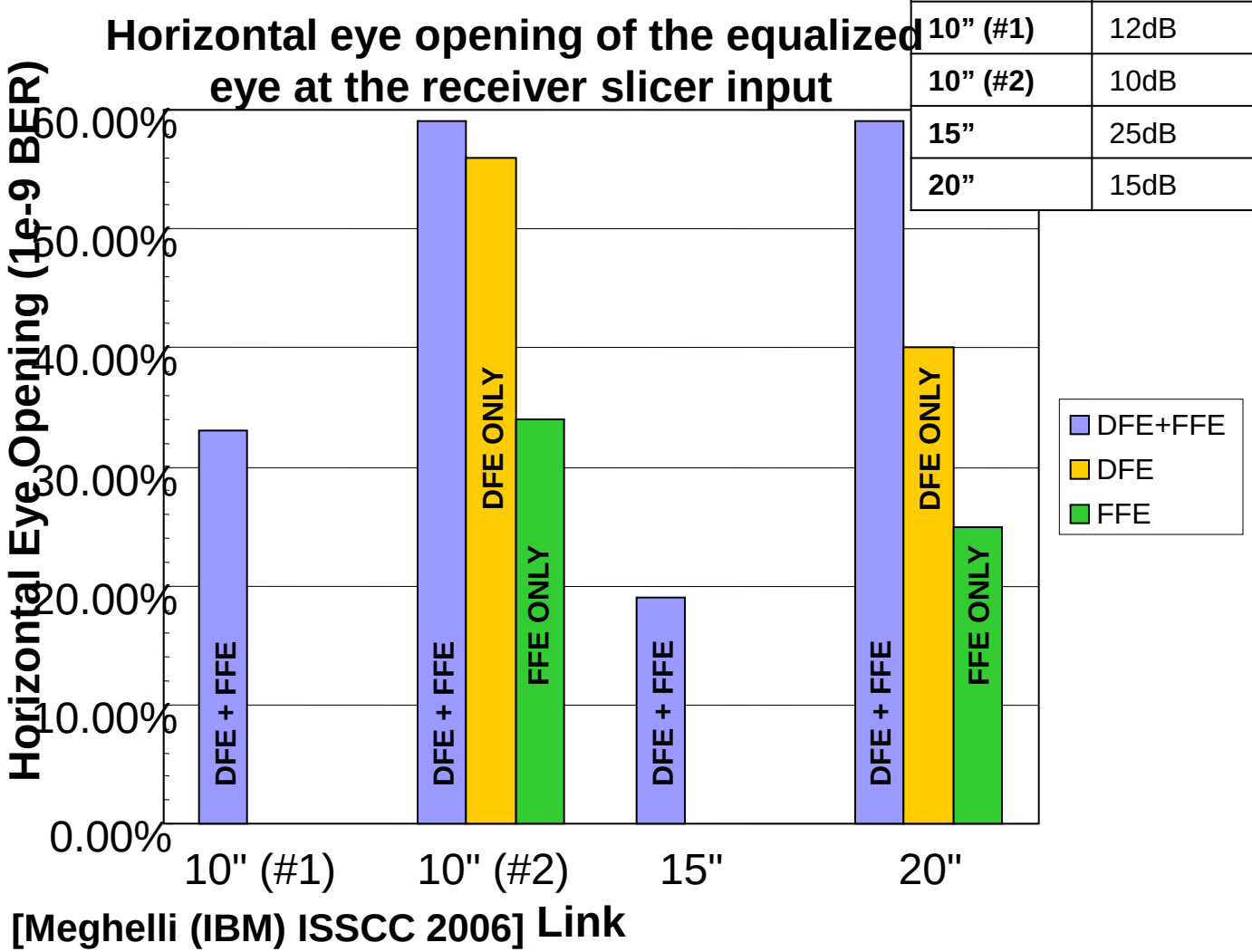




| Trace Length | 5GHz losses (Tx module + board trace + Rx module) | Number of vias 3.8mm via stub / 1.8mm via stub / 1.8mm via through |
|---|---|---|
| **10” (#1)** | 12dB | 2 / 0 / 0 |
| **10” (#2)** | 10dB | 0 / 2 / 0 |
| **15”** | 25dB | 4 / 2 / 0 |
| **20”** | 15dB | 0 / 0 / 2 |

**[Meghelli (IBM) ISSCC 2006]**

# Chip-to-Chip Measurement Results

| Trace Length | 5GHz losses (Tx module + board trace + Rx module) | Number of vias 3.8mm via stub / 1.8mm via stub / 1.8mm via through |
|---|---|---|
| 10” (#1) | 12dB | 2 / 0 / 0 |
| 10” (#2) | 10dB | 0 / 2 / 0 |
| 15” | 25dB | 4 / 2 / 0 |
| 20” | 15dB | 0 / 0 / 2 |




[Meghelli (IBM) ISSCC 2006]

# Preliminary Schedule

| Topic | | Week |
|---|---|---|
| I. | Channels | Week 1-7 |
| II. | Communication Techniques | |
| III. | Equalizers | |
| IV. | Transmitter/Receiver Circuits | |
| | **First Exam** | **March 7** |
| V. | Equalizer Circuits | Week 8-14 |
| VI. | Clocking Circuits | |
| VII. | Clocking Systems | |
| VIII. | Link Modeling | |
| IX. | Link Examples | |
| | **Second Exam** | **April 25** |
| | **Project Report Due** | **May 1** |
| | **Project Presentations** | **May 9** |

- Dates may change with reasonable notice

# Next Time

- Channels
  - Components
    - Chip packages, PCBs, Wires, Connectors
  - Modeling
    - Wires, Transmission Lines