ECEN689: Special Topics in High-Speed Links Circuits and Systems Spring 2010

Lecture 19: RX DFE Equalization

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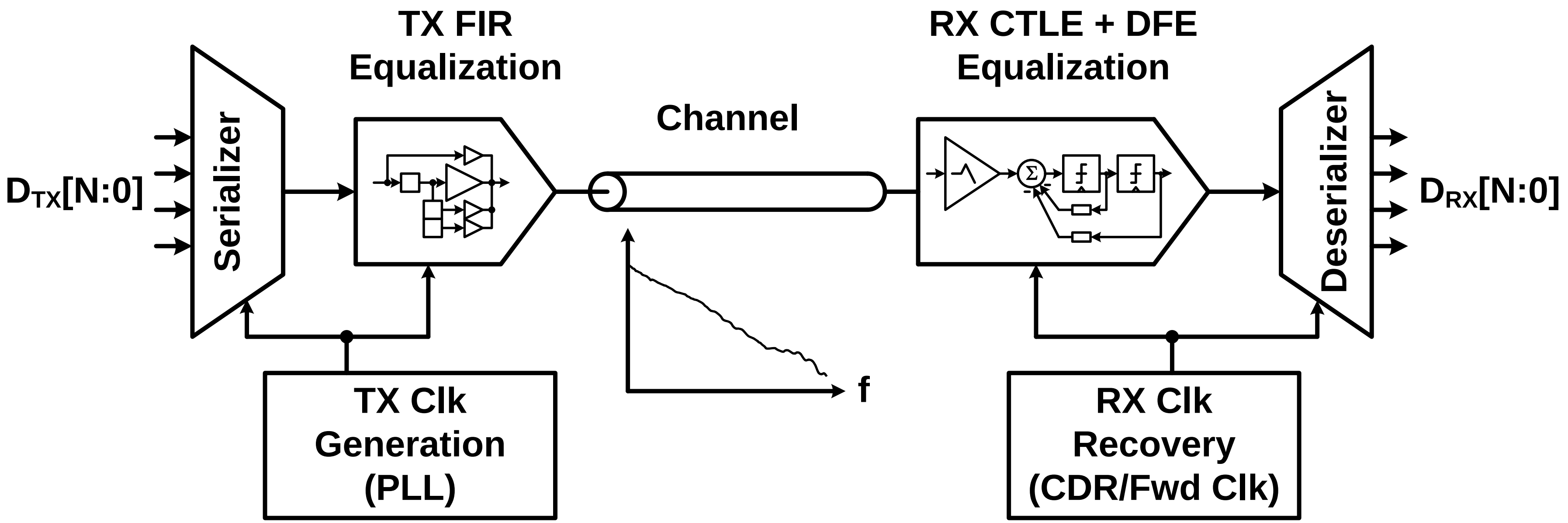
Announcements

- HW5 now due Friday (in class)
  - Any issues?
- Reading
  - Will post some DFE papers

Agenda

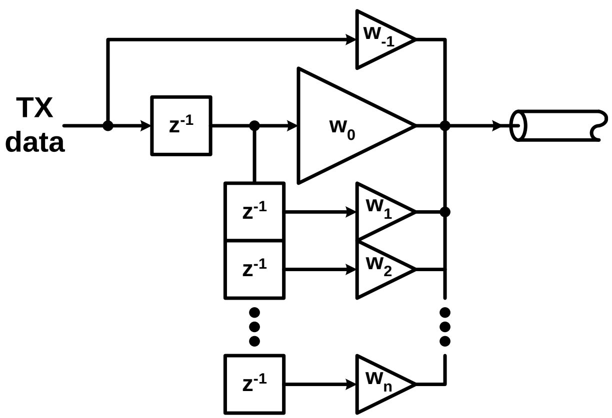
- RX DFE Equalization
- Future Approaches

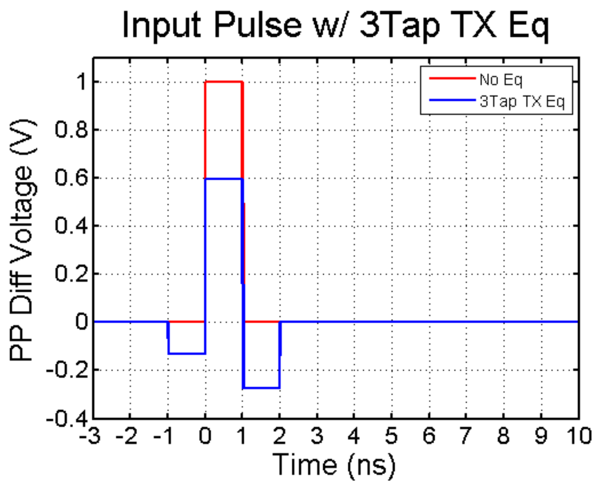
Link with Equalization

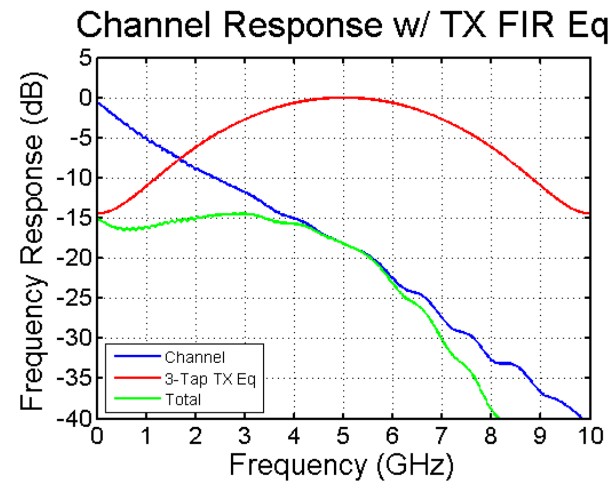


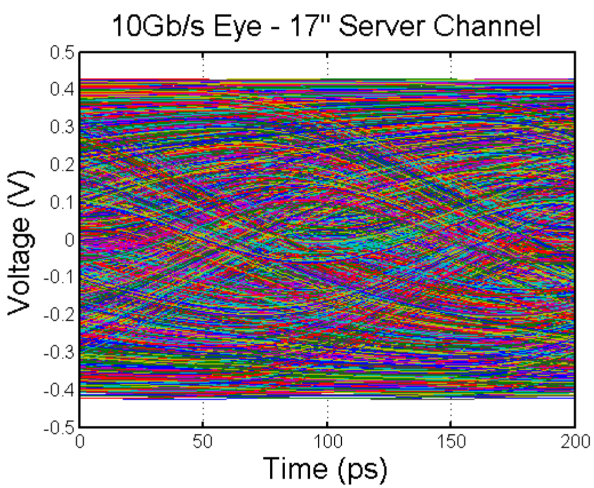
TX FIR Equalization

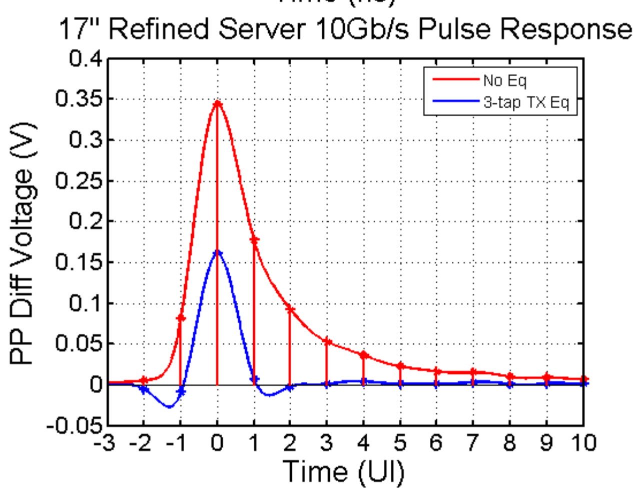
- TX FIR filter pre-distorts transmitted pulse in order to invert channel distortion at the cost of attenuated transmit signal (de-emphasis)

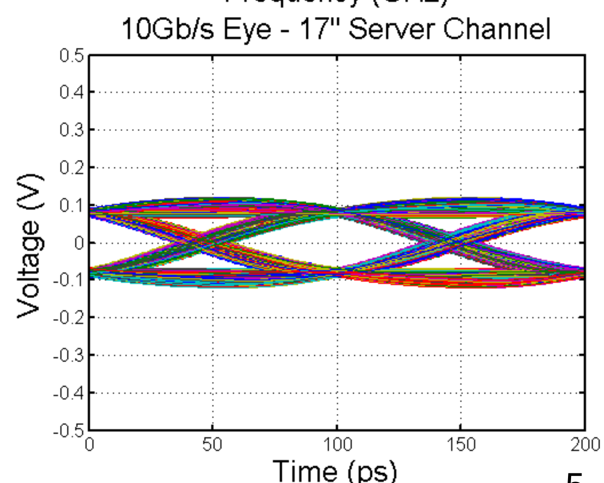






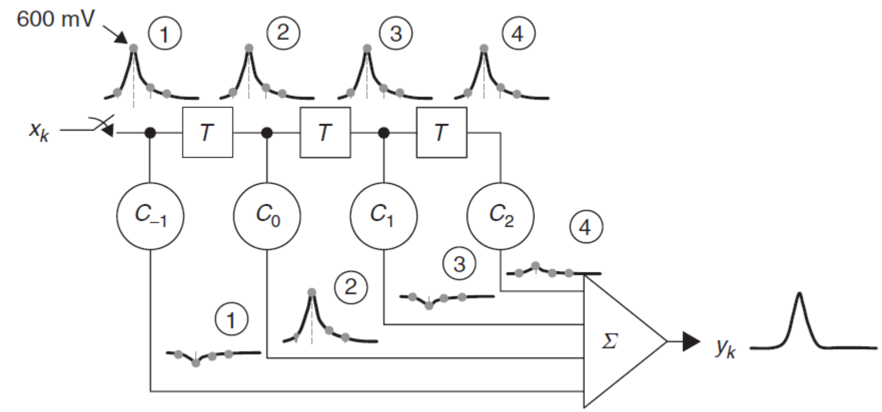


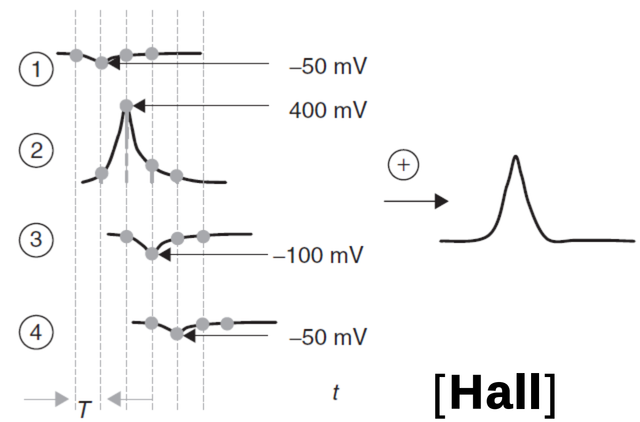




RX FIR Equalization

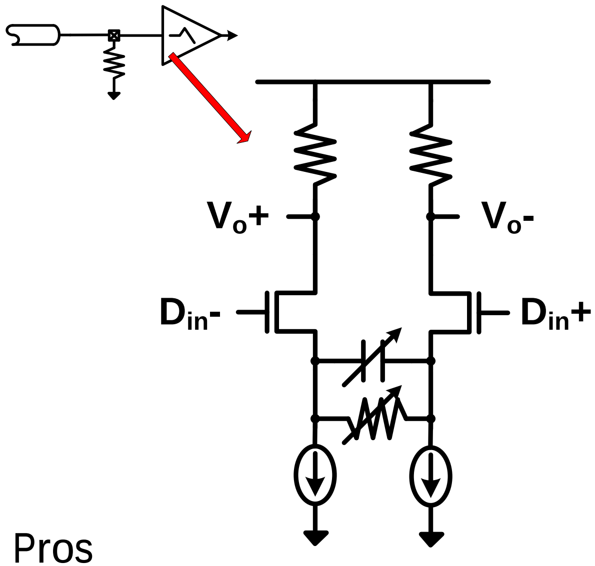
- Delay analog input signal and multiply by equalization coefficients
- Pros
  - With sufficient dynamic range, can amplify high frequency content (rather than attenuate low frequencies)
  - Can cancel ISI in pre-cursor and beyond filter span
  - Filter tap coefficients can be adaptively tuned without any back-channel
- Cons
  - Amplifies noise/crosstalk
  - Implementation of analog delays
  - Tap precision

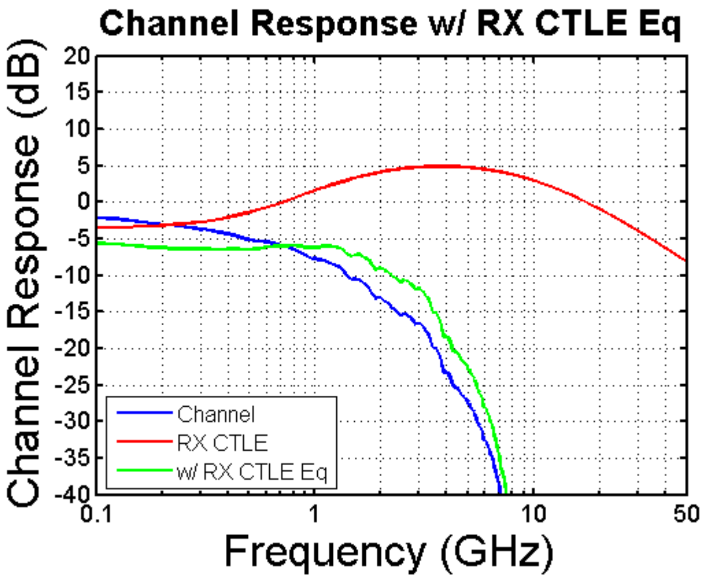




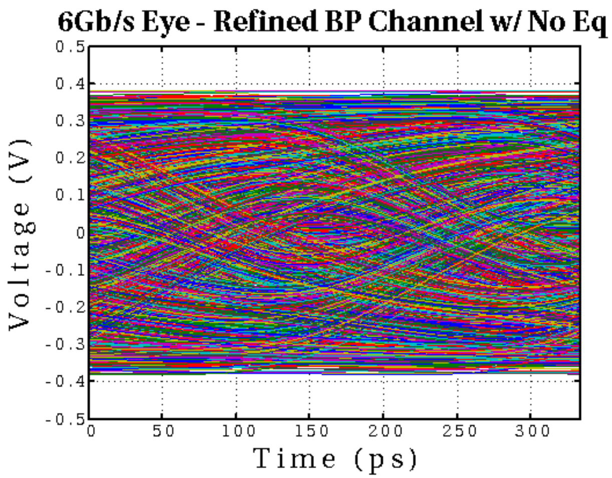
[Hall]

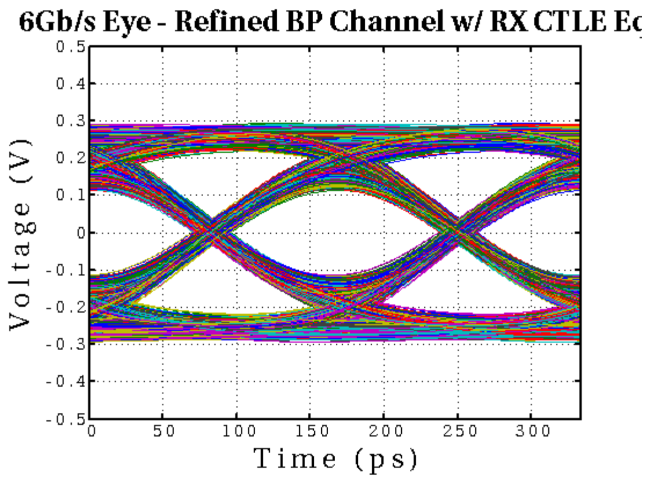
RX CTLE Equalization





- Pros
  - Provides gain and equalization with low power and area overhead
  - Can cancel both pre-cursor and long-tail ISI
- Cons
  - Generally limited to 1st order compensation
  - Amplifies noise/crosstalk
  - PVT sensitivity
  - Can be hard to tune

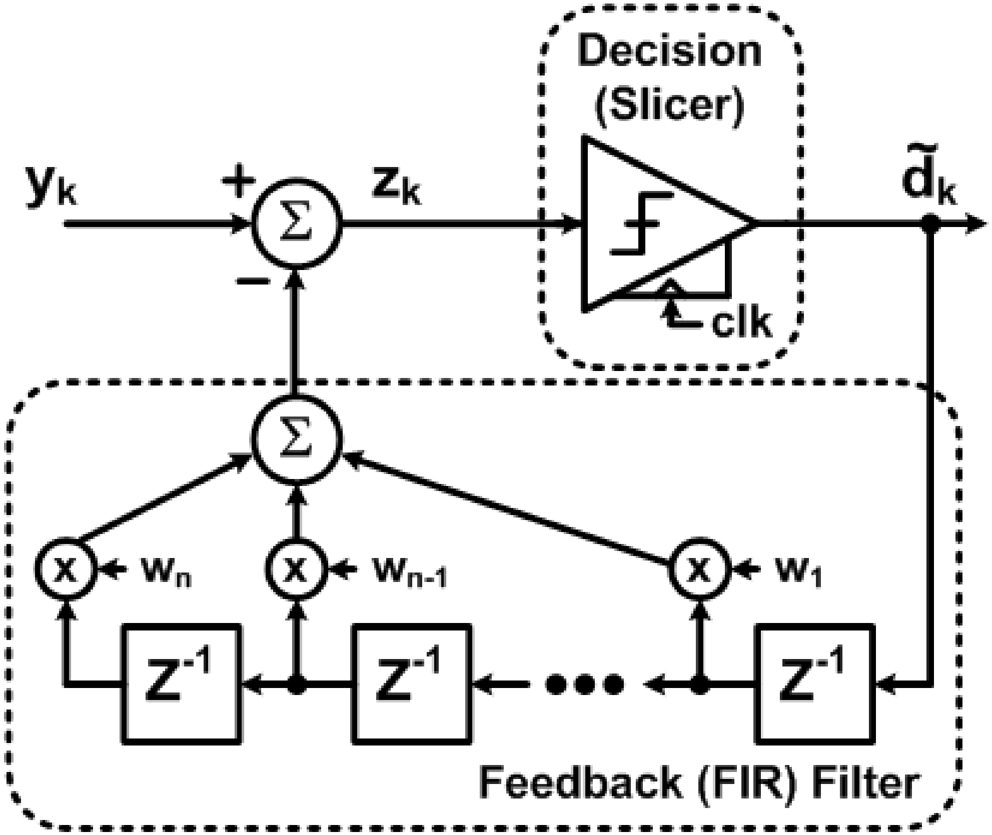




RX Decision Feedback Equalization (DFE)

$$z_k = y_k - w_1 \tilde{d}_{k-1} \cdots - w_{n-1} \tilde{d}_{k-(n-1)} - w_n \tilde{d}_{k-n}$$

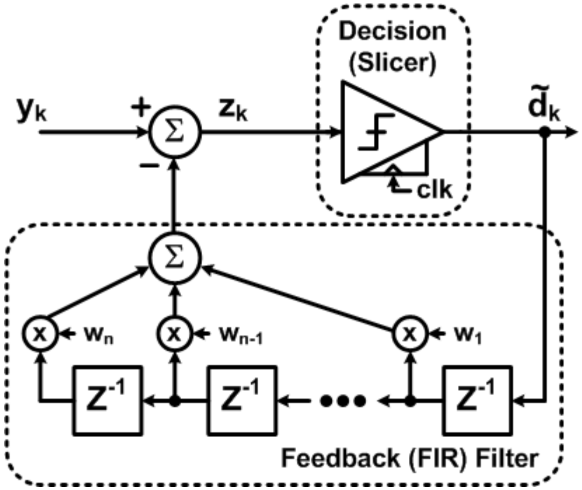
- DFE is a **non-linear** equalizer
- Slicer makes a **symbol decision**, i.e. quantizes input
- ISI is then directly subtracted from the incoming signal via a feedback FIR filter

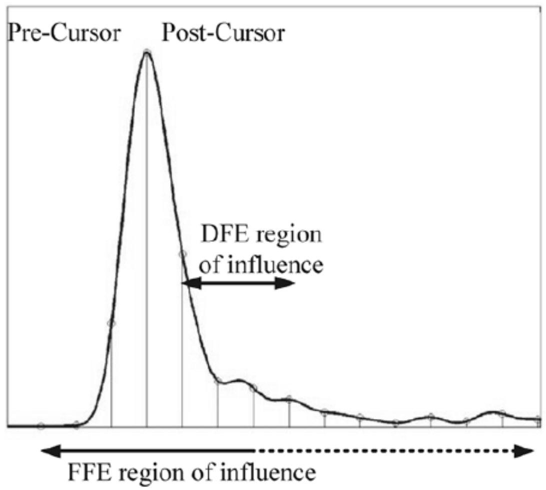


RX Decision Feedback Equalization (DFE)

- Pros
  - Can boost high frequency content without noise and crosstalk amplification
  - Filter tap coefficients can be adaptively tuned without any back-channel
- Cons
  - Cannot cancel pre-cursor ISI
  - Chance for error propagation
    - Low in practical links (BER=10^{-12})
  - Critical feedback timing path
  - Timing of ISI subtraction complicates CDR phase detection

$$z_k = y_k - w_1 \tilde{d}_{k-1} \cdots - w_{n-1} \tilde{d}_{k-(n-1)} - w_n \tilde{d}_{k-n}$$

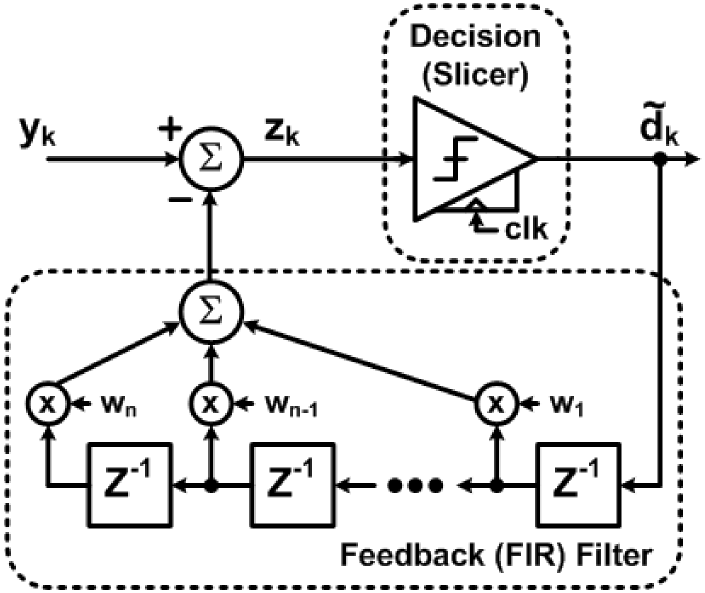




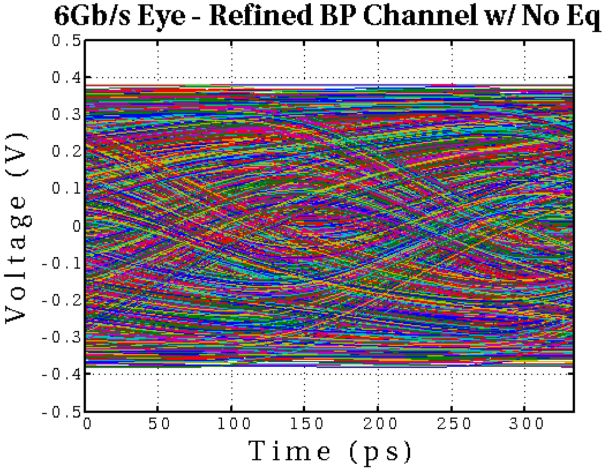
[Payne]

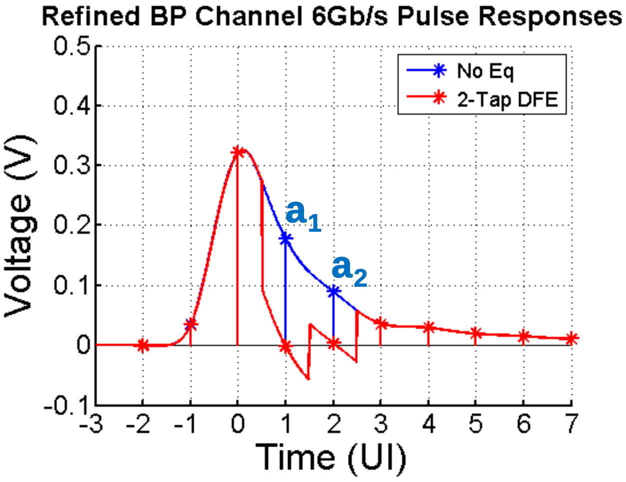
DFE Example

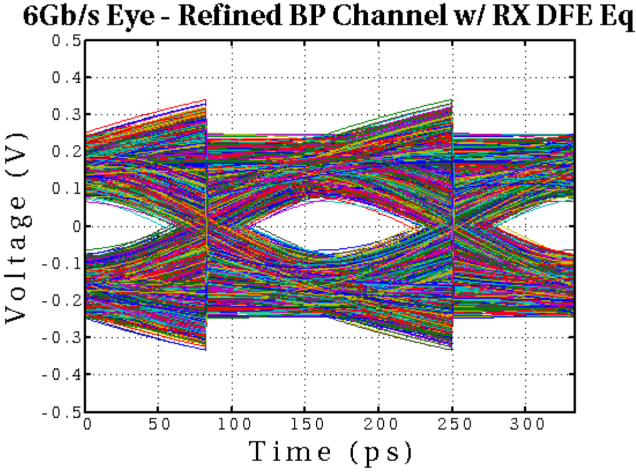
- If only DFE equalization, DFE tap coefficients should equal the unequalized channel pulse response values $[a_1\ a_2\ ...\ a_n]$
- With other equalization, DFE tap coefficients should equal the pre-DFE pulse response values



$$[w_1\ w_2] = [a_1\ a_2]$$

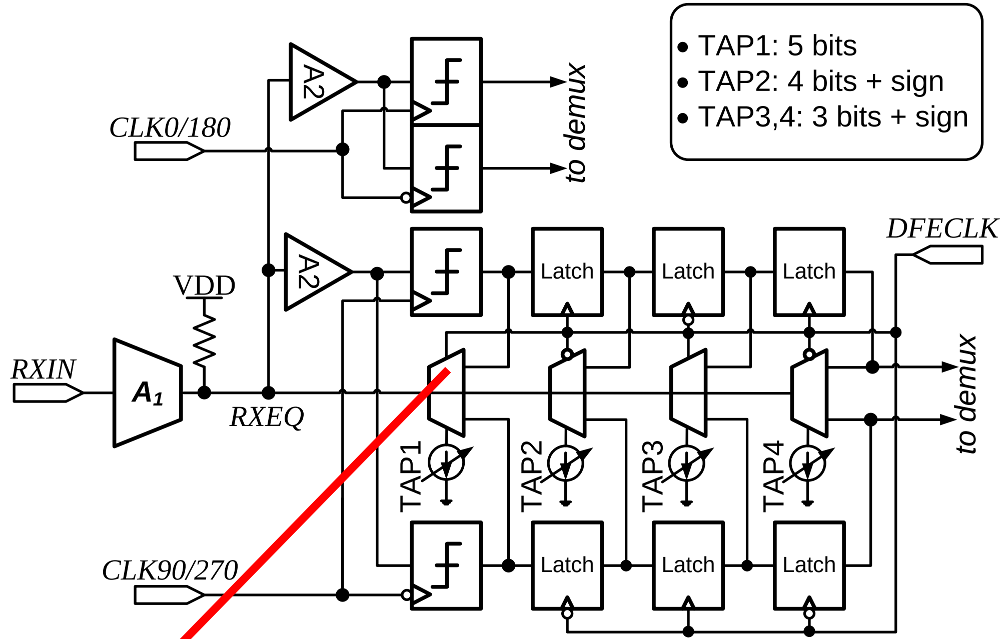




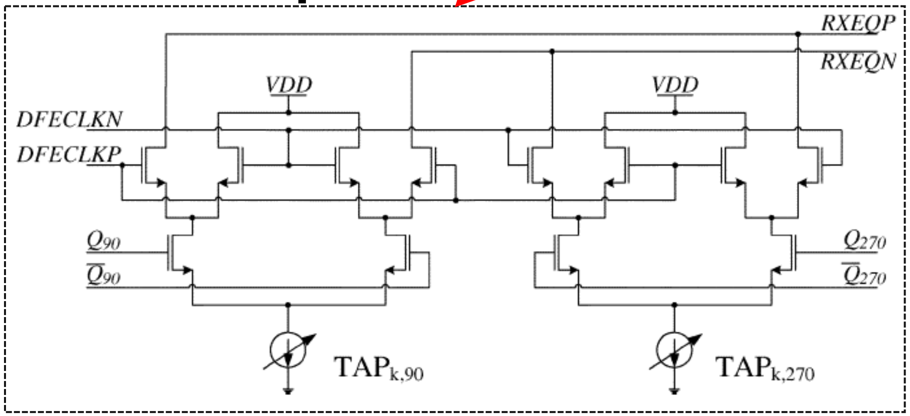


Direct Feedback DFE Example (TI)

- 6.25Gb/s 4-tap DFE
  - ½ rate architecture
  - Adaptive tap algorithm
  - Closes timing on 1st tap in **½ UI** for convergence of both adaptive equalization tap values and CDR

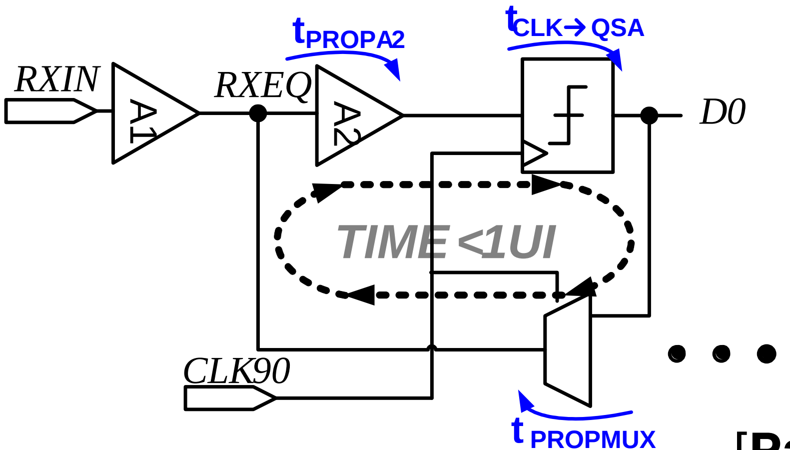


Feedback tap mux

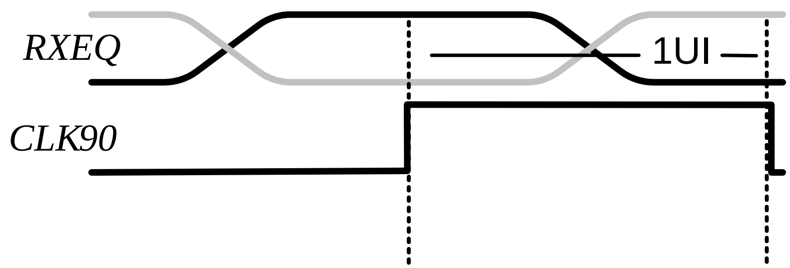


R. Payne *et al,* "A 6.25-Gb/s Binary Transceiver in 0.13-um CMOS for Serial Data Transmission Across High Loss Legacy Backplane Channels," *JSSC*, vol. 40, no. 12, Dec. 2005, pp. 2646-2657

Direct Feedback DFE Critical Path



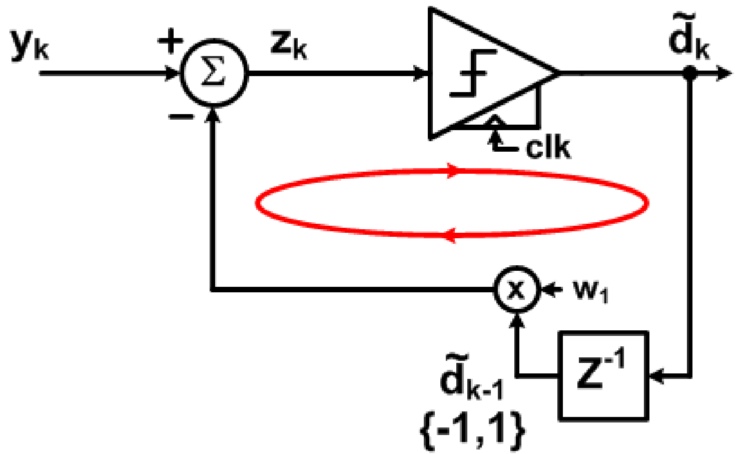
[**Payne**]

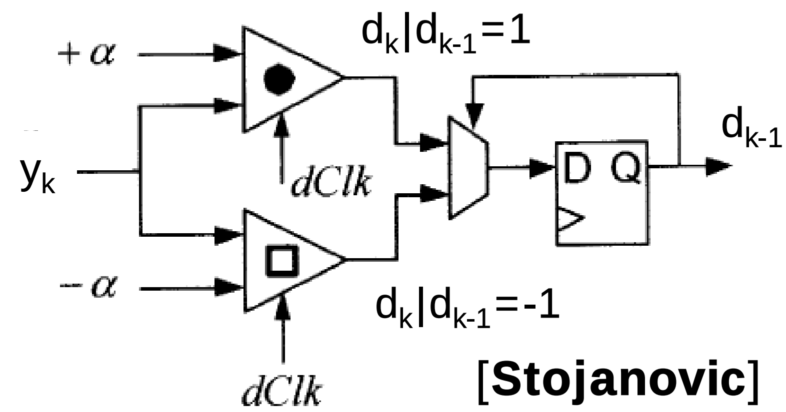


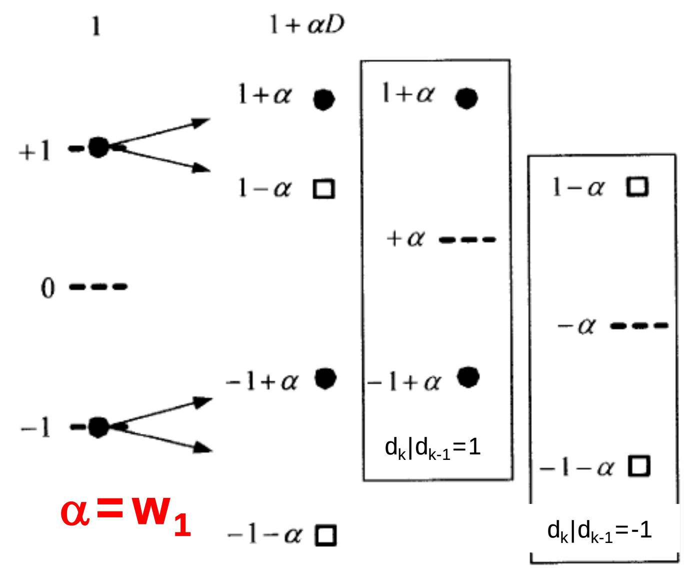
$$t_{CLK \to QSA} + t_{PROPMUX} + t_{PROPA2} \leq 1UI$$

- Must resolve data and feedback in 1 bit period
  - TI design actually does this in ½UI for CDR

DFE Loop Unrolling



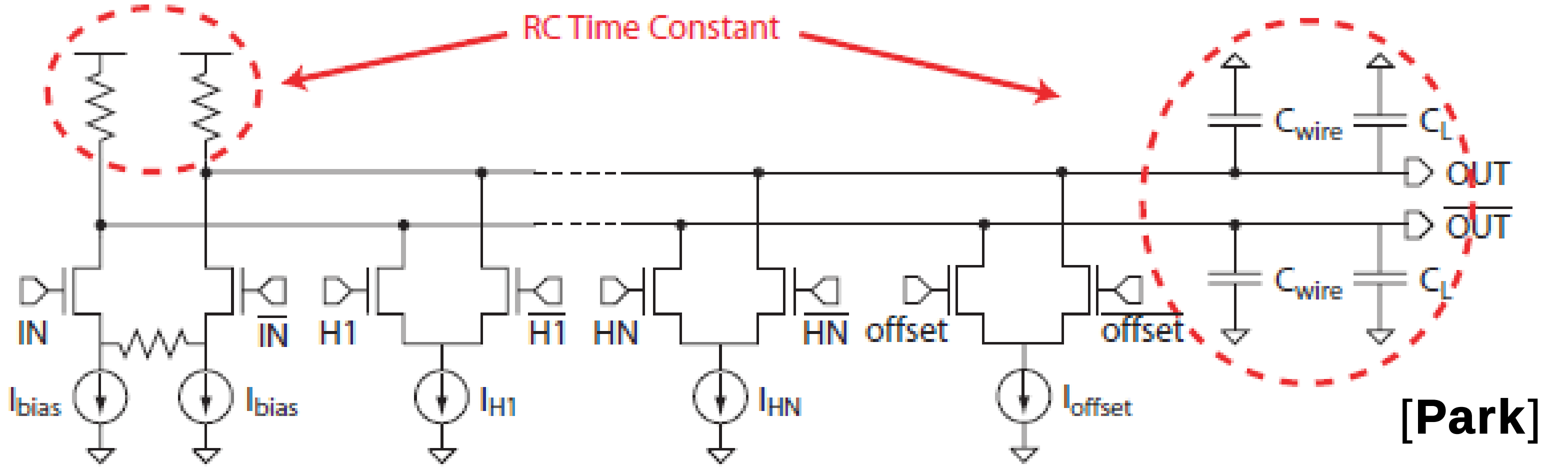




- Instead of feeding back and subtracting ISI in 1UI
- Unroll loop and pre-compute 2 possibilities (1-tap DFE) with adjustable slicer threshold
- With increasing tap number, comparator number grows as $2^{\#\text{taps}}$

$$\tilde{d}_k = \begin{cases} \operatorname{sgn}(y_k - w_1) \text{ "if" } \tilde{d}_{k-1} = 1 \\ \operatorname{sgn}(y_k + w_1) \text{ "if" } \tilde{d}_{k-1} = -1 \end{cases}$$

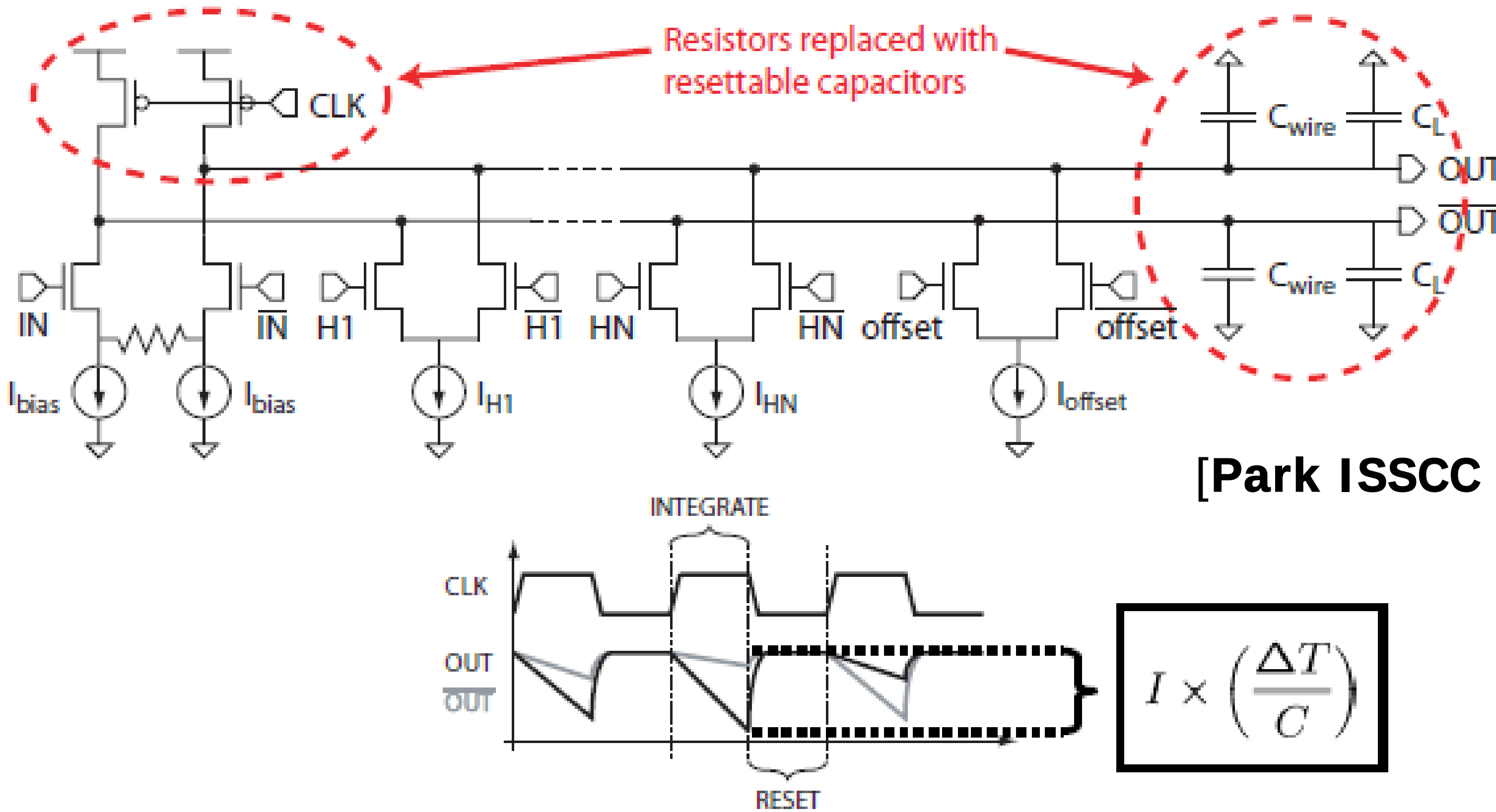
DFE Resistive-Load Summer



$$\textbf{Summer Swing} = IR, \quad \tau = RC$$

- Summer performance is critical for DFE operation
- Summer must settle within a certain level of accuracy (>95%) for ISI cancellation
- Trade-off between summer output swing and settling time
- Can result in large bias currents for input and taps

DFE Integrating Summer

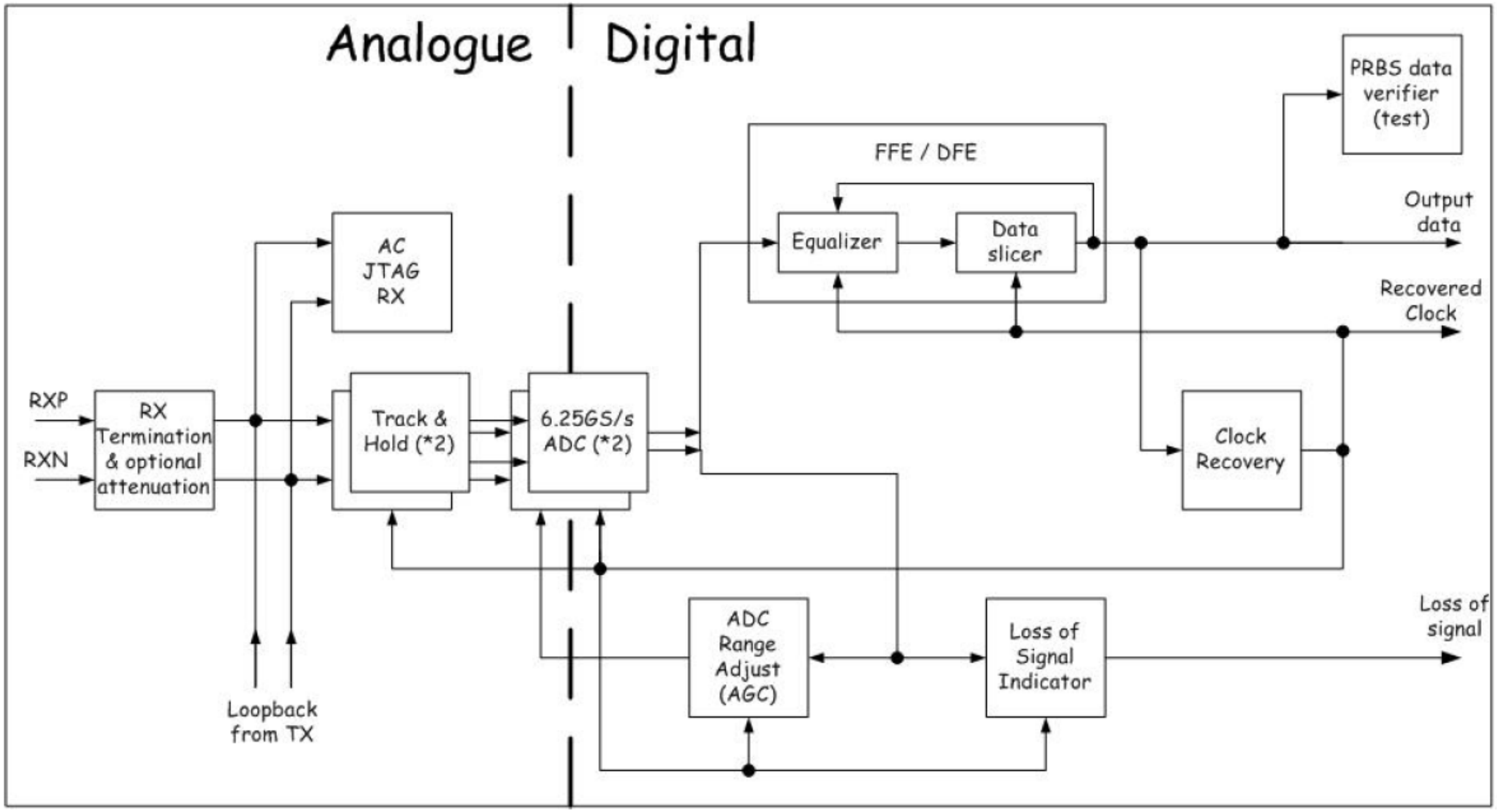


$$I \times \left(\frac{\Delta T}{C}\right)$$

[Park ISSCC 2007]

- Integrating current onto load capacitances eliminates RC settling time
- Since ΔT/C > R, bias current can be reduced for a given output swing
  - Typically a 3x bias current reduction

Digital RX FIR & DFE Equalization Example



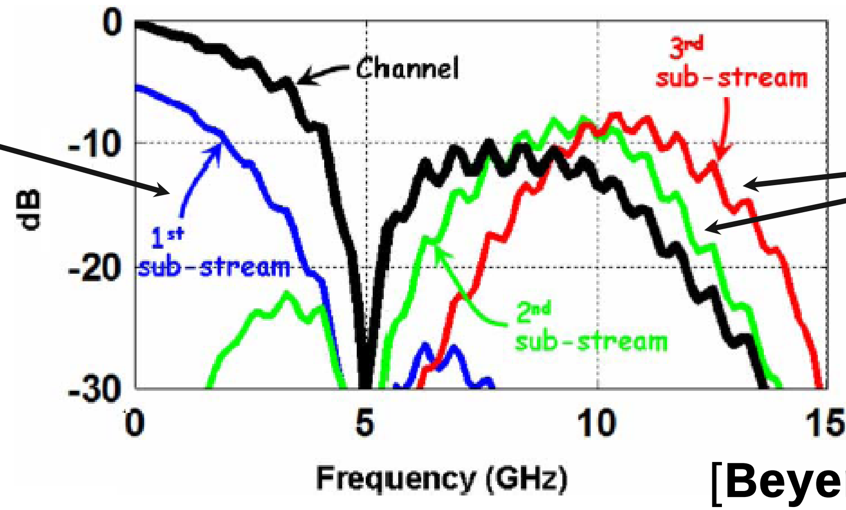
- 12.5GS/s 4.5-bit Flash ADC in 65nm CMOS [**Harwood ISSCC 2007**]
- 2-tap FFE & 5-tap DFE
- XCVR power (inc. TX) = 330mW, Analog = 245mW, Digital = 85mW

Advanced Modulation

- In order to remove ISI, we attempt to equalize or flatten the channel response out to the Nyquist frequency
- For less frequency-dependent loss, move the Nyquist frequency to a lower value via more advance modulation
  - 4-PAM (or higher)
  - Duo-binary
- Refer to lecture 9 for more details

Multi-tone Signaling

10Gb/s duo-binary



2 Quarature 10Gb/s duo-binary

30Gb/s total!

[**Beyene AdvPack 2008**]

- Instead equalizing out to baseband Nyquist frequency
- Divide the channel into bands with less frequency-dependent loss
- Should result in less equalization complexity for each sub-band
- Requires up/down-conversion
- Discrete Multi-tone used in DSL modems with very challenging channels
  - Lower data rates allow for high performance DSP
  - High-speed links don’t have this option (yet)

Next Time

- Link Noise and BER Analysis