ECEN689: Special Topics in High-Speed Links Circuits and Systems
Spring 2010

Lecture 18: RX FIR & CTLE Equalization

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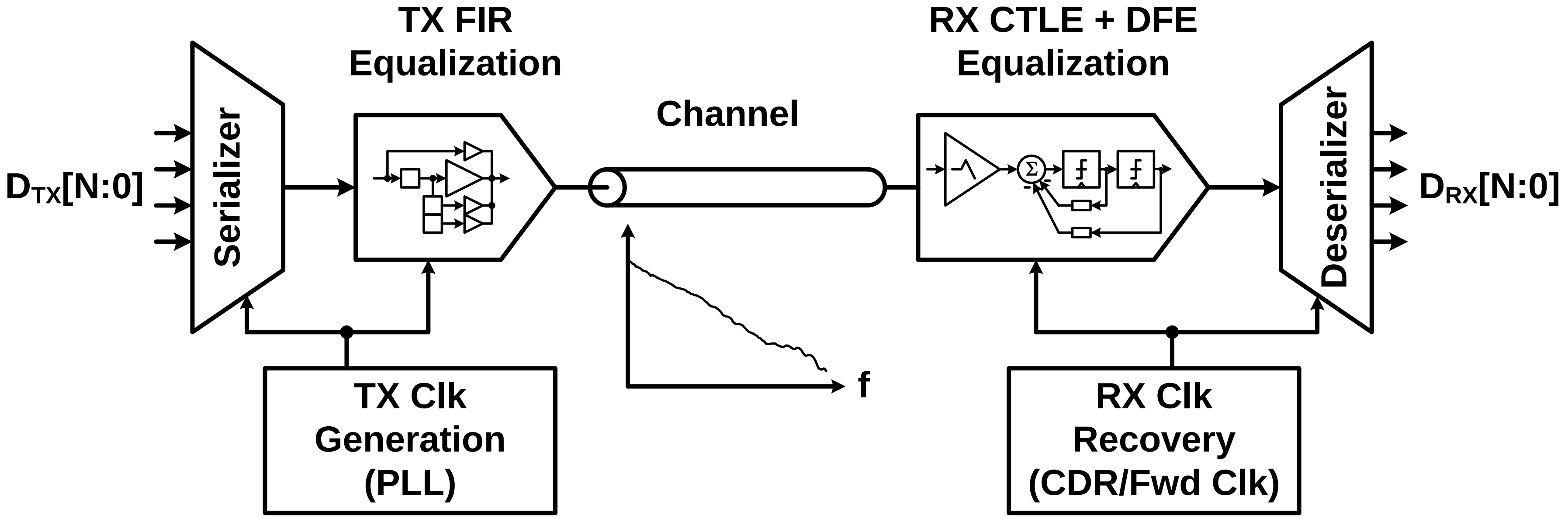
Announcements

- HW5 now due Friday (in class)
  - Any issues?
- Reading
  - Hanumolu equalization overview paper

Agenda

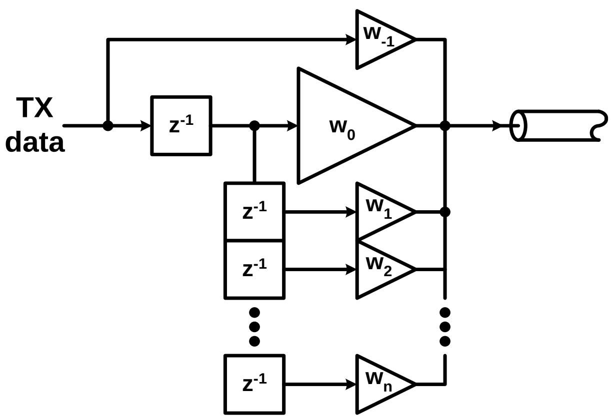
- RX FIR Equalization
- RX CTLE Equalization

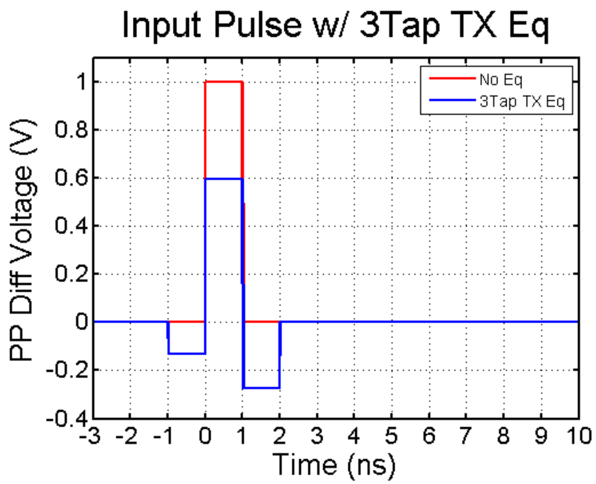
Link with Equalization

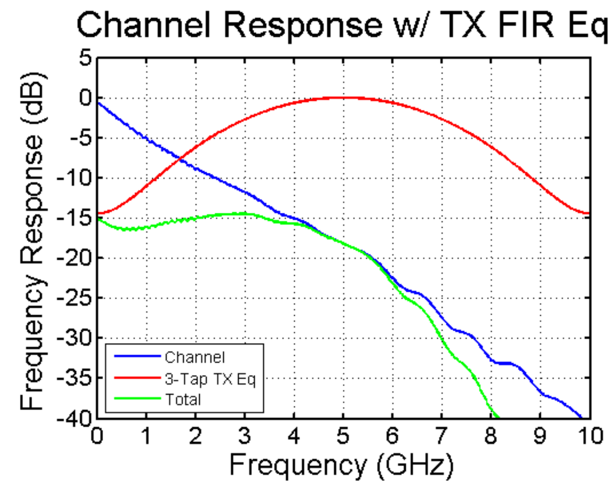


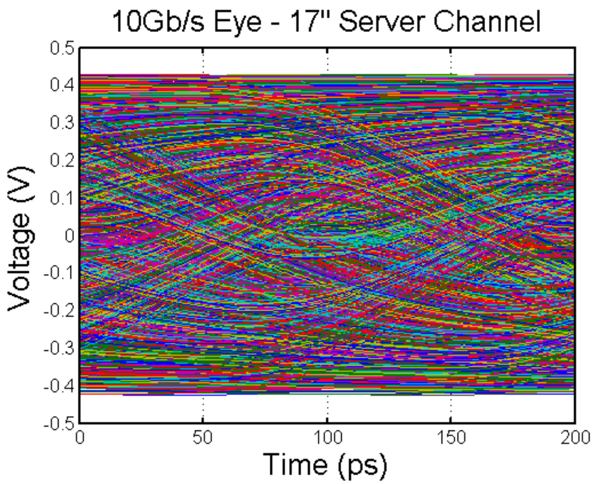
TX FIR Equalization

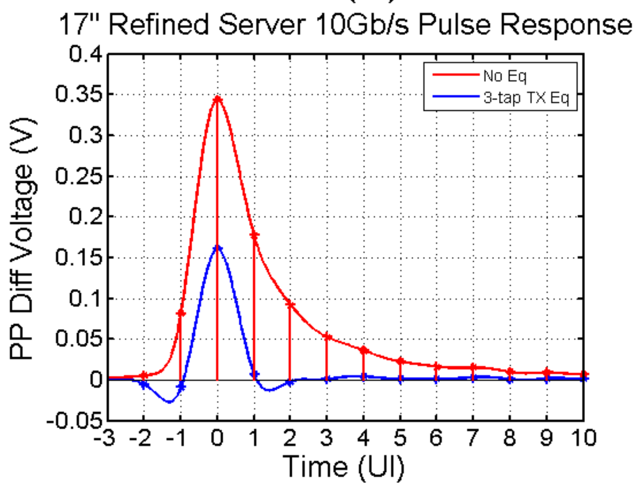
- TX FIR filter pre-distorts transmitted pulse in order to invert channel distortion at the cost of attenuated transmit signal (de-emphasis)

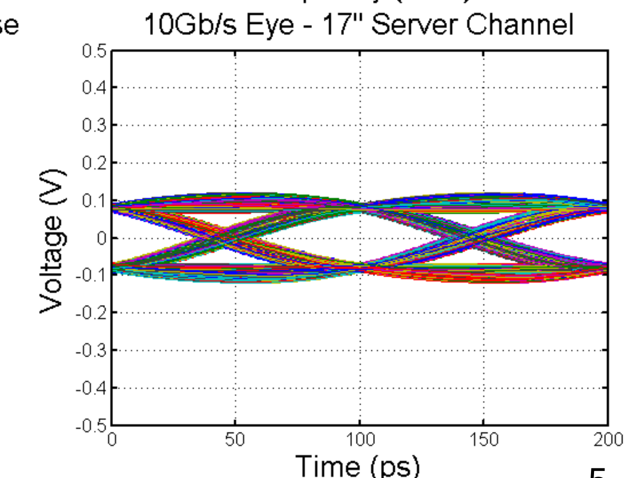






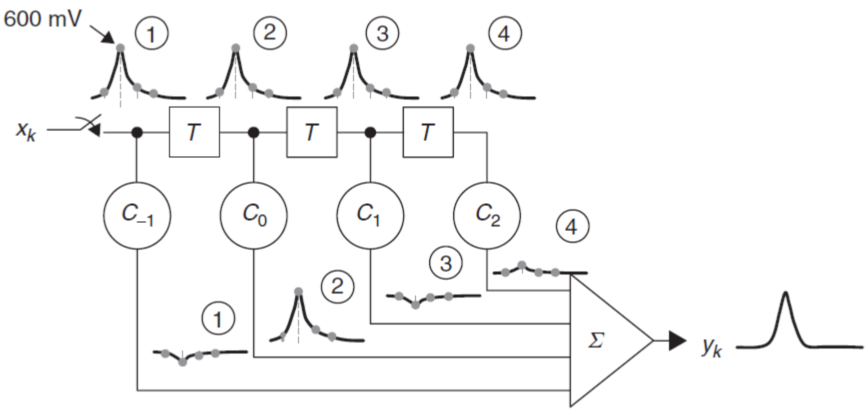


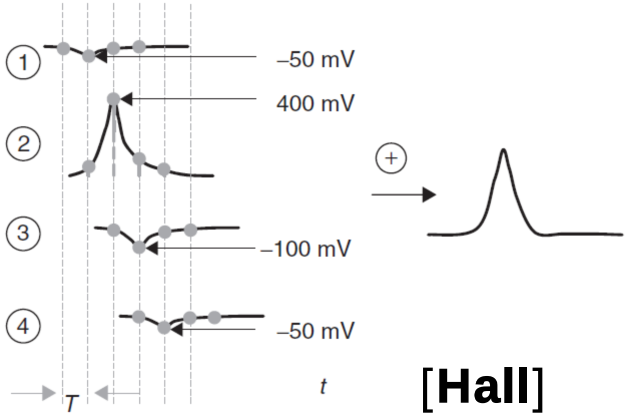




RX FIR Equalization

- Delay analog input signal and multiply by equalization coefficients
- Pros
  - With sufficient dynamic range, can amplify high frequency content (rather than attenuate low frequencies)
  - Can cancel ISI in pre-cursor and beyond filter span
  - Filter tap coefficients can be adaptively tuned without any back-channel
- Cons
  - Amplifies noise/crosstalk
  - Implementation of analog delays
  - Tap precision

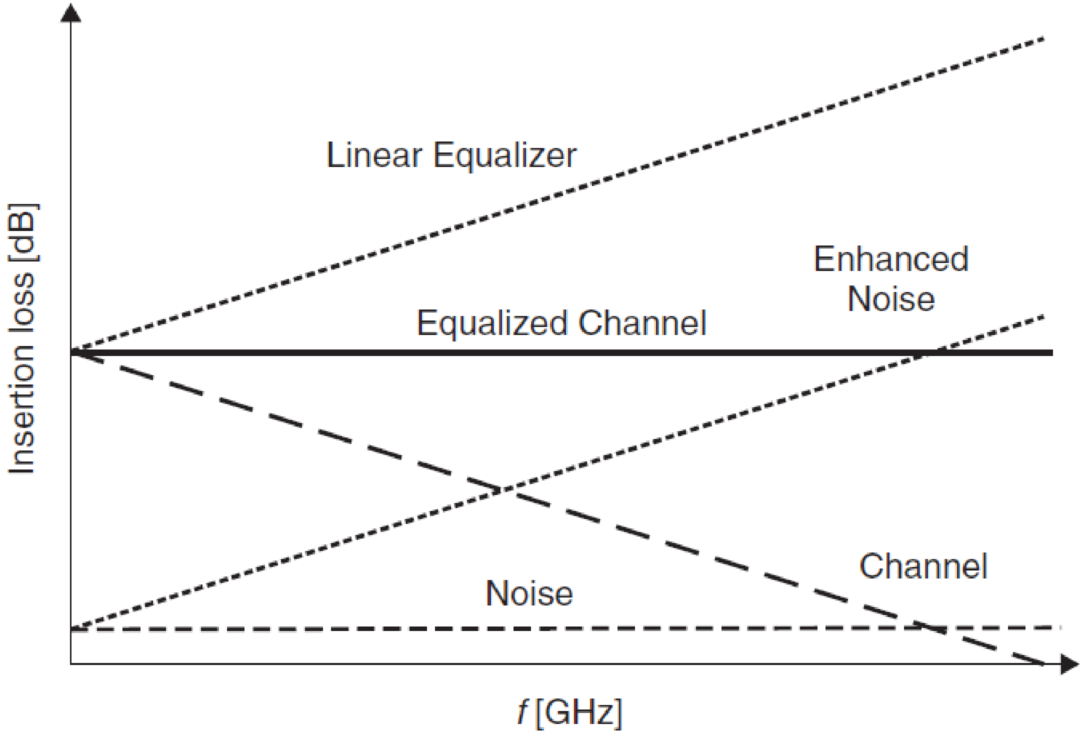




[Hall]

RX Equalization Noise Enhancement

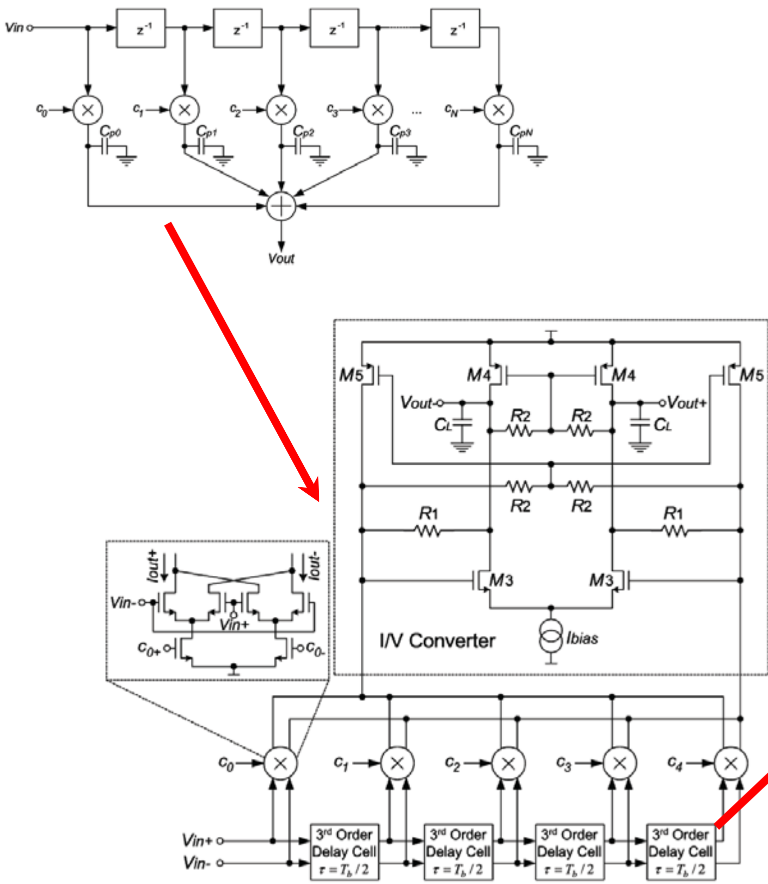
- Linear RX equalizers don't discriminate between signal, noise, and cross-talk
  - While signal-to-distortion (ISI) ratio is improved, SNR remains unchanged



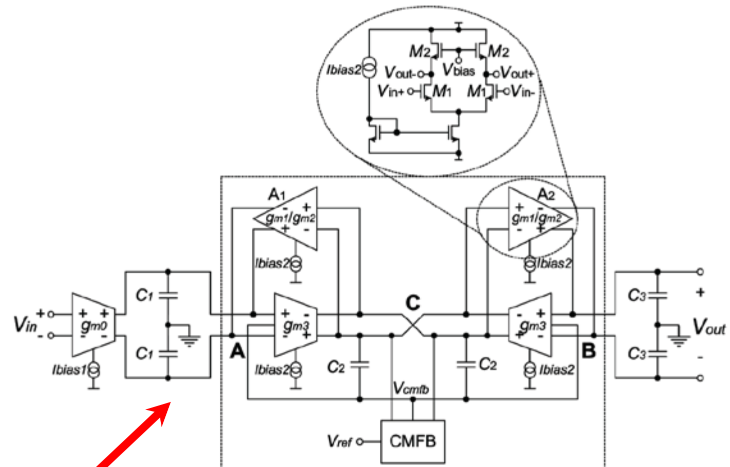
[**Hall**]

Analog RX FIR Equalization Example

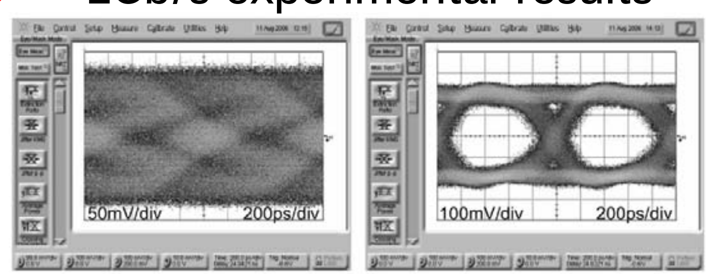
- 5-tap equalizer with tap spacing of $T_b/2$



3rd-order delay cell



1Gb/s experimental results

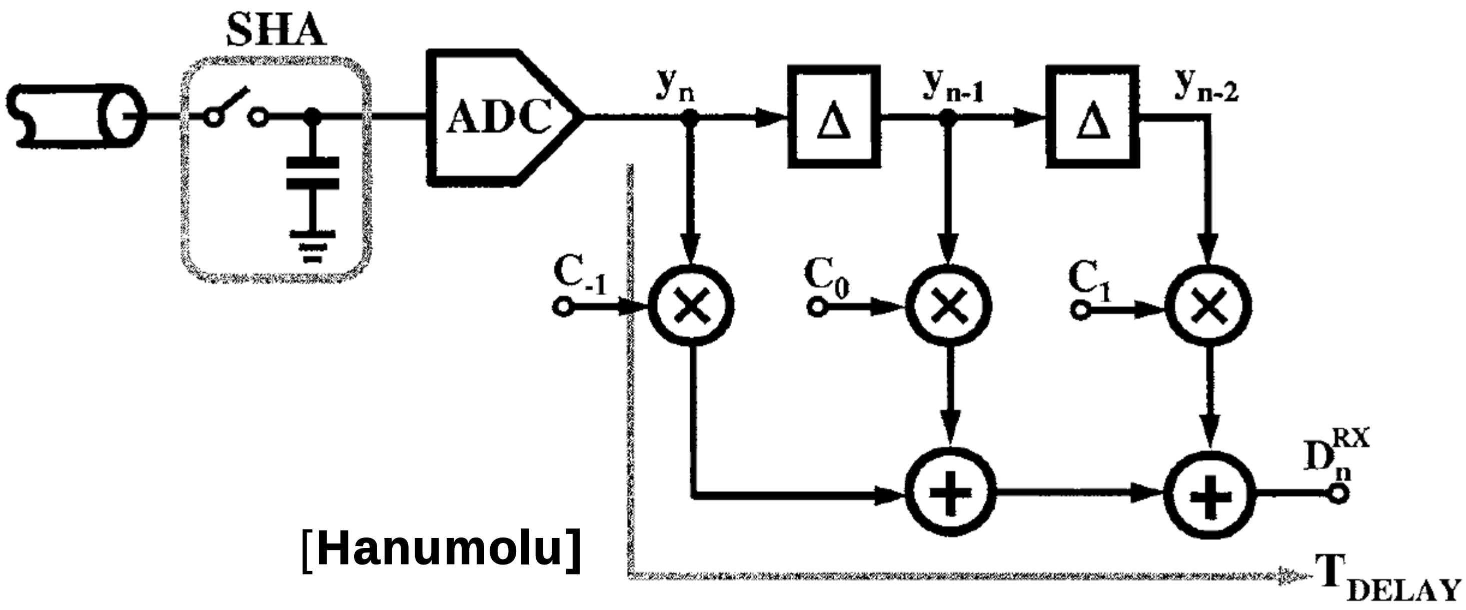


Before Equalizer: 23meters After Equalizer: 23meters

D. Hernandez-Garduno and J. Silva-Martinez, "A CMOS 1Gb/s 5-Tap Transversal Equalizer based on 3rd-Order Delay Cells," ISSCC, 2007.

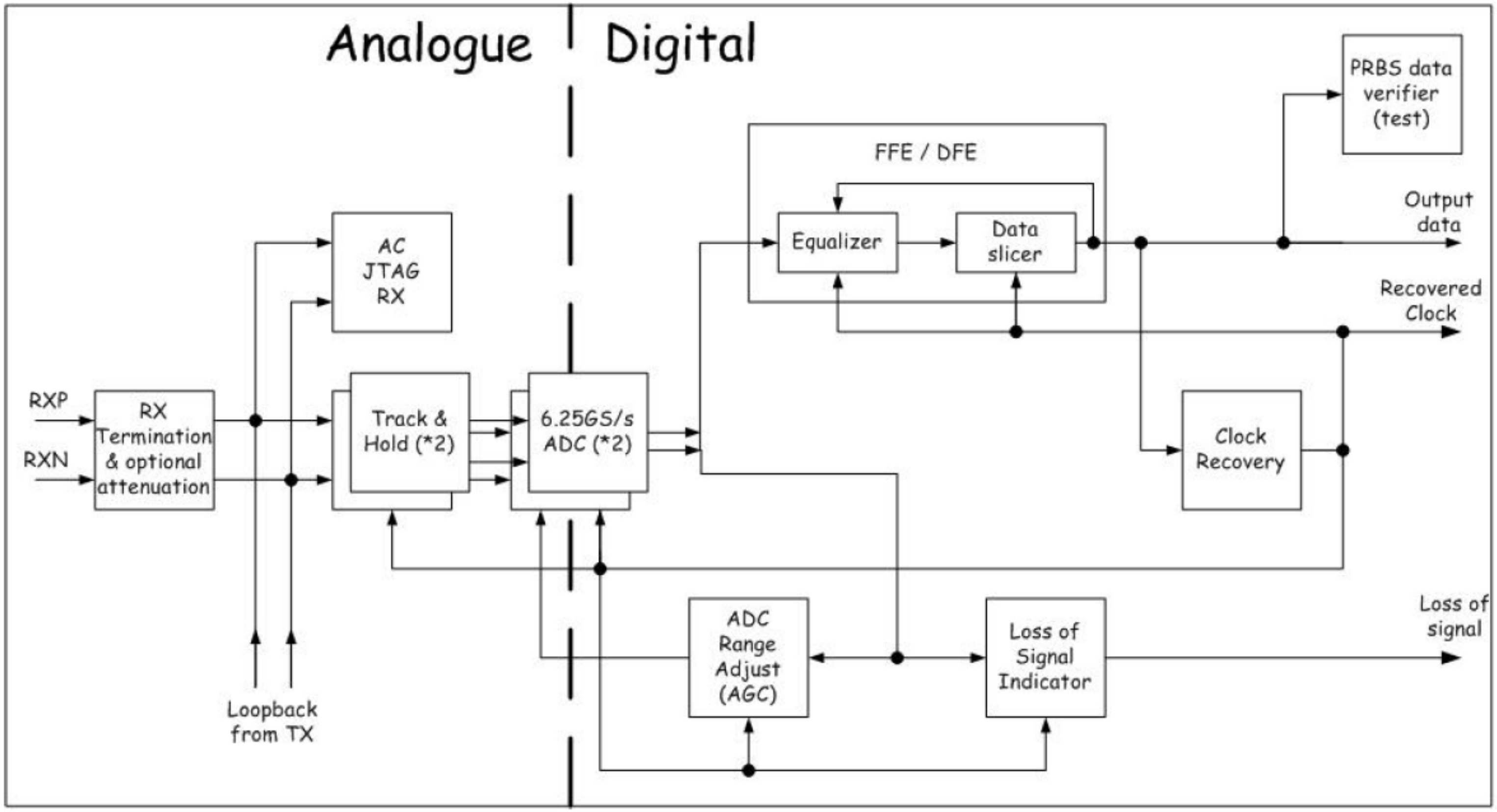
Digital RX FIR Equalization

- Digitize the input signal with high-speed low/medium resolution ADC and perform equalization in digital domain
  - Digital delays, multipliers, adders
  - Limited to ADC resolution
- Power can be high due to very fast ADC



[Hanumolu]

Digital RX FIR Equalization Example



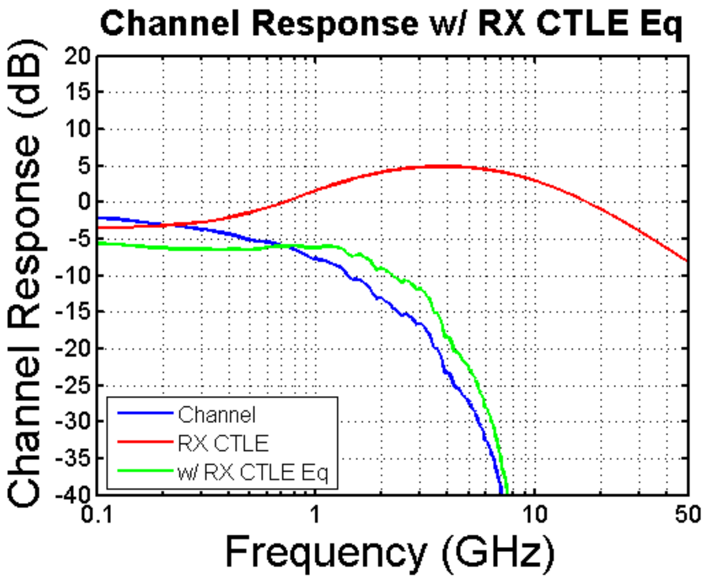
- 12.5GS/s 4.5-bit Flash ADC in 65nm CMOS

[**Harwood ISSCC 2007**]

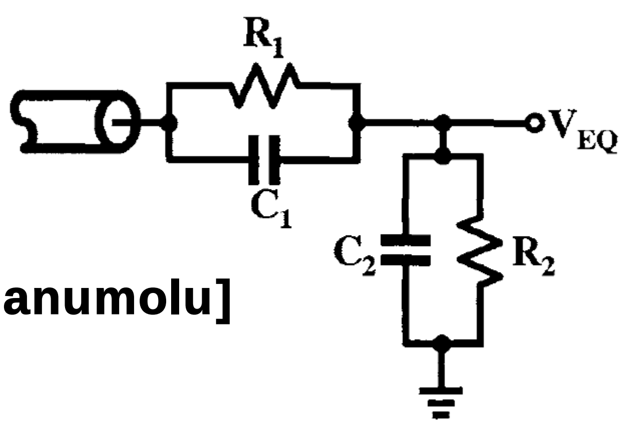
- 2-tap FFE & 5-tap DFE
- XCVR power (inc. TX) = 330mW, Analog = 245mW, Digital = 85mW

RX Continuous-Time Linear Equalizer (CTLE)

- Passive R-C (or L) can implement high-pass transfer function to compensate for channel loss
- Cancel both precursor and long-tail ISI
- Can be purely passive or combined with an amplifier to provide gain

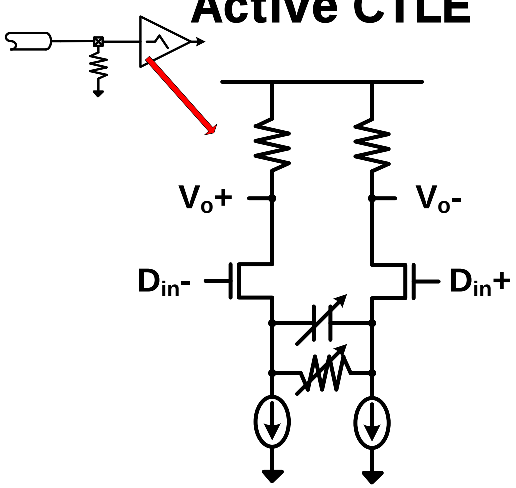


Passive CTLE



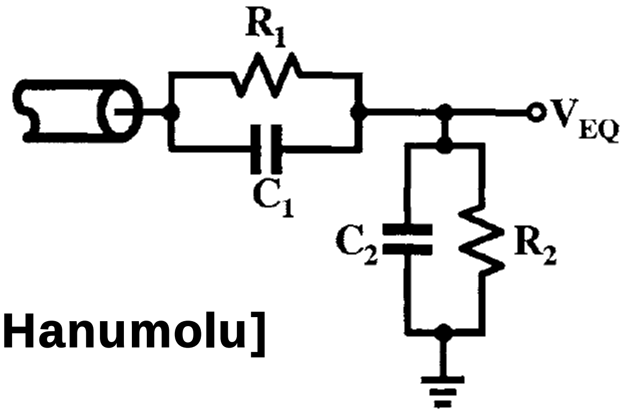
[**Hanumolu**]

Active CTLE



Passive CTLE

- Passive structures offer excellent linearity, but no gain at Nyquist frequency



[Hanumolu]

$$H(s) = \frac{R_2}{R_1 + R_2} \frac{1 + R_1 C_1 s}{1 + \frac{R_1 R_2}{R_1 + R_2}(C_1 + C_2)s}$$

$$\omega_z = \frac{1}{R_1 C_1}, \qquad \omega_\mathrm{p} = \frac{1}{\frac{R_1 R_2}{R_1 + R_2}(C_1 + C_2)}$$

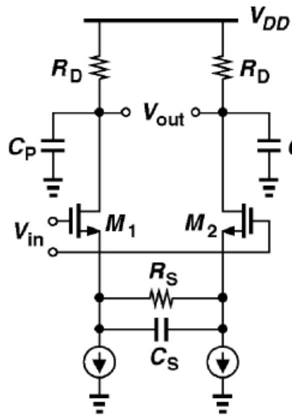
$$\textbf{DC gain} = \frac{R_2}{R_1 + R_2}, \ \textbf{HF gain} = \frac{C_1}{C_1 + C_2}$$

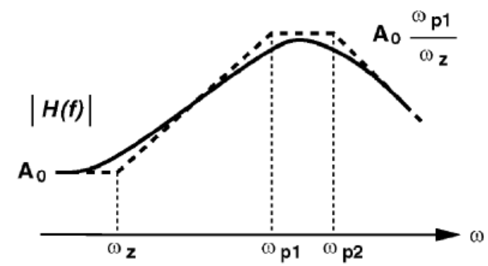
$$\textbf{Peaking} = \frac{\textbf{HF gain}}{\textbf{DC gain}} = \frac{\omega_p}{\omega_z} = \frac{R_1 + R_2}{R_2} \frac{C_1}{C_1 + C_2}$$

Active CTLE

- Input amplifier with RC degeneration can provide frequency peaking with gain at Nyquist frequency
- Potentially limited by gain-bandwidth of amplifier
- Amplifier must be designed for input linear range
  - Often TX eq. provides some low frequency attenuation
- Sensitive to PVT variations and can be hard to tune
- Generally limited to 1st-order compensation

[Gondi JSSC 2007]





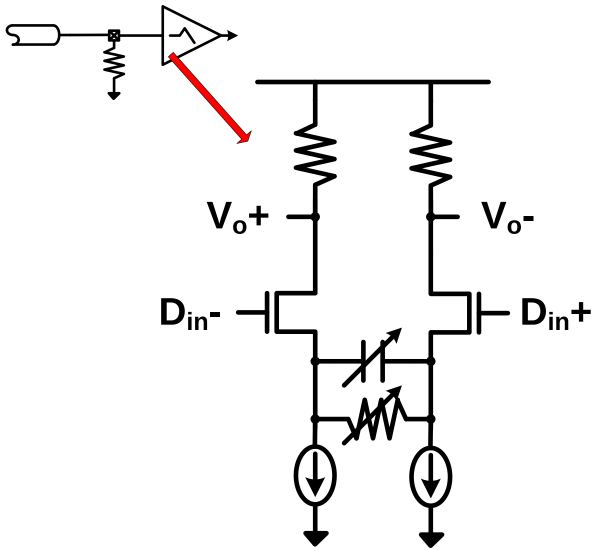
$$H(s) = \frac{g_m}{C_p} \frac{s + \frac{1}{R_S C_S}}{\left(s + \frac{1 + g_m R_S/2}{R_S C_S}\right)\left(s + \frac{1}{R_D C_p}\right)}$$

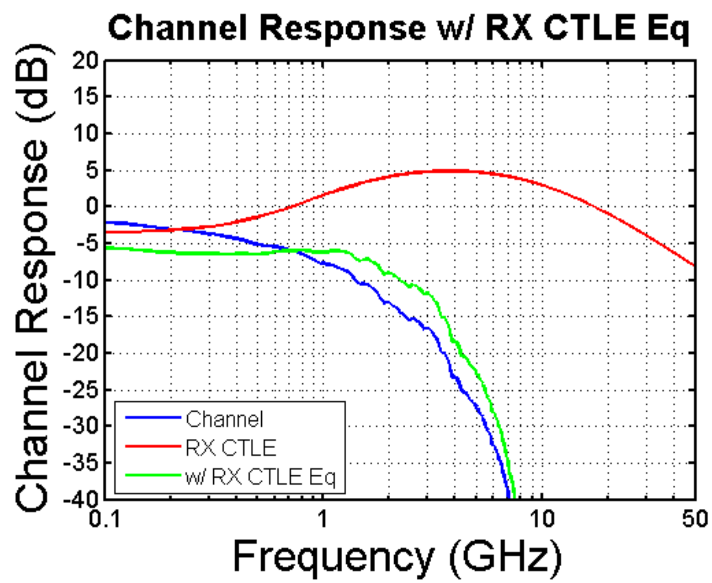
$$\omega_z = \frac{1}{R_S C_S}, \quad \omega_{\mathbf{p1}} = \frac{1 + g_m R_S/2}{R_S C_S}, \quad \omega_{\mathbf{p2}} = \frac{1}{R_D C_p}$$

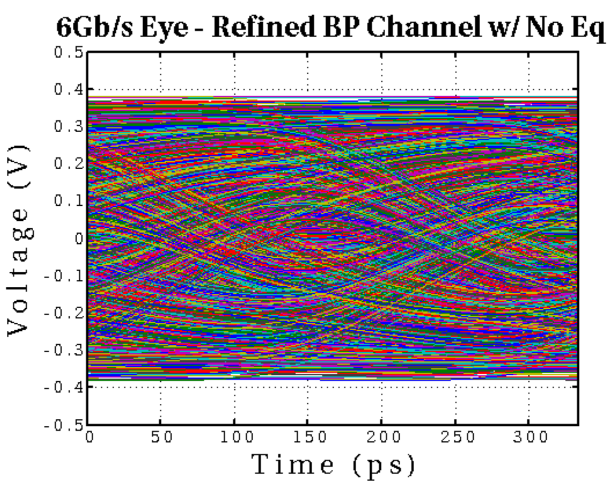
$$\textbf{DC gain} = \frac{g_m R_D}{1 + g_m R_S/2}, \quad \textbf{Ideal peak gain} = g_m R_D$$

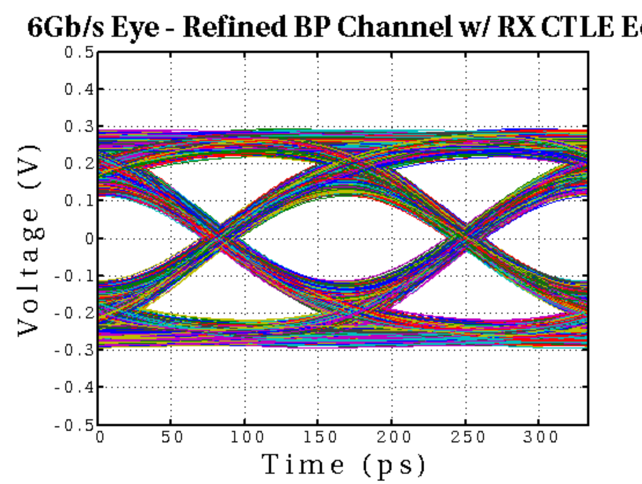
$$\textbf{Ideal Peaking} = \frac{\textbf{Ideal peak gain}}{\textbf{DC gain}} = \frac{\omega_{p1}}{\omega_z} = 1 + g_m R_S/2$$

Active CTLE Example





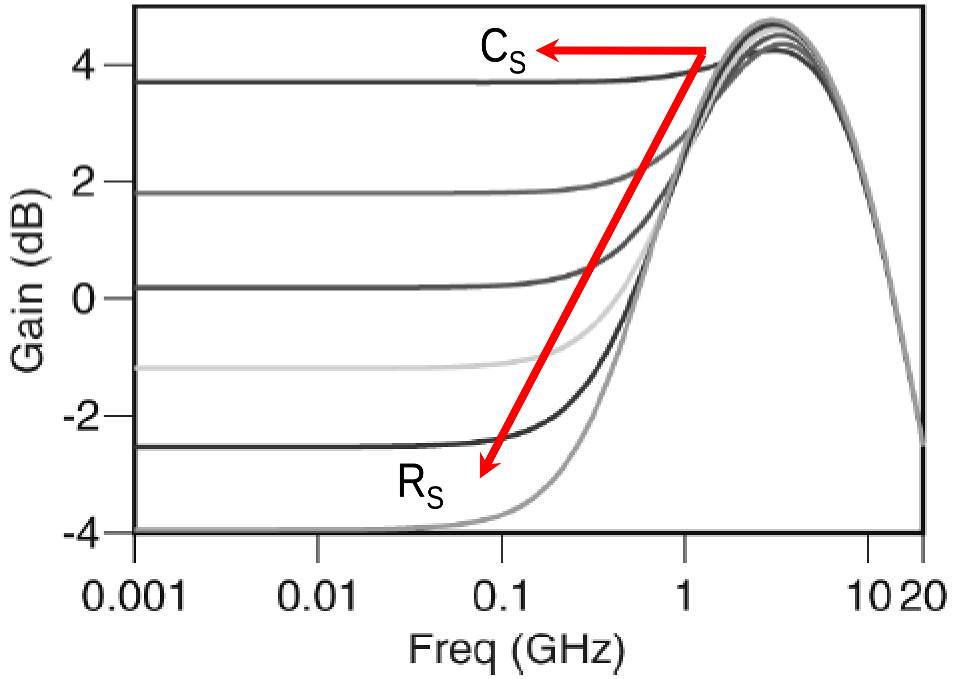




Active CTLE Tuning

- Tune degeneration resistor and capacitor to adjust zero frequency and 1st pole which sets peaking and DC gain

$$\omega_z = \frac{1}{R_S C_S}, \quad \omega_{\mathbf{p1}} = \frac{1 + g_m R_S / 2}{R_S C_S}$$



Next Time

- RX DFE
- Alternate/Future Approaches