ECEN689: Special Topics in High-Speed Links Circuits and Systems
Spring 2010

Lecture 17: TX FIR Equalization

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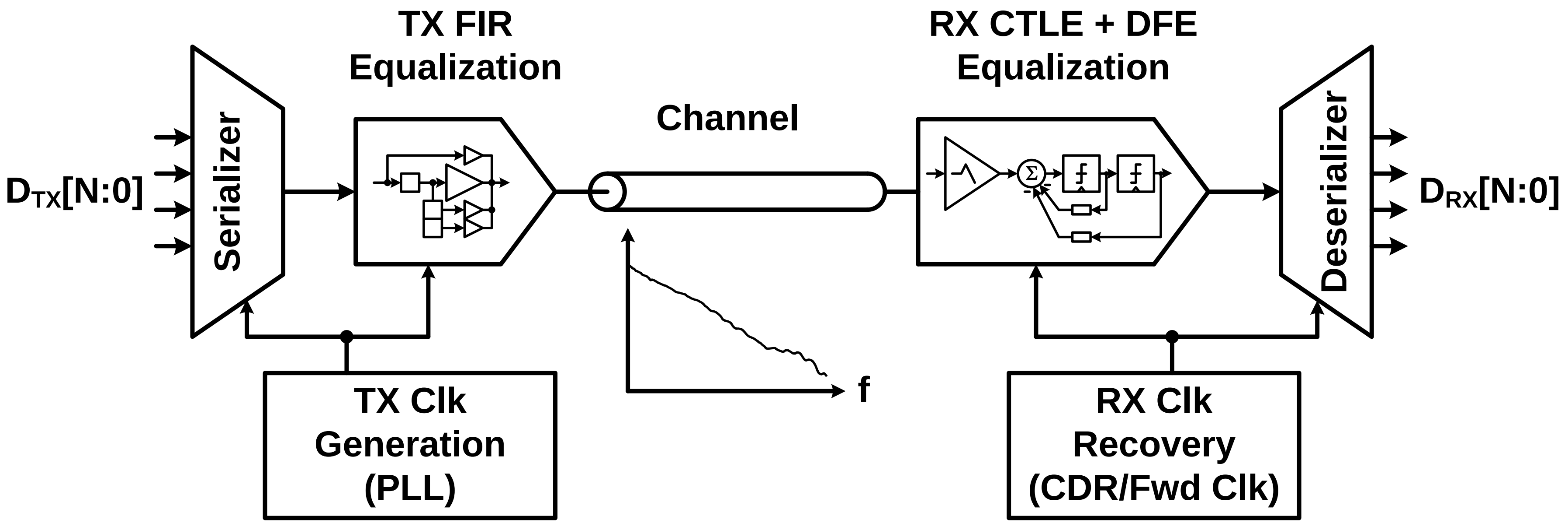
Announcements

- HW4 due today 5PM
  - Any issues?
- HW5 posted today and due March 24 (2 wks from today)
- Exam 1 is Friday
  - 9:10-10:10AM (10 extra minutes)
  - Closed book w/ one standard note sheet
    - 8.5”x11” front & back
  - Bring your calculator
- Reading
  - Equalization overview paper will be posted

Agenda

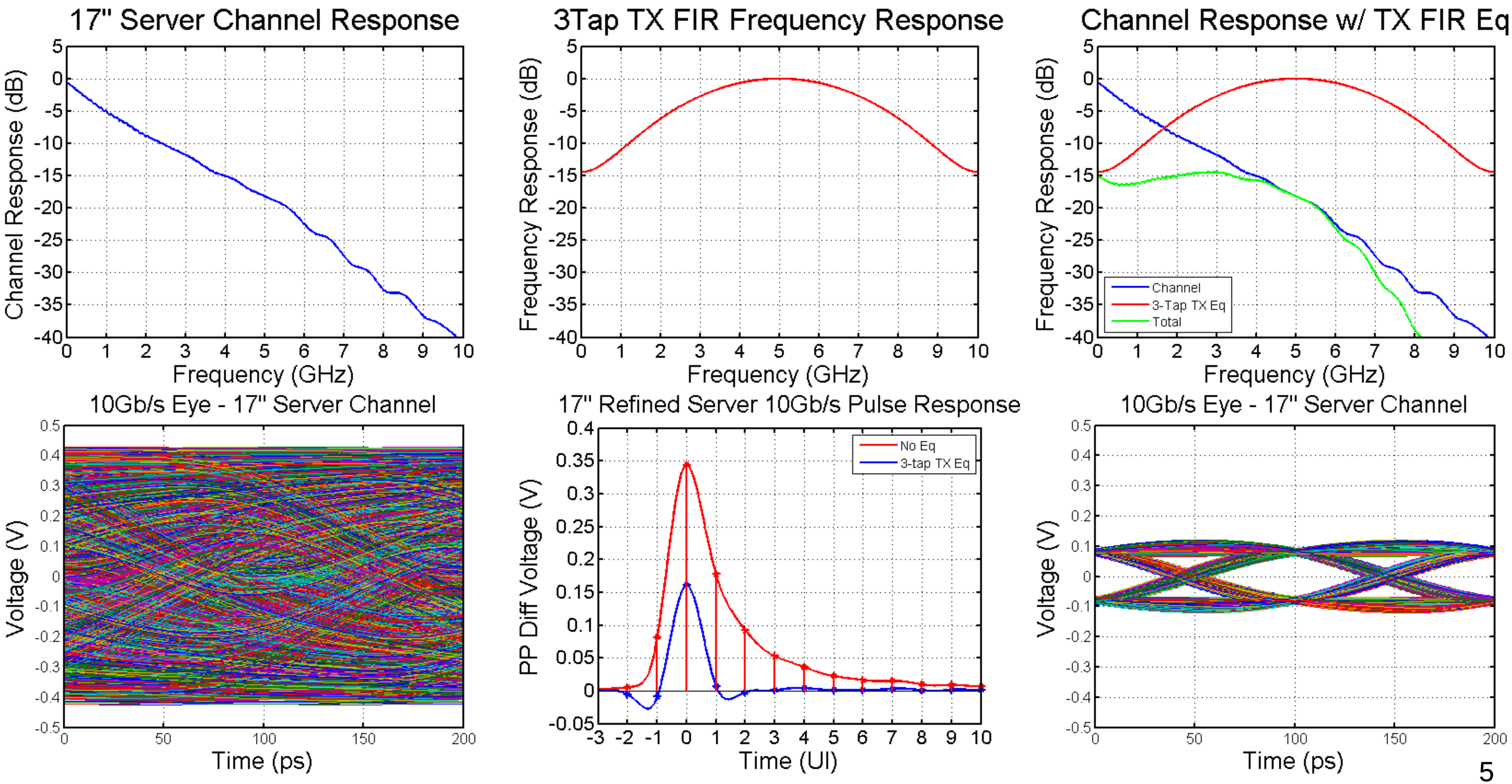
- TX FIR Equalization

Link with Equalization



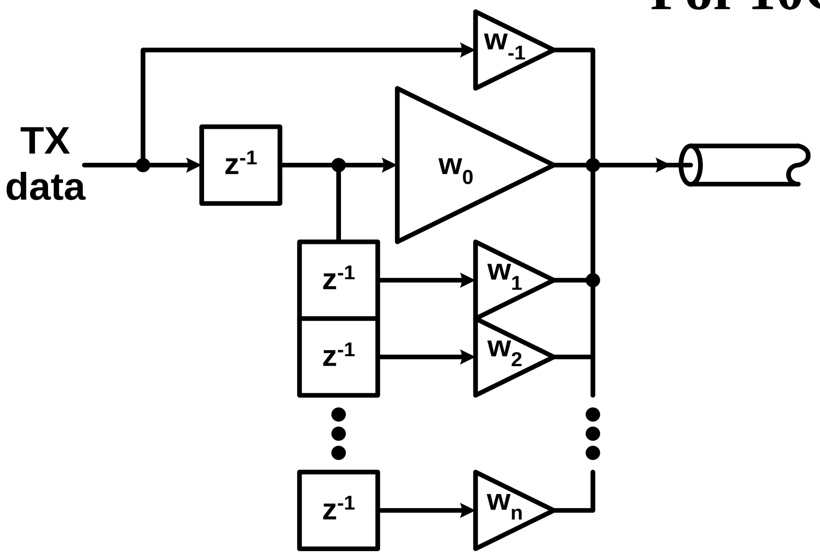
Channel Equalization

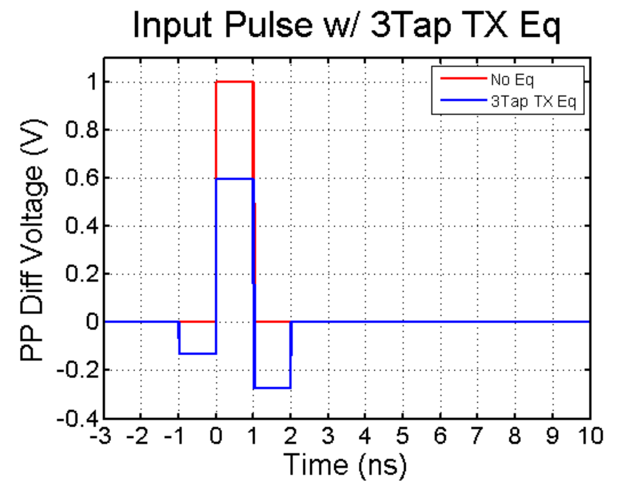
- Equalization goal is to flatten the frequency response out to the Nyquist Frequency and remove time-domain ISI



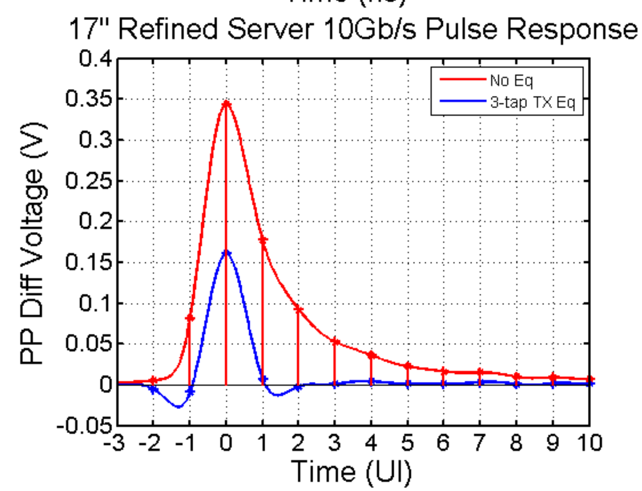
TX FIR Equalization – Time Domain

For 10Gbps : $W(z) = -0.131 + 0.595z^{-1} - 0.274z^{-2}$





$$\mathbf{W} = \left[-0.131 \quad 0.595 \quad -0.274\right]$$



Low Frequency Response (Sum Taps)

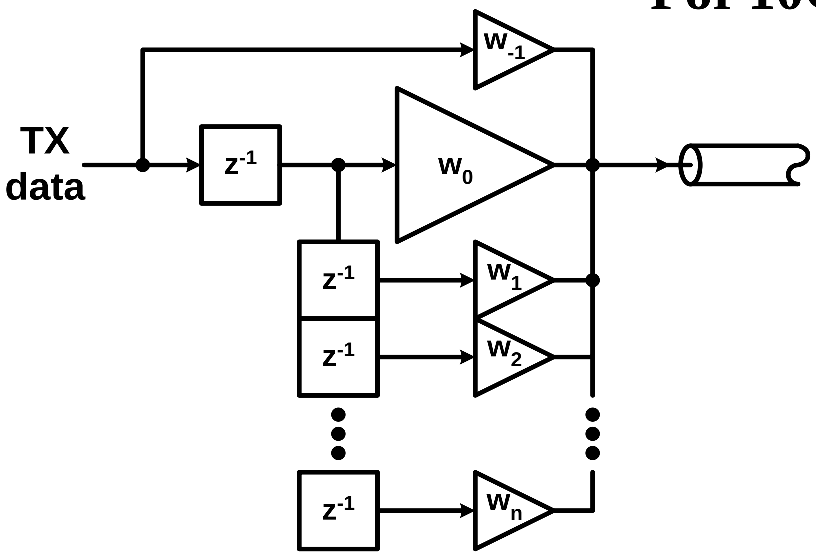
$$[\ldots \quad 1 \quad 1 \quad 1 \quad \ldots] * [-0.131 \quad 0.595 \quad -0.274] = [\ldots \quad 0.190 \quad 0.190 \quad 0.190 \quad \ldots]$$

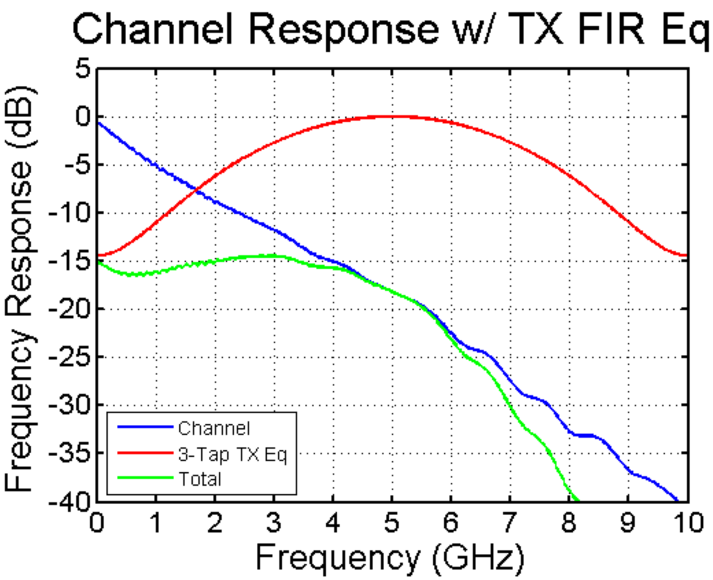
Nyquist Frequency Response (Sum Taps w/ Alternating Polarity)

$$[\ldots \quad -1 \quad 1 \quad -1 \quad \ldots] * [-0.131 \quad 0.595 \quad -0.274] = [\ldots \quad 1 \quad -1 \quad 1 \quad \ldots]$$

TX FIR Equalization – Freq. Domain

$$\textbf{For 10Gbps}: W(z) = -0.131 + 0.595z^{-1} - 0.274z^{-2}$$





$$W(z) = -0.131 + 0.595z^{-1} - 0.274z^{-2}$$

$$\text{w/}\quad z = e^{j2\pi f T_s} = \cos(2\pi f T_s) + j\sin(2\pi f T_s)$$

Low Frequency Response $(f = 0)$

$$z = \cos(0) + j\sin(0) = 1 \Rightarrow W(f = 0) = 0.190 \Rightarrow -14.4dB$$

Nyquist Frequency Response $\left(f = \frac{1}{2T_s}\right)$

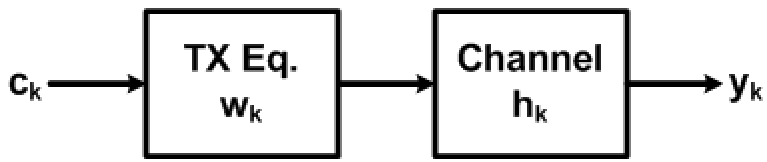
$$z = \cos(\pi) + j\sin(\pi) = -1 \Rightarrow W\left(f = \frac{1}{2T_s}\right) = -1 \Rightarrow 0dB$$

Note: Ts=Tb=100ps

- Equalizer has 14.4dB of frequency peaking
  - Attenuates DC at -14.4dB and passes Nyquist frequency at 0dB

TX FIR Coefficient Selection

- One approach to set the TX FIR coefficients is a Minimum Mean-Square Error (MMSE) Algorithm



TX Eq "w" Matrix
Rows = n+ℓ-1 where n = tap number
Columns = ℓ = input symbol number

channel output vector, y

$$\begin{bmatrix} y(0) \\ y(1) \\ \cdots \\ y(l+n+k-3) \end{bmatrix} = \begin{bmatrix} h(0) & 0 & 0 & \cdots & 0 & 0 \\ h(1) & h(0) & 0 & \cdots & 0 & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & 0 & \cdots & h(k-1) & h(k-2) \\ 0 & 0 & 0 & \cdots & 0 & h(k-1) \end{bmatrix} \begin{bmatrix} w(0) & 0 & 0 & \cdots & 0 & 0 \\ w(1) & w(0) & 0 & \cdots & 0 & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & 0 & \cdots & w(n-1) & w(n-2) \\ 0 & 0 & 0 & \cdots & 0 & w(n-1) \end{bmatrix} \begin{bmatrix} c(0) \\ c(1) \\ \cdots \\ c(l-1) \end{bmatrix}$$

Channel "h" Matrix
Rows = k+n+ℓ-1 where k = channel pulse model length
Columns = n+ℓ-1

ℓ input symbols, c

TX FIR Coefficient Selection

- Total system

$$\begin{bmatrix} y(0) \\ y(1) \\ \dots \\ y(l+n+k-3) \end{bmatrix} = \begin{bmatrix} h(0) & 0 & 0 & \dots & 0 & 0 \\ h(1) & h(0) & 0 & \dots & 0 & 0 \\ \dots & \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & 0 & \dots & h(k-1) & h(k-2) \\ 0 & 0 & 0 & \dots & 0 & h(k-1) \end{bmatrix} \begin{bmatrix} w(0) & 0 & 0 & \dots & 0 & 0 \\ w(1) & w(0) & 0 & \dots & 0 & 0 \\ \dots & \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & 0 & \dots & w(n-1) & w(n-2) \\ 0 & 0 & 0 & \dots & 0 & w(n-1) \end{bmatrix} \begin{bmatrix} c(0) \\ c(1) \\ \dots \\ c(l-1) \end{bmatrix}$$

- Multiplying input symbols by TX Eq., wc=w*c

$$\begin{bmatrix} y(0) \\ y(1) \\ \dots \\ y(l+n+k-3) \end{bmatrix} = \begin{bmatrix} h(0) & 0 & 0 & \dots & 0 & 0 \\ h(1) & h(0) & 0 & \dots & 0 & 0 \\ \dots & \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & 0 & \dots & h(k-1) & h(k-2) \\ 0 & 0 & 0 & \dots & 0 & h(k-1) \end{bmatrix} \begin{bmatrix} wc(0) \\ wc(1) \\ \dots \\ wc(n+l-1) \end{bmatrix}$$

- We desire the output vector, y, to be ISI free

$$y_{des} = \begin{cases} y_{des}(n) = 1, n = \textbf{Channel pre-cursor sample \# + Eq precursor tap \# + 1} \\ y_{des}(n) = 0, n \neq \textbf{Channel pre-cursor sample \# + Eq precursor tap \# + 1} \end{cases}$$

TX FIR Coefficient Selection

- We can calculate the error w.r.t to a desired output

$$E = Y - Y_{des} = HW_C - Y_{des} = HW - Y_{des} \textbf{ with pulse input}$$

- Squaring this error

$$\left\|E\right\|^2 = W^T H^T HW - 2Y_{des}^T HW + Y_{des}^T Y_{des}$$

- Differentiating this error to find minimum

$$\frac{d}{dW}\left\|E\right\|^2 = 2W^T H^T H - 2Y_{des}^T H = 0$$

$$W^T H^T H = Y_{des}^T H$$

- Solving for optimum TX Eq taps, W

$$\boxed{W_{ls} = \left(H^T H\right)^{-1} H^T Y_{des}}$$

- We will work some examples in a homework

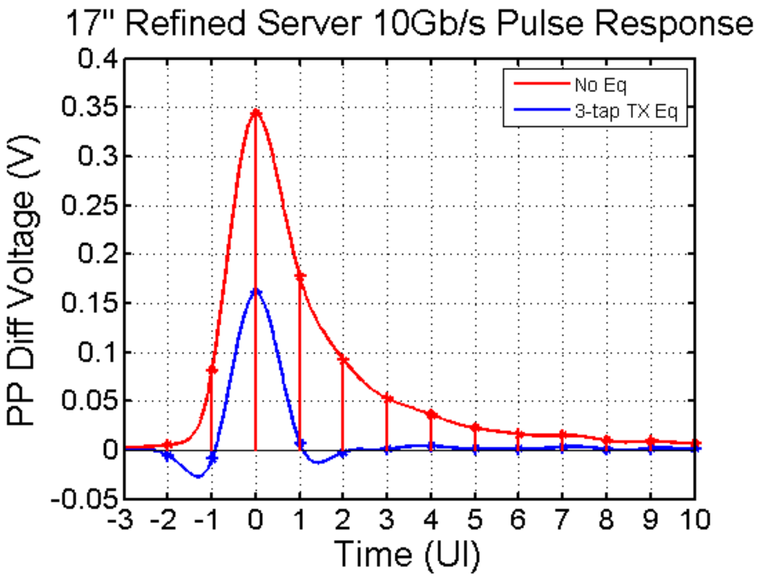
TX FIR Tap Resolution

- Using the above MMSE algorithm for the Refined Server Channel at 10Gb/s

$$W(z) = -0.131 + 0.595z^{-1} - 0.274z^{-2}$$

$$\begin{bmatrix} 1pre & main & 1post \end{bmatrix}$$

$$\begin{bmatrix} -0.131 & 0.595 & -0.274 \end{bmatrix}$$

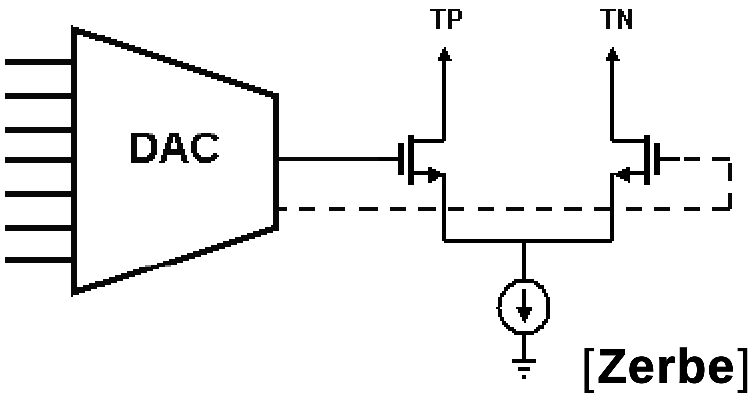


- Generally, TX DAC resolution is limited to between 4 to 6bits
- Mapping these equalization coefficients with this resolution may impact performance

TX FIR Circuit Architectures

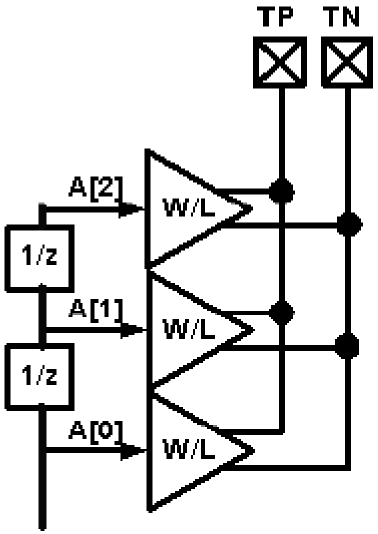
- Segmented DAC vs Direct FIR
- Segmented DAC
  - Minimum sized output transistors to handle peak output current
  - Lowest output capacitance
  - Most power & complexity
    - Need mapping table (RAM)
    - Very flexible in equalization
- Direct FIR
  - Parallel output drivers for output taps
  - Each parallel driver must be sized to handle its potential maximum current
  - Lower power & complexity
  - Higher output capacitance

Segmented DAC



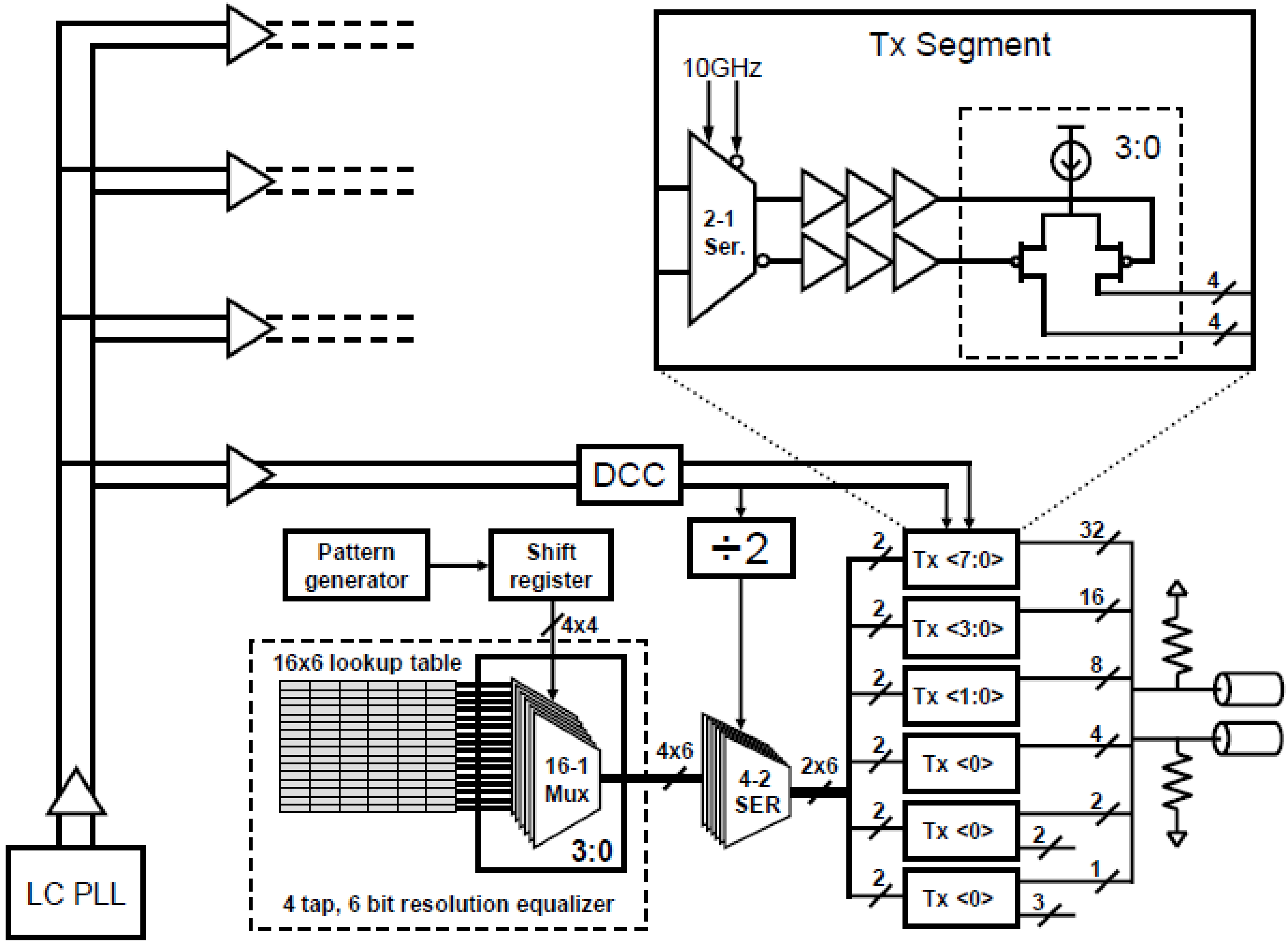
[Zerbe]

Direct FIR



[Zerbe]

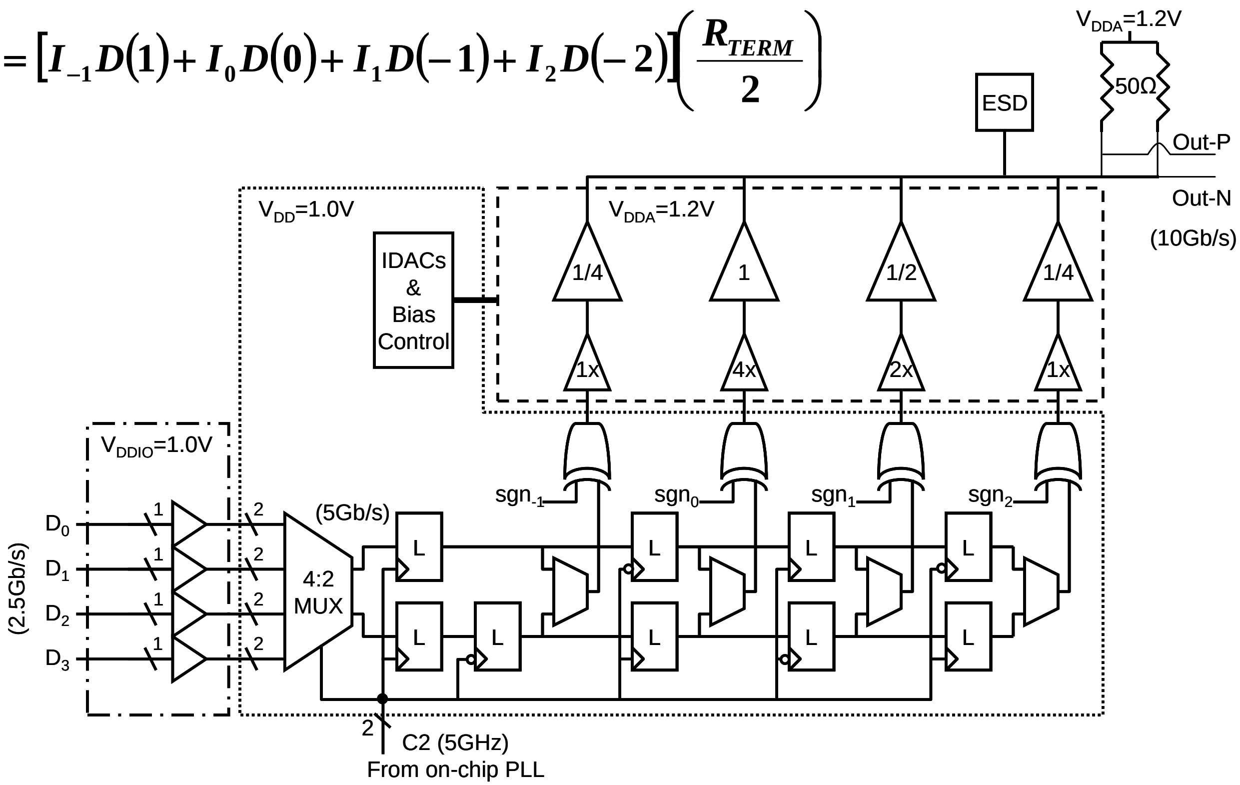
Segmented DAC Example



[Casper ISSCC 2006]

Direct FIR Equalization

$$V_{out}(0) = \left[I_{-1}D(1) + I_0 D(0) + I_1 D(-1) + I_2 D(-2)\right]\left(\frac{R_{TERM}}{2}\right)$$



"A Low Power 10Gb/s Serial Link Transmitter in 90-nm CMOS," A. Rylyakov et al., CSICS 2005

Next Time

- RX FIR
- RX CTLE
- RX DFE
- Alternate/Future Approaches