ECEN689: Special Topics in High-Speed Links Circuits and Systems Spring 2010

Lecture 15: RX Circuits

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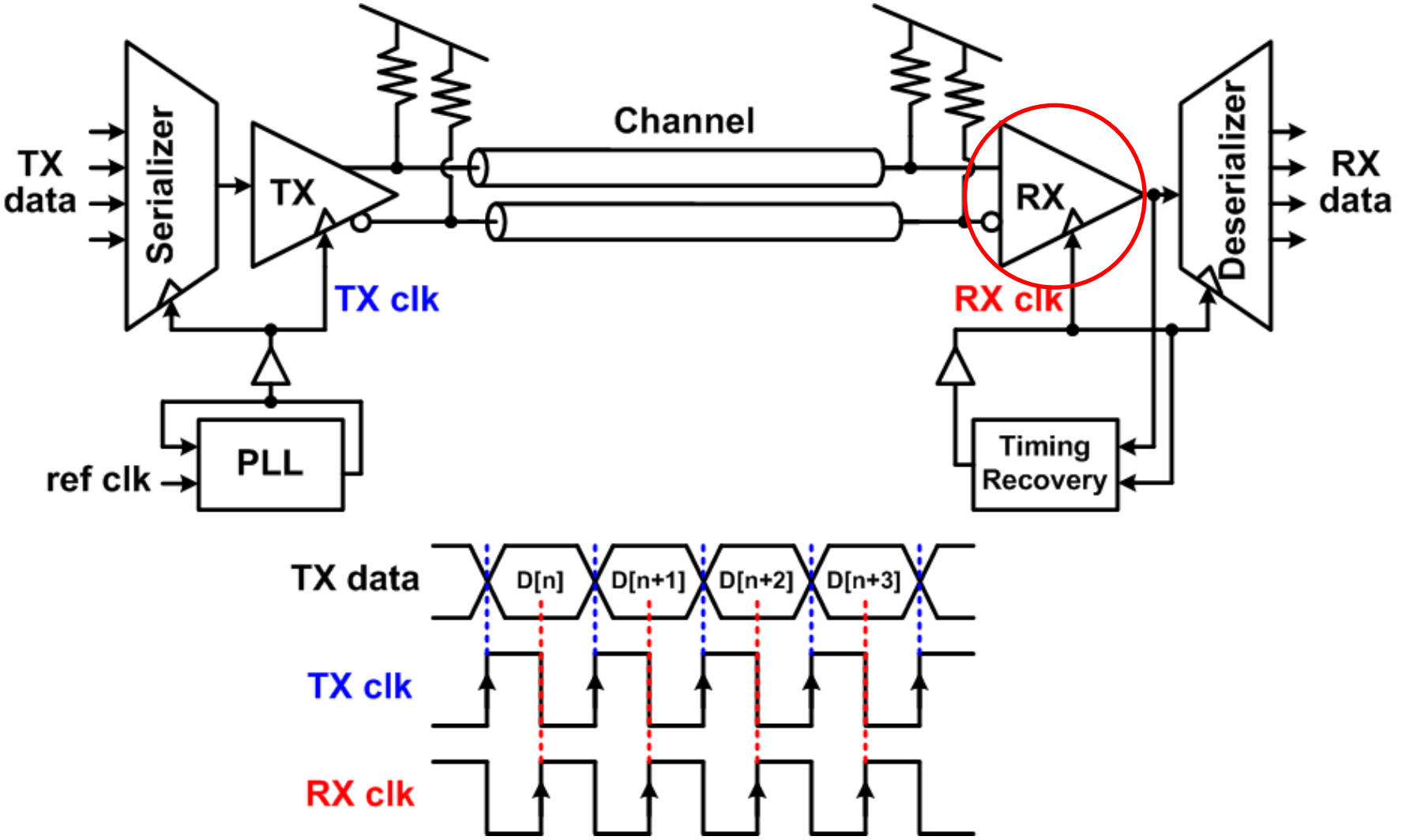
Announcements

- HW4 due Wednesday 5PM
  - Involves transistor-level circuit design
  - Use 90nm or more advanced CMOS technology
  - Instructions on how to access 90nm CMOS models on website for students who don't already have access to a design kit
- Exam 1 is March 12
  - 9:10-10:10AM (10 extra minutes)
  - Closed book w/ one standard note sheet
    - 8.5"x11" front & back
  - Bring your calculator
- Reading
  - Dally 11.1-11.3
  - Papers posted on TX drivers and RX comparator analysis

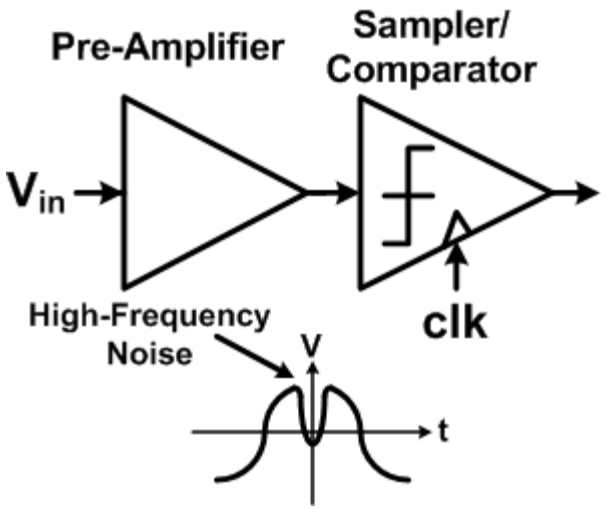
Agenda

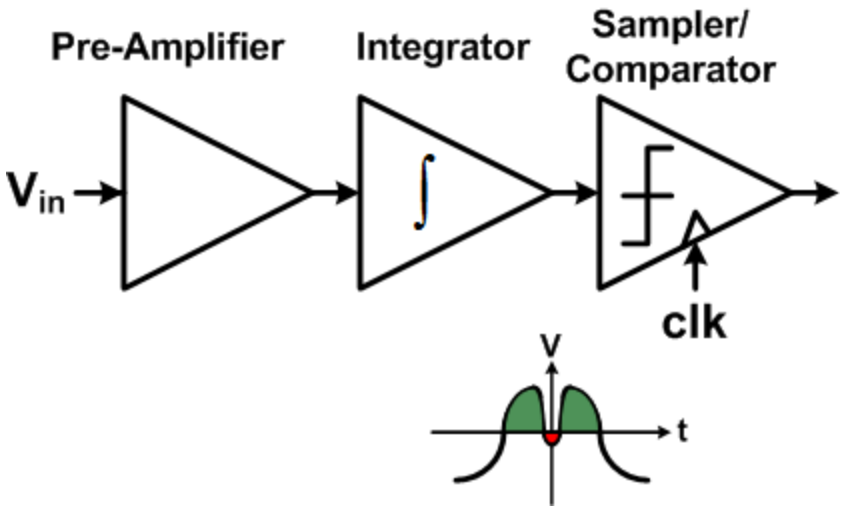
- RX Circuits
  - Integrating receivers
  - RX sensitivity
    - Offset correction
  - Demultiplexing receivers

High-Speed Electrical Link System



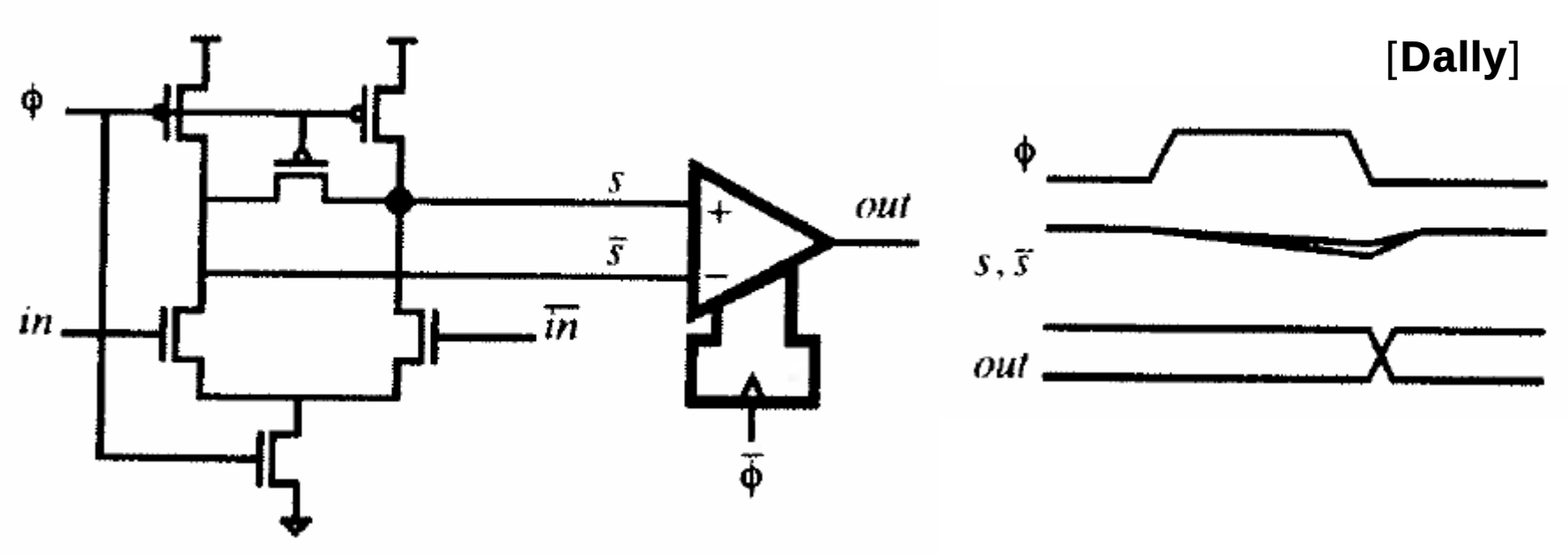
Integrating RX & High-Frequency Noise





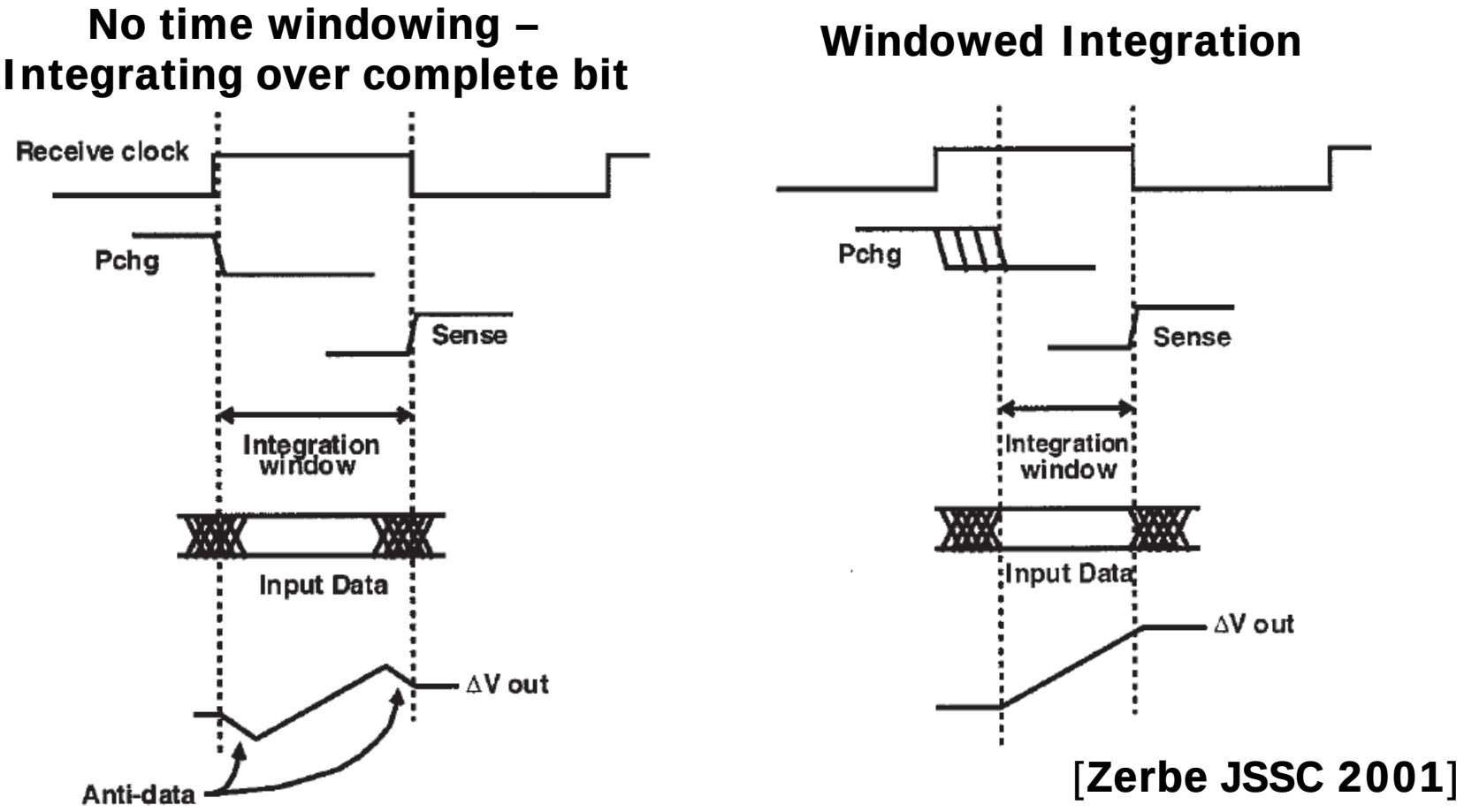
- A small aperture time is desired in most receiver samplers
- However, high-frequency noise can degrade performance at sampling time
  - Can be an issue in single-ended systems with excessive LdI/dt switching noise
- Integrating the input signal over a sampling interval reduces the high-frequency noise impact

Integrating Amplifier



- Differential input voltage converted to a differential current that is integrated on the sense nodes' capacitance

Windowed Integration



[**Zerbe JSSC 2001**]

- Windowing integration time can minimize transition noise and maximize integration of valid data

RX Sensitivity

- RX sensitivity is a function of the input referred noise, offset, and minimum latch resolution voltage

$$v_S^{pp} = 2v_n^{rms}\sqrt{SNR} + v_{\min} + v_{offset*}$$

- Gaussian (unbounded) input referred noise comes from input amplifiers, comparators, and termination
  - A minimum signal-to-noise ratio (SNR) is required for a given bit-error-rate (BER)

$$\textbf{For BER} = 10^{-12}\ (\sqrt{\text{SNR}} = 7)$$

- Minimum latch resolution voltage comes from hysteresis, finite regeneration gain, and bounded noise sources

$$\textbf{Typical}\ v_{\min} < 5mV$$

- Input offset is due to circuit mismatch (primarily V_{th} mismatch) & is most significant component if uncorrected

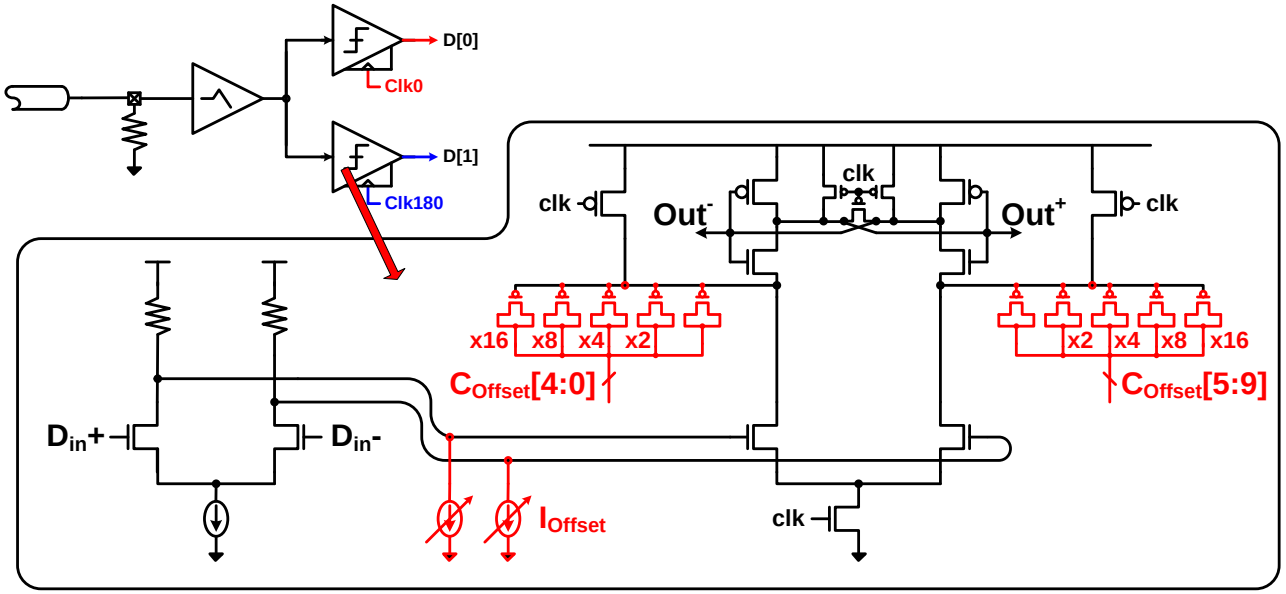
RX Sensitivity & Offset Correction

- RX sensitivity is a function of the input referred noise, offset, and min latch resolution voltage

$$v_S^{pp} = 2v_n^{rms}\sqrt{SNR} + v_{\min} + v_{offset*} \qquad \textbf{Typical Values}: v_n^{rms} = 1mV_{rms},\ v_{\min} + v_{offset*} < 6mV$$

$$\textbf{For BER} = 10^{-12}\ (\sqrt{\text{SNR}} = 7) \Rightarrow v_S^{pp} = 20mV_{pp}$$

- Circuitry is required to reduce input offset from a potentially large uncorrected value (>50mV) to near 1mV



Input Referred Offset

- The input referred offset is primarily a function of V_{th} mismatch and a weaker function of β (mobility) mismatch

$$\sigma_{V_t} = \frac{A_{V_t}}{\sqrt{WL}}, \quad \sigma_{\Delta\beta/\beta} = \frac{A_\beta}{\sqrt{WL}}$$

- To reduce input offset 2x, we need to increase area 4x
  - Not practical due to excessive area and power consumption
  - Offset correction necessary to efficiently achieve good sensitivity
- Ideally the offset "A" coefficients are given by the design kit and Monte Carlo is performed to extract offset sigma
- If not, here are some common values:
  - A_{Vt} = 1mVμm per nm of t_{ox}
    - For our default 90nm technology, t_{ox}=2.8nm $\rightarrow$ A_{Vt} ~2.8mVμm
  - A_β is generally near 2%μm

Offset Correction Range & Resolution

- Generally circuits are designed to handle a minimum variation range of $\pm 3\sigma$ for 99.7% yield
  - Example: Input differential transistors W=4μm, L=150nm

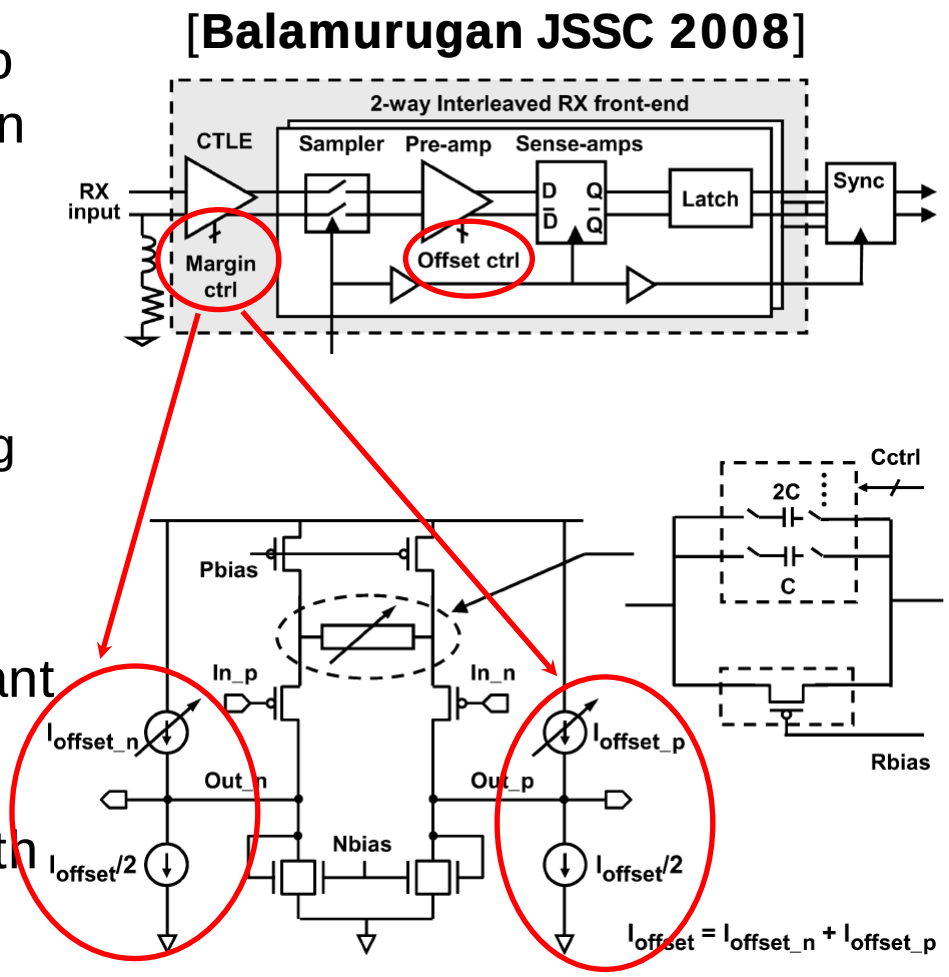
$$\sigma_{V_t} = \frac{A_{V_t}}{\sqrt{WL}} = \frac{2.8mV\mu m}{\sqrt{4\mu m \cdot 150nm}} = 3.6mV, \quad \sigma_{\Delta\beta/\beta} = \frac{A_\beta}{\sqrt{WL}} = \frac{2\%\mu m}{\sqrt{4\mu m \cdot 150nm}} = 2.6\%$$

- If we assume (optimistically) that the input offset is only dominated by the input pair V_t mismatch, we would need to design offset correction circuitry with a range of about ±11mV
- If we want to cancel within 1mV, we would need an offset cancellation resolution of 5bits, resulting in a worst-case offset of

$$1LSB = \frac{\textbf{Offset Correction Range}}{\mathbf{2^{Resolution}} - 1} = \frac{22mV}{2^5 - 1} = 0.65mV$$

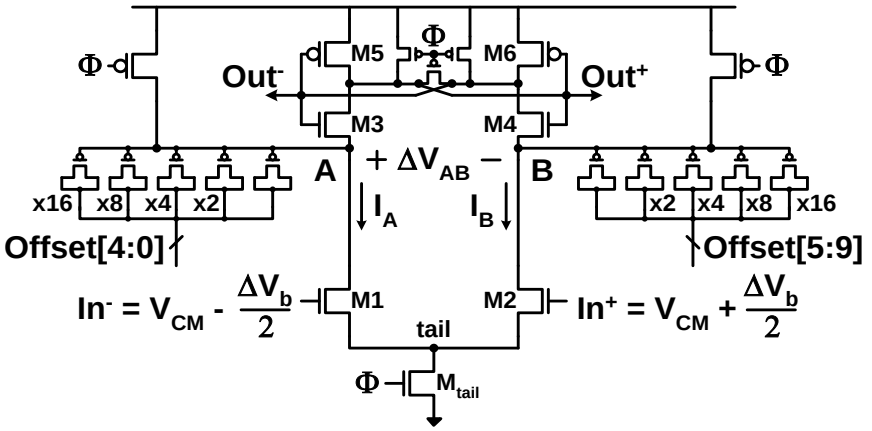
Current-Mode Offset Correction Example

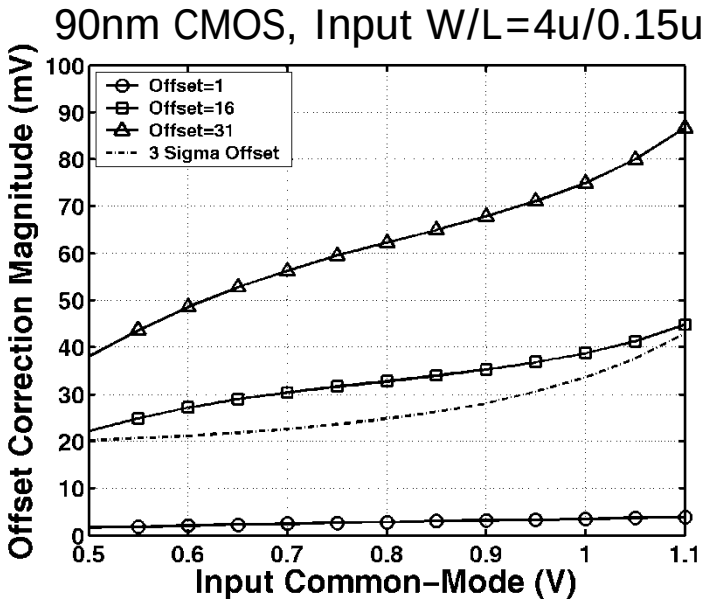
- Differential current injected into input amplifier load to induce an input-referred offset that can cancel the inherent amplifier offset
  - Can be made with extended range to perform link margining
- Passing a constant amount of total offset current for all the offset settings allows for constant output common-mode level
- Offset correction performed both at input amplifier and in individual receiver segments of the 2-way interleaved architecture



Capacitive Offset Correction Example

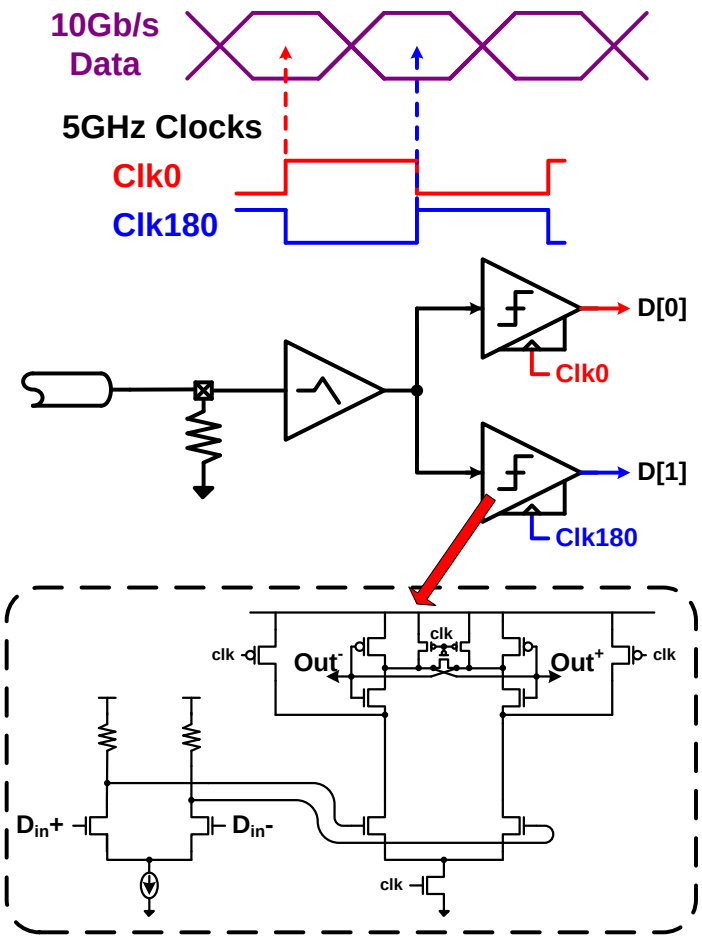
- A capacitive imbalance in the sense-amplifier internal nodes induces an input-referred offset
- Pre-charges internal nodes to allow more integration time for more increased offset range
- Additional capacitance does increase sense-amp aperture time
- Offset is trimmed by shorting inputs to a common-mode voltage and adjusting settings until an even distribution of “1”s and “0”s are observed
- Offset correction settings can be sensitive to input common-mode



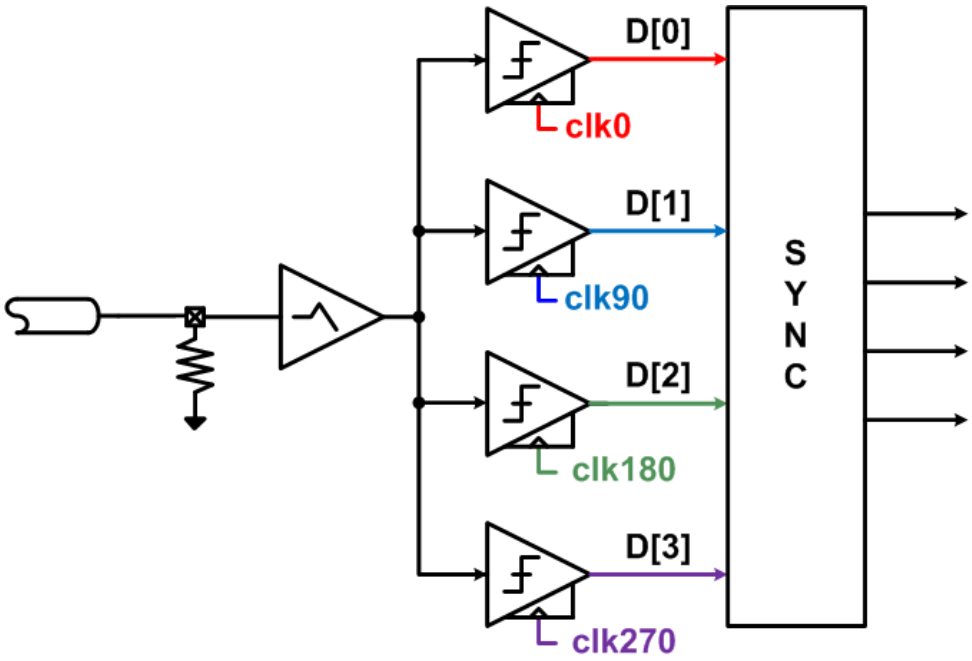


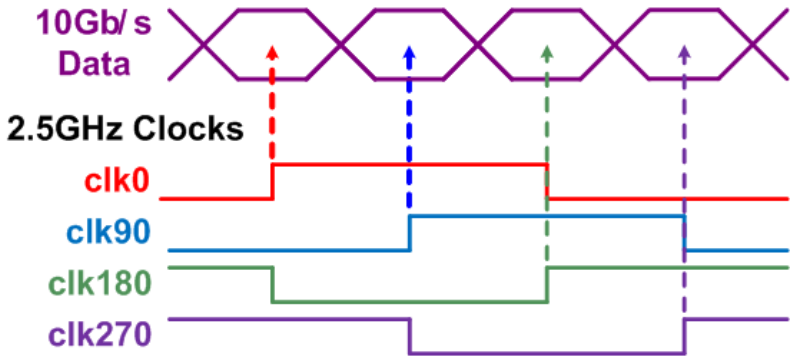
Demultiplexing RX

- Demultiplexing allows for lower clock frequency relative to data rate
- Gives extra regeneration and pre-charge time in comparators
- Need precise phase spacing, but not as sensitive to duty-cycle as TX multiplexing



1:4 Demultiplexing RX Example

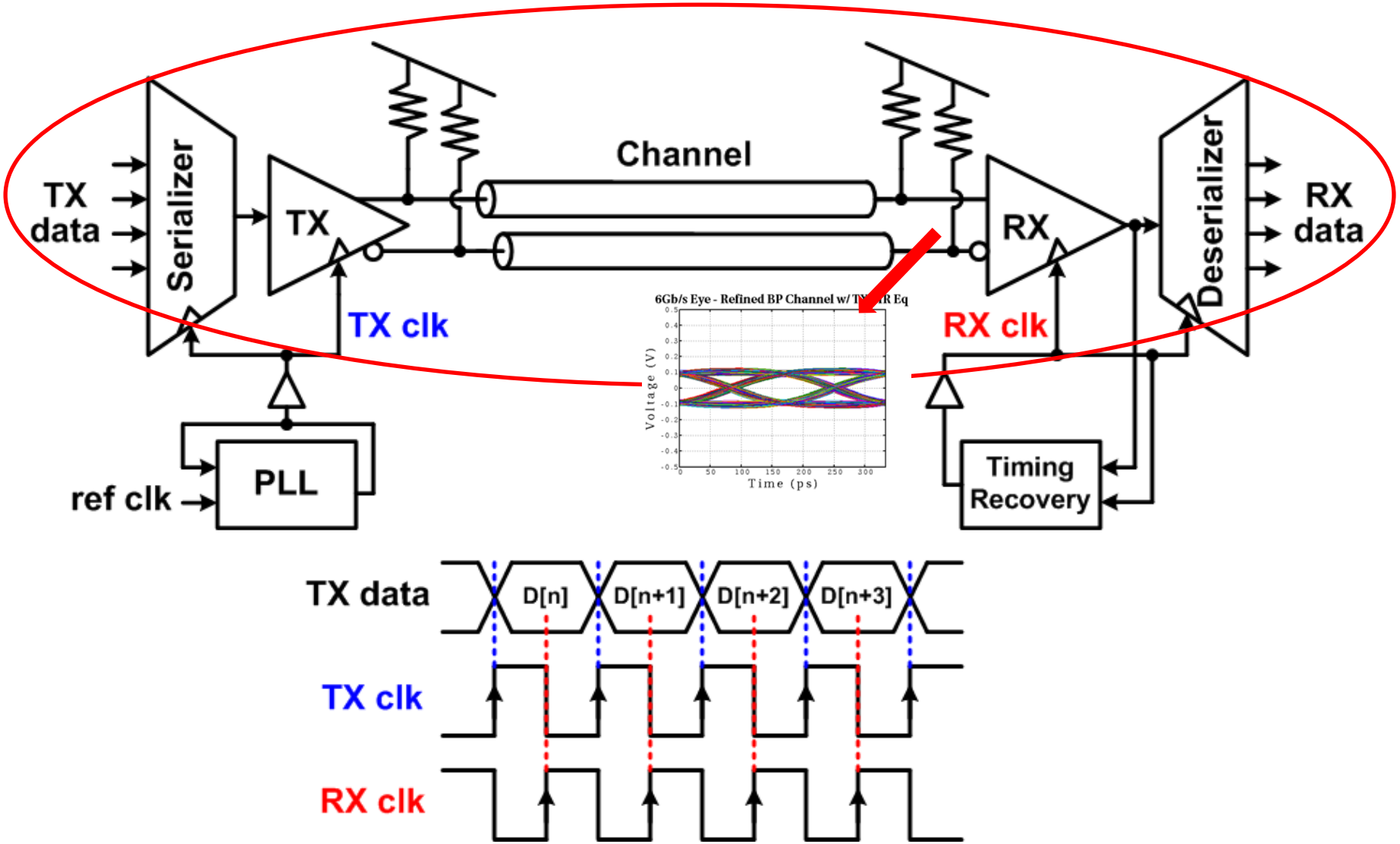




- Increased demultiplexing allows for higher data rate at the cost of increased input or pre-amp load capacitance
- Higher multiplexing factor more sensitive to phase offsets in degrees

End Exam 1 Material

High-Speed Electrical Link System



Next Time

- Equalization theory and circuits
  - Equalization overview
  - Equalization implementations
    - TX FIR
    - RX FIR
    - RX CTLE
    - RX DFE
  - Setting coefficients
  - Equalization effectiveness
  - Alternate/future approaches