ECEN720: High-Speed Links Circuits and Systems Spring 2025

Lecture 14: Clock Distribution Techniques

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Announcements

- Project Final Report due Apr 29

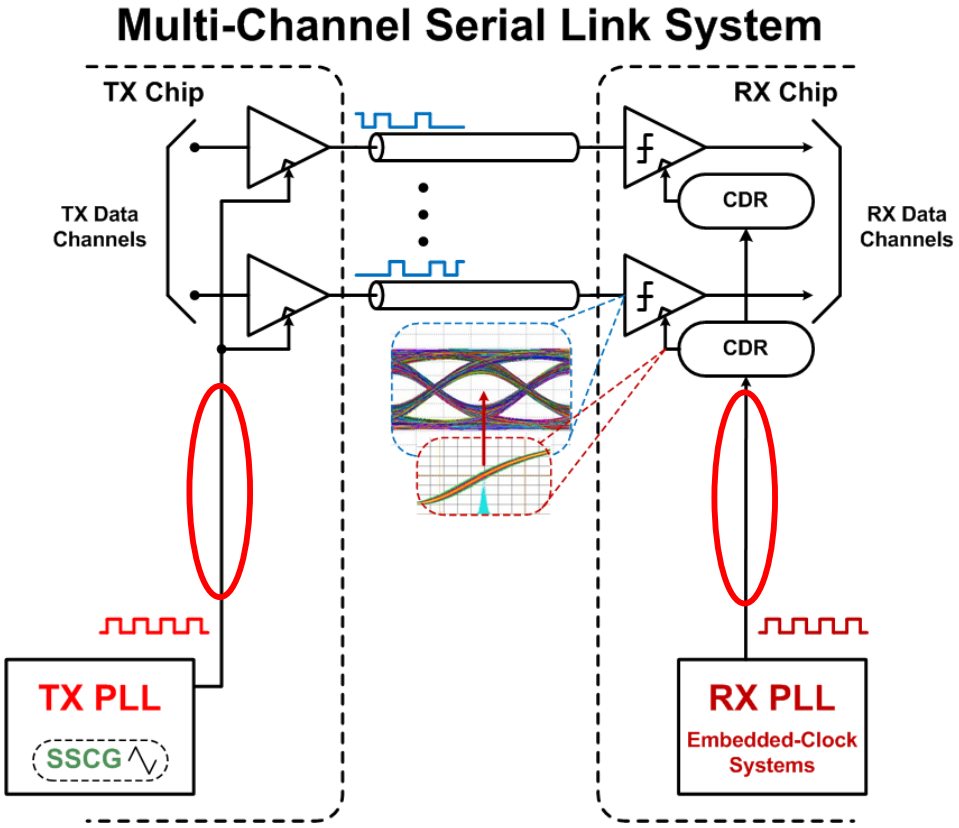
- Exam 2 May 2
  - 1PM-3PM for in-person sections
  - Focuses on material from Lectures 7-15
  - Previous years' Exam 2s are posted on the website for reference

Agenda

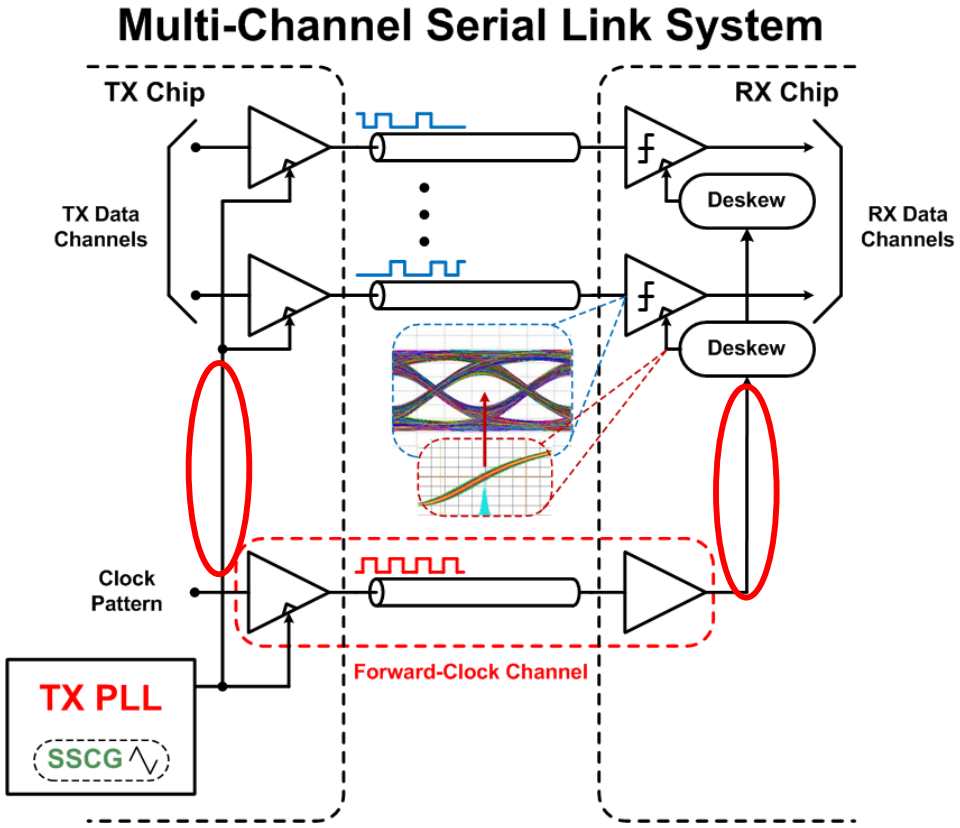
- Wire Scaling
- Clock Distribution
- CML2CMOS Converters
- Multi-Phase Generation
- Multi-Phase Calibration

Clock Distribution in Serial I/O Systems

Embedded Clock System



Forwarded Clock System



- On-die global clock distribution is necessary in multi-channel embedded and fowarded clock serial link systems

VLSI Interconnect (Wires)

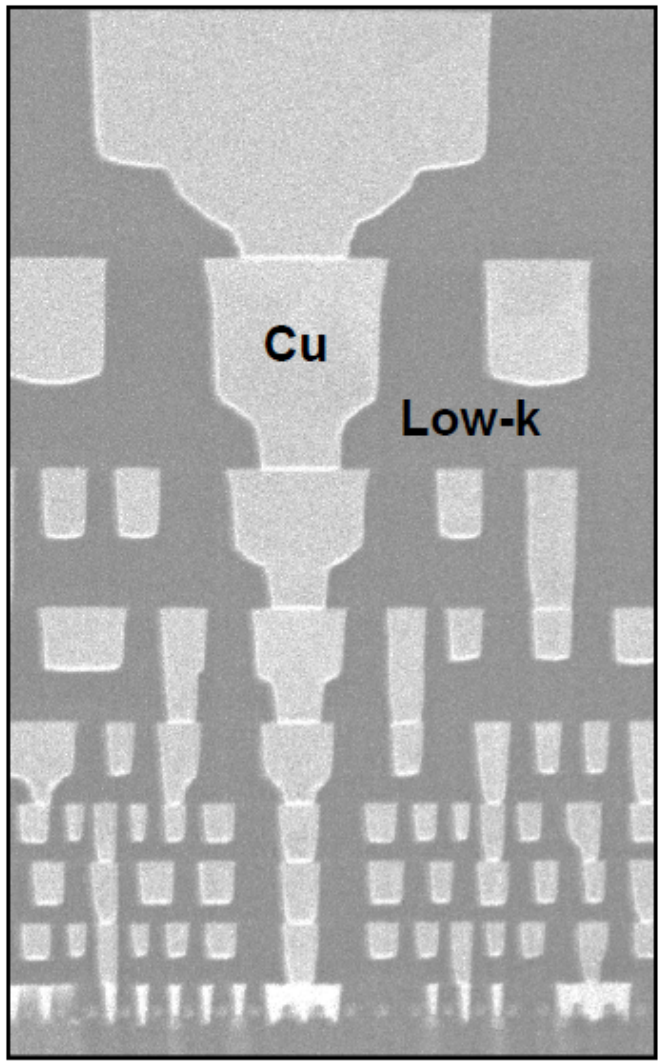
Loose pitch + thick metal on upper layers

- High speed global wires
- Low resistance power grid

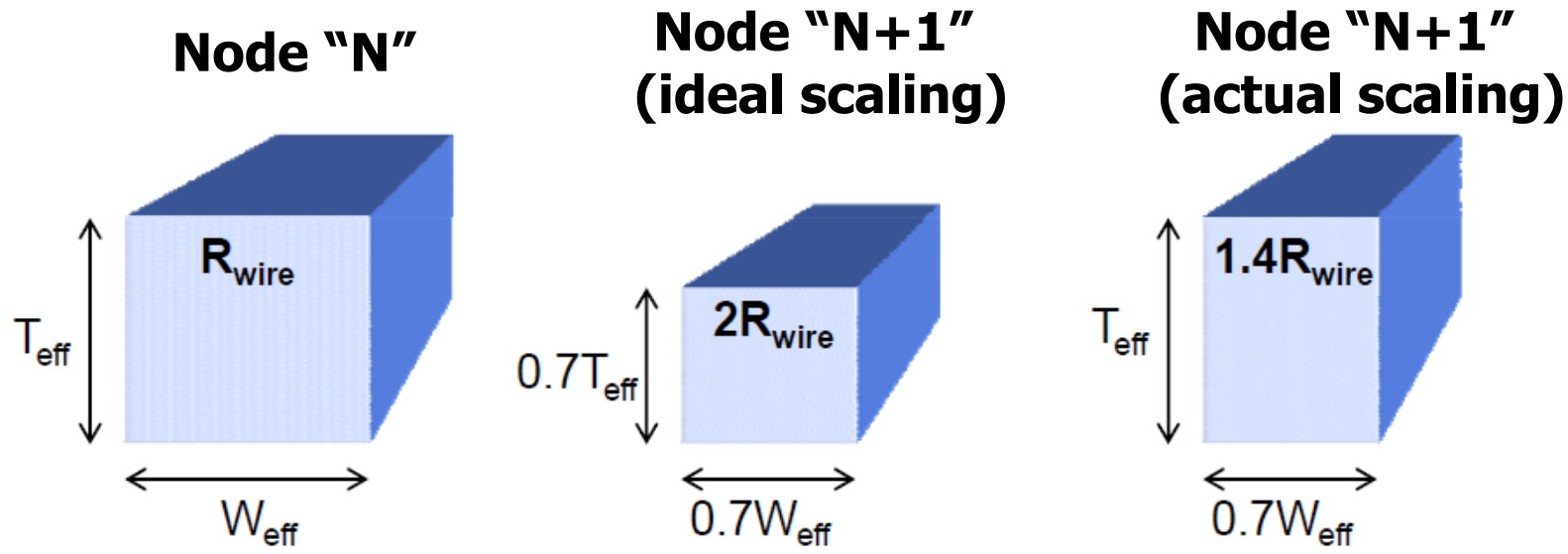
Tight pitch on lower layers

- Maximum density for local interconnects

[Bohr ISSCC 2009]



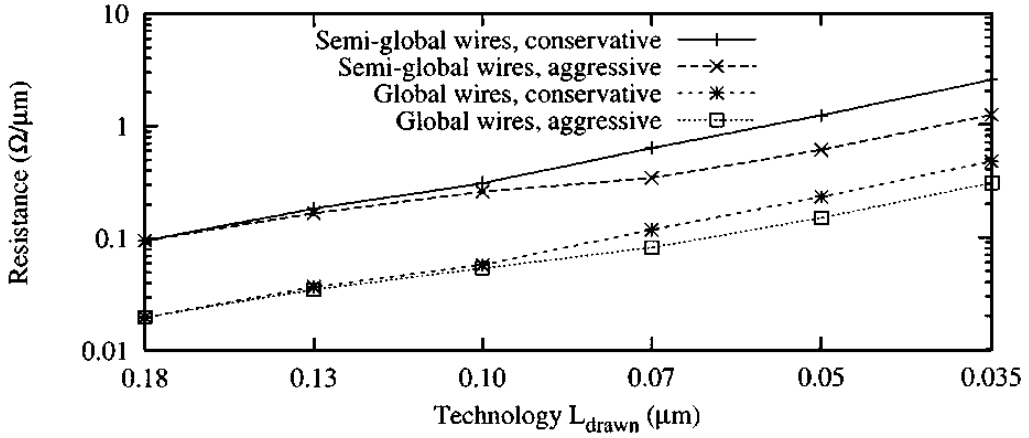
Wire Scaling

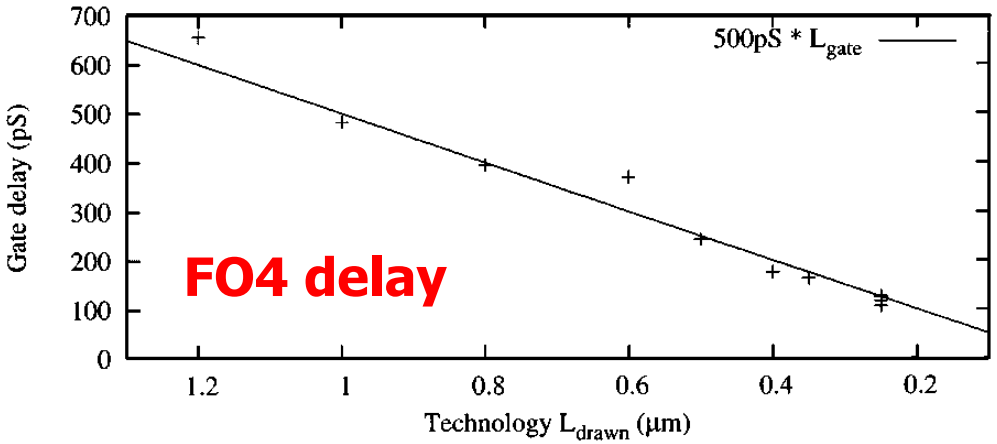


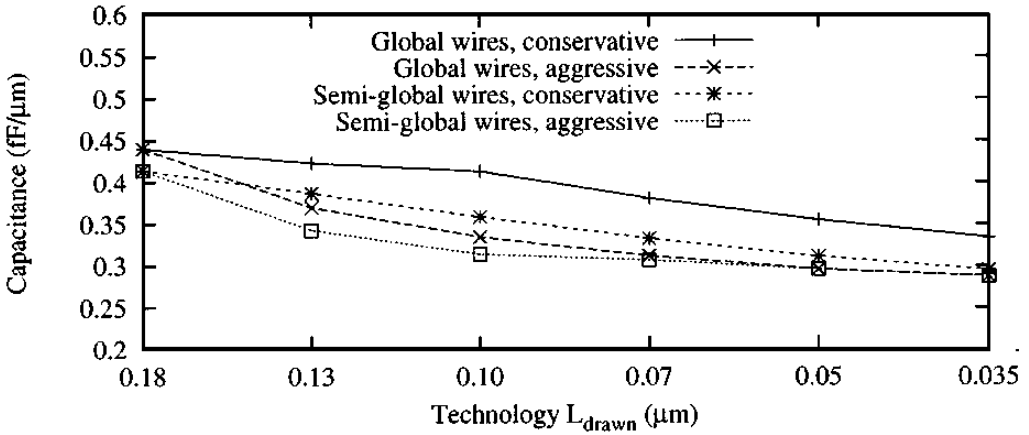
[Ho]

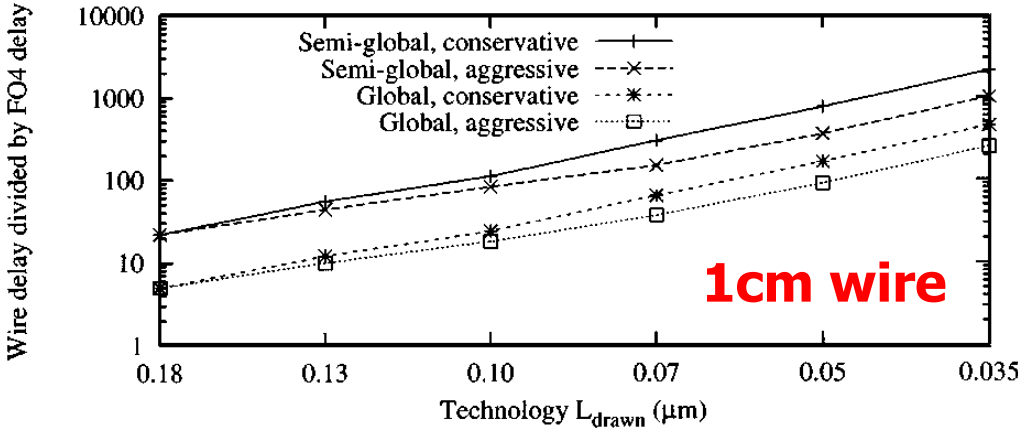
- Ideally, we scale everything by 0.7x when we move to a more advanced technology node for 2x density
- Results in 2x wire resistance, which dramatically increases wire RC delay
  - To compensate resistance wires get taller
- Cap grows at a smaller pace with scaling
  - Taller wires increase sidewall cap
  - Improved (low-k) dielectrics help reduce cap

Wire Scaling - Delay





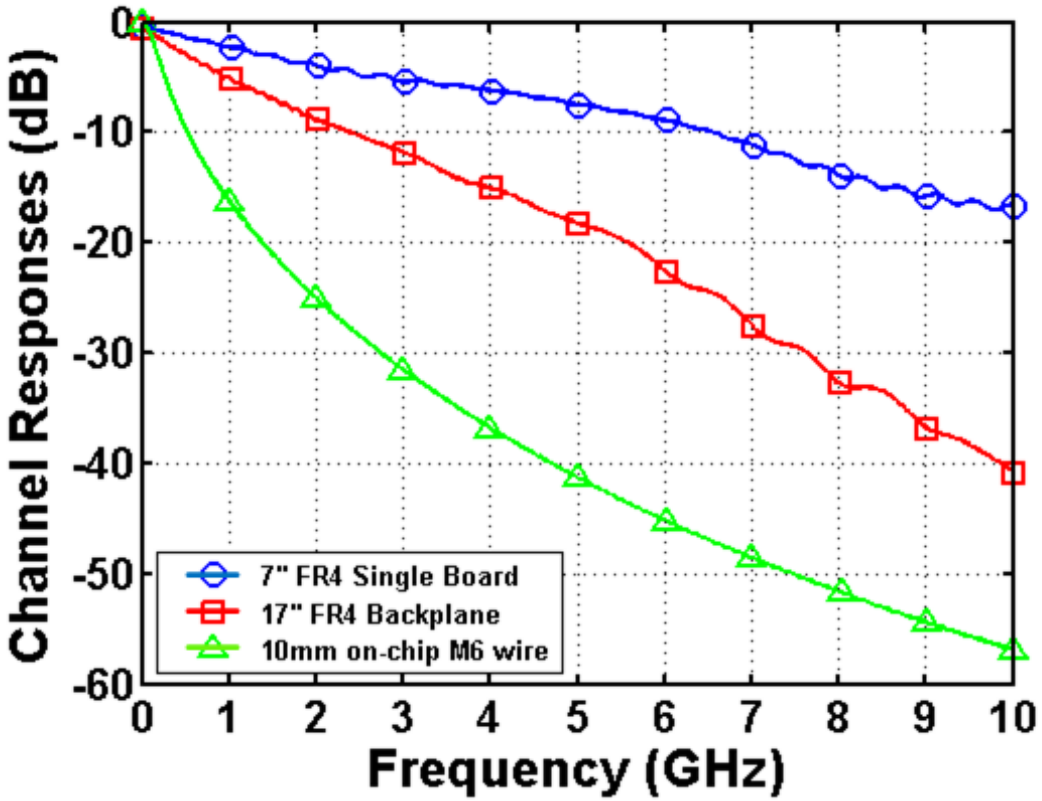




[Ho Proc. IEEE 2001]

- Global on-chip wire RC delay becomes many (100+) gate delays (if driven w/ one lumped driver)

Limited Wire Bandwidth



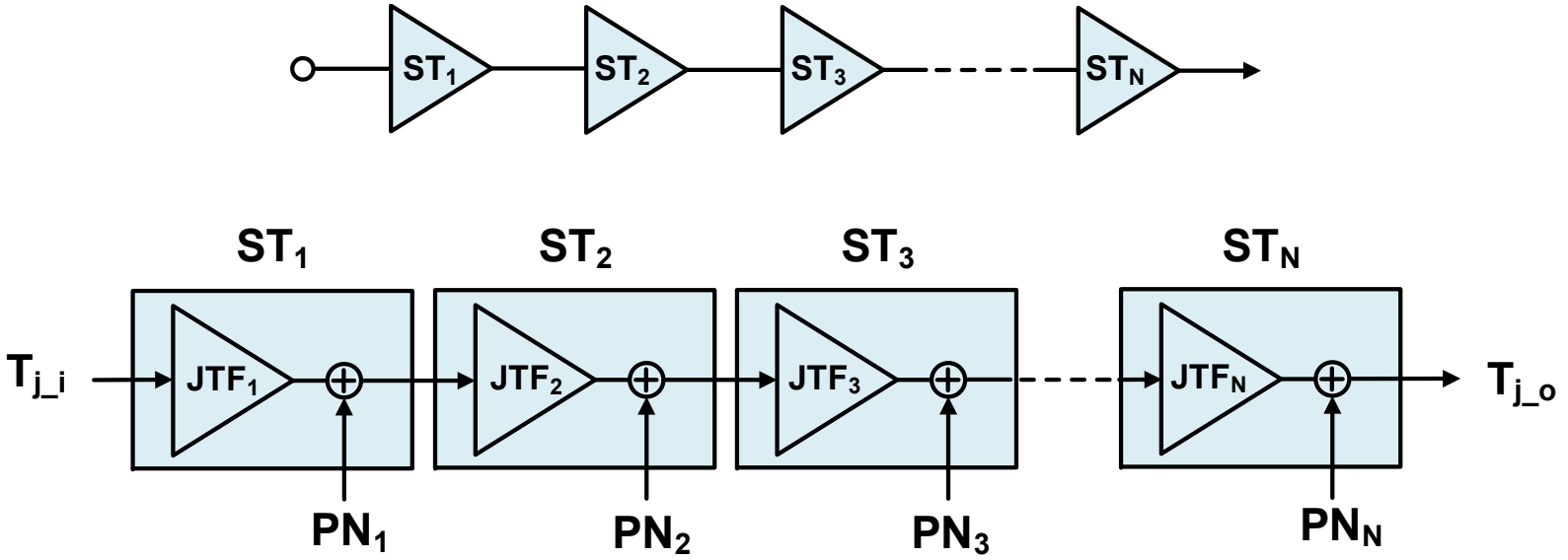
- Global on-chip wire bandwidth is much worse than chip-to-chip channels
- RC-dominated on-chip wires vs (R)LC-dominated off-chip wires

Agenda

- Wire Scaling
- Clock Distribution
- CML2CMOS Converters
- Multi-Phase Generation
- Multi-Phase Calibration

Cascaded Clock Buffers

[**Kim ISSCC 2019**]

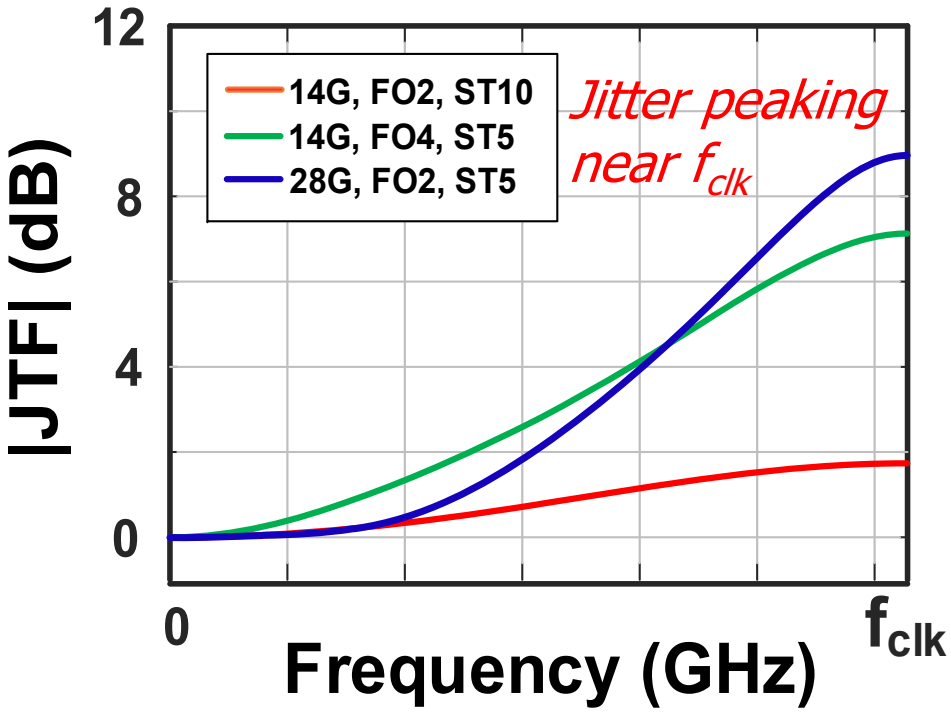


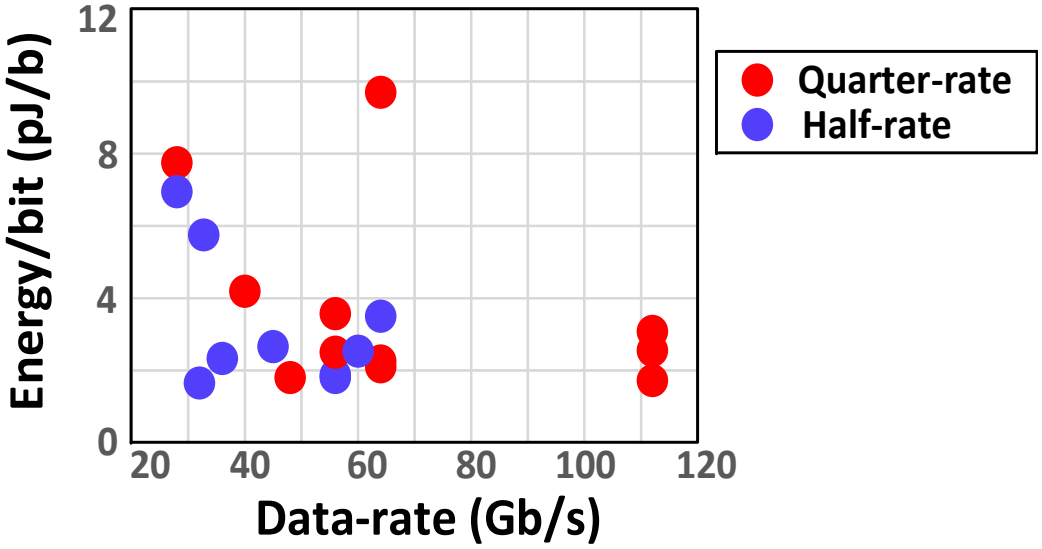
$$T_{j\_o}=(\ldots (((T_{j\_i} * JTF_1) + PN_1) * JTF_2) + PN_2) * \ldots) * JTF_N) + PN_N$$

- Total output jitter in frequency domain can be obtained from per-stage JTFs and phase noise (PN)

Clock Buffer Jitter Transfer Function

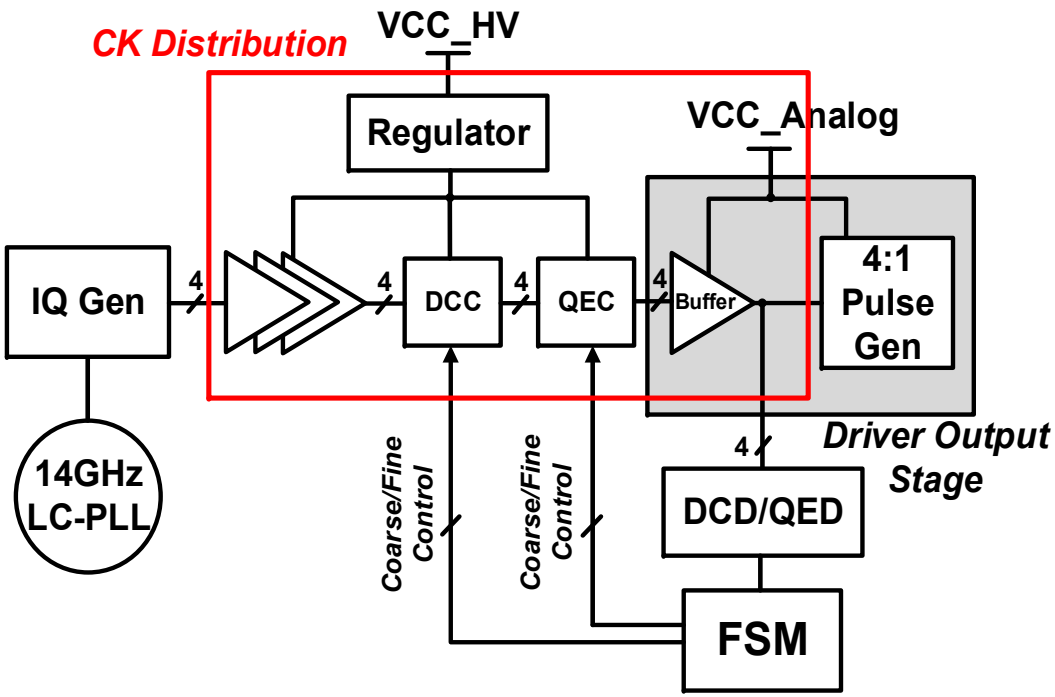
[Kim ISSCC 2019]



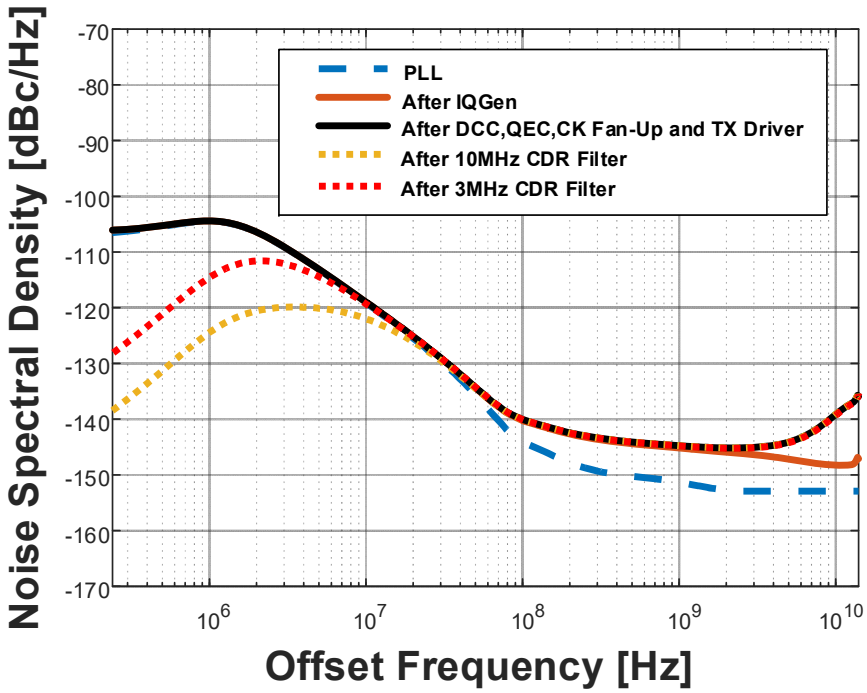


- Significant jitter amplification at 28GHz in the clock distribution chain
- Motivates most 112Gb/s systems to use a quarter-rate clocking scheme with 14GHz clocks
- Quadrature phase spacing and duty cycle correction is necessary for uniform output eyes

14GHz Quadrature Clock Distribution



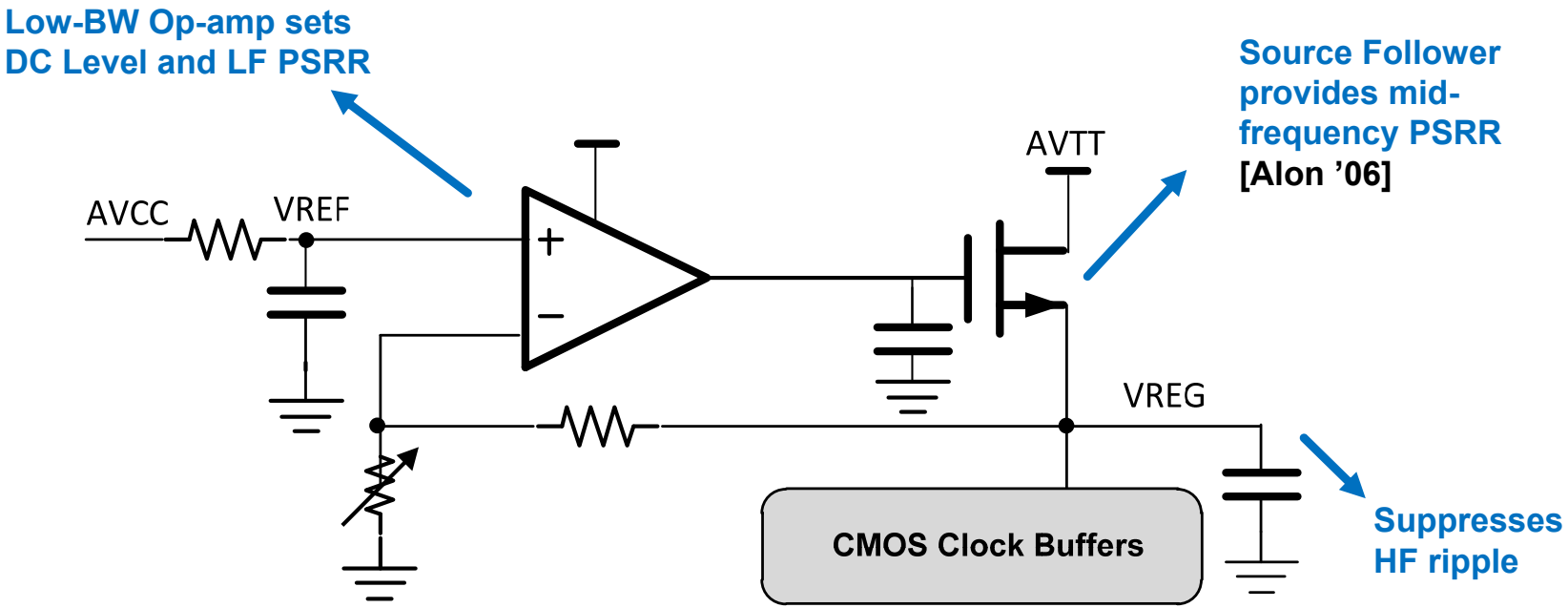
[Kim ISSCC 2019]



- PLL output phase noise is multiplied by clock distribution JTF
- CDR filter (high-pass) is applied to get the untracked effective TX jitter

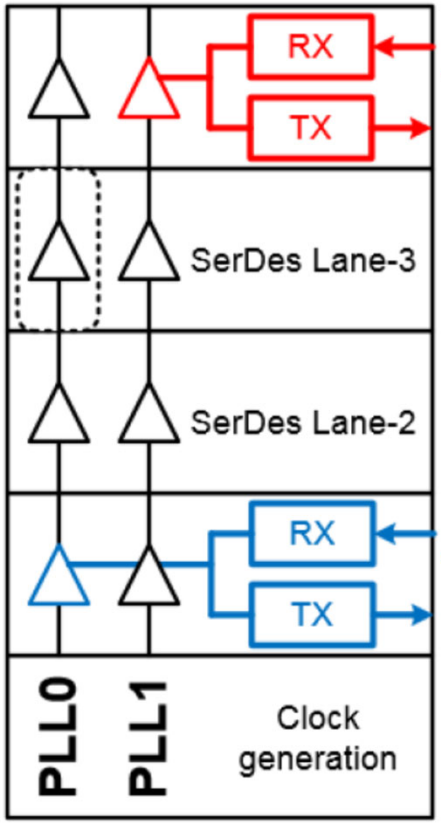
208fs$_{rms}$ w/ 3MHz CDR BW
185fs$_{rms}$ w/ 10MHz CDR BW

Clock Distribution Regulation

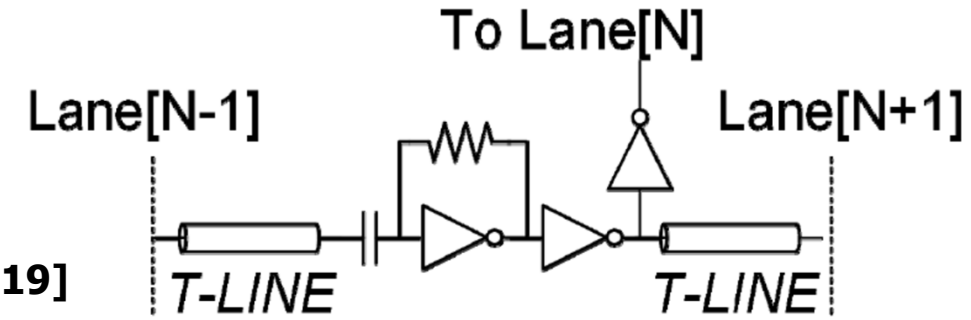


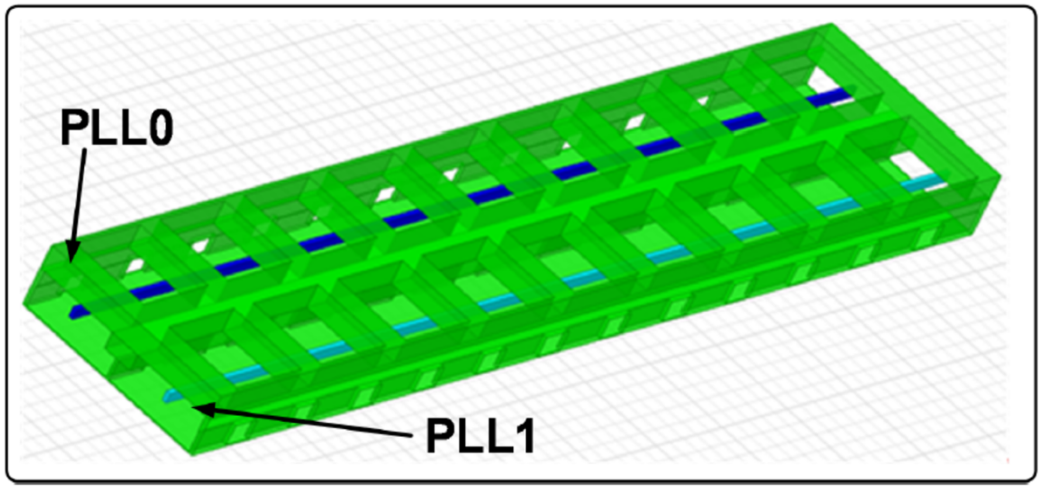
[Turker ISSCC 2019]

Huawei 60Gb/s PAM4 Clock Distribution



[LaCroix ISSCC 2019]

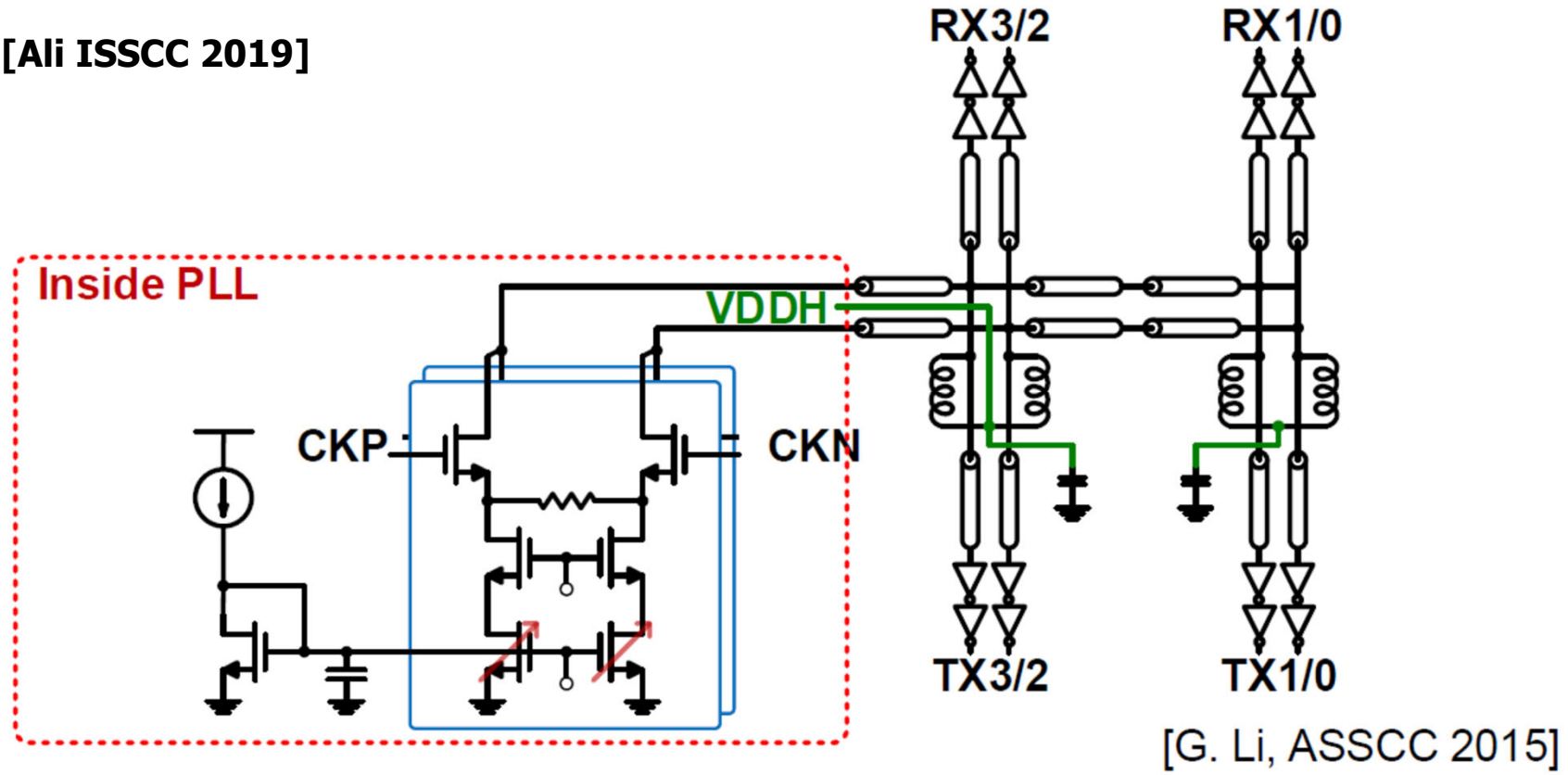




- Wideband ½-rate single-ended clock distribution (2-16GHz)
- 2 independent data rates possible per 4-lane macro
- LDO-powered CMOS inverter-based distribution
- Metal shield around distribution wires to lower crosstalk

Mediatek 56Gb/s PAM4 Clock Distribution

[Ali ISSCC 2019]

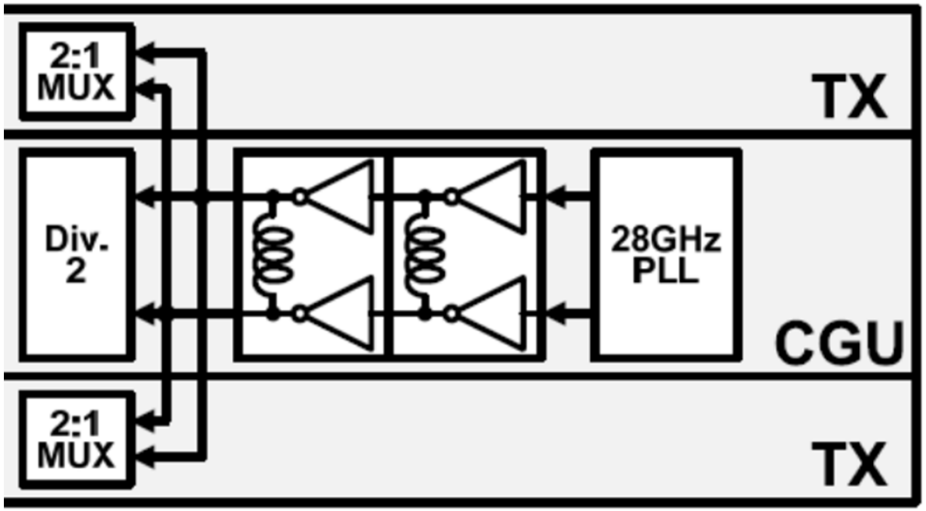


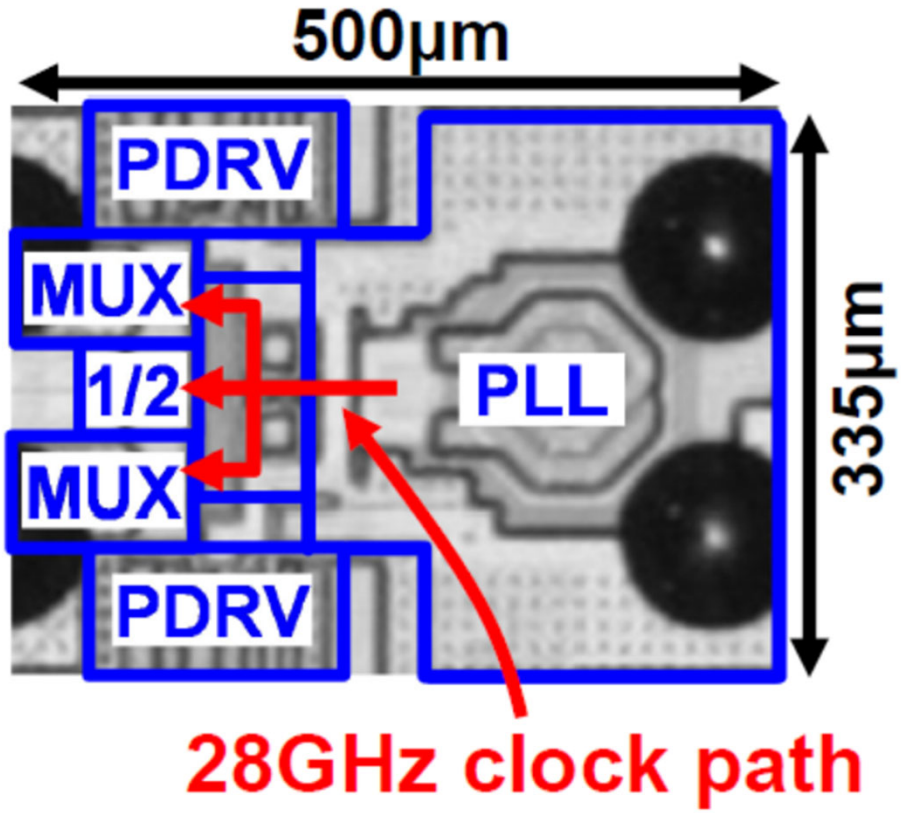
[G. Li, ASSCC 2015]

- Tuned standing-wave clock distribution
- Two shunt inductors placed in the middle set boundary conditions for the transmission line and tune nearly equal amplitude at the drop points

Inductive-Loaded Clock Distribution

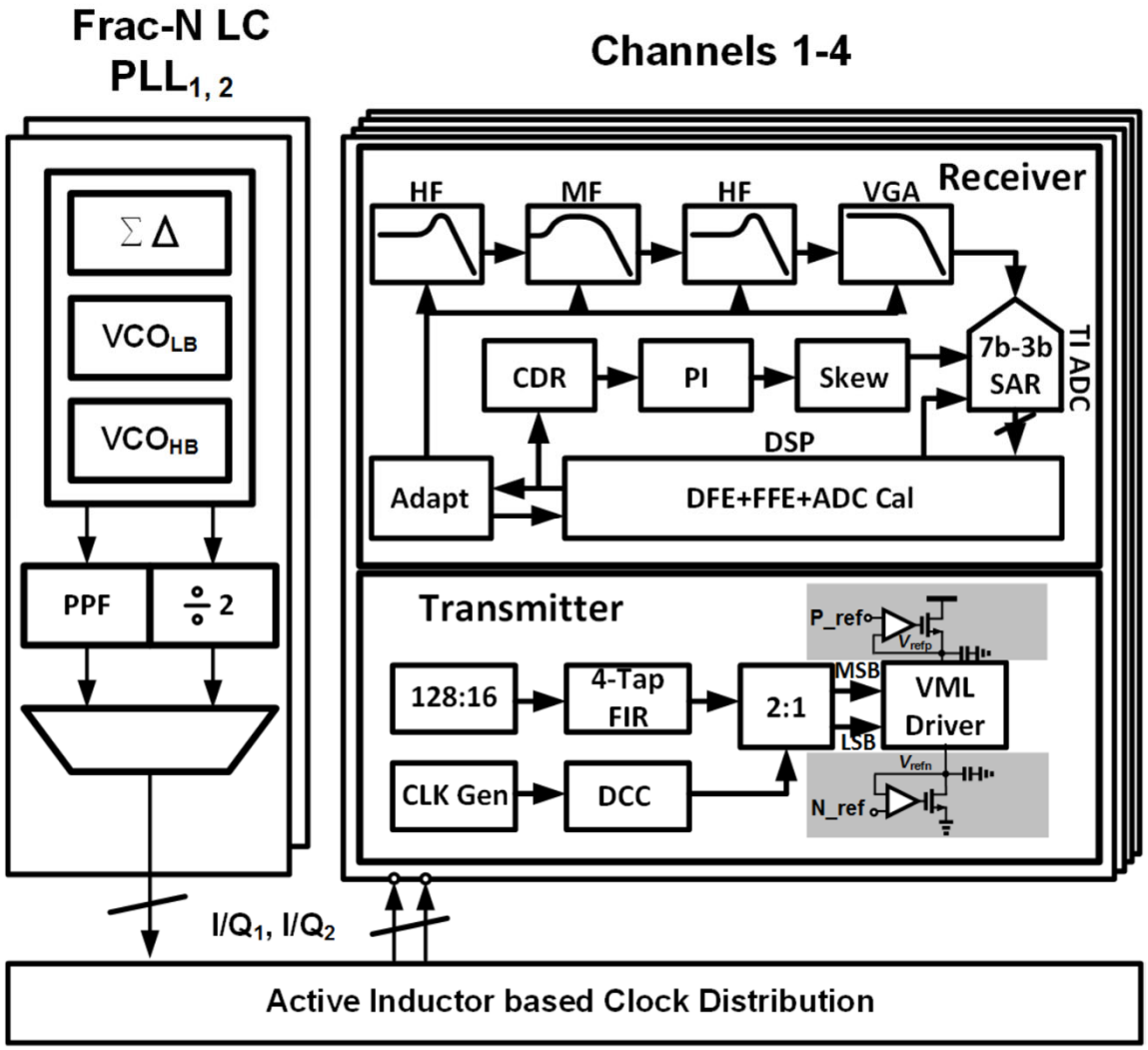
[Shibasaki ISSCC 2016]



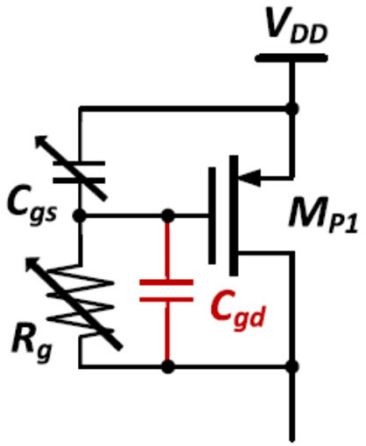


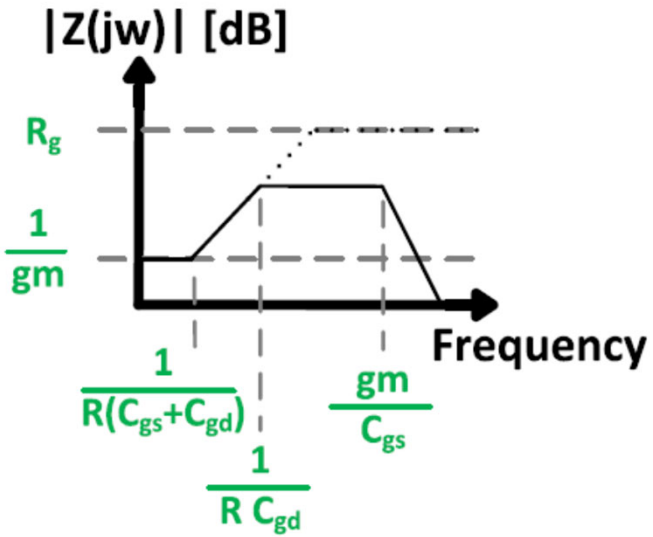
- 2-stage narrow-band buffer drives 2-lane 2:1 MUXs and divider
- Minimal length 28GHz clock path

Active-Inductor-Based Clock Distribution



Active Inductor CML Load





[Upadhyaya ISSCC 2018]

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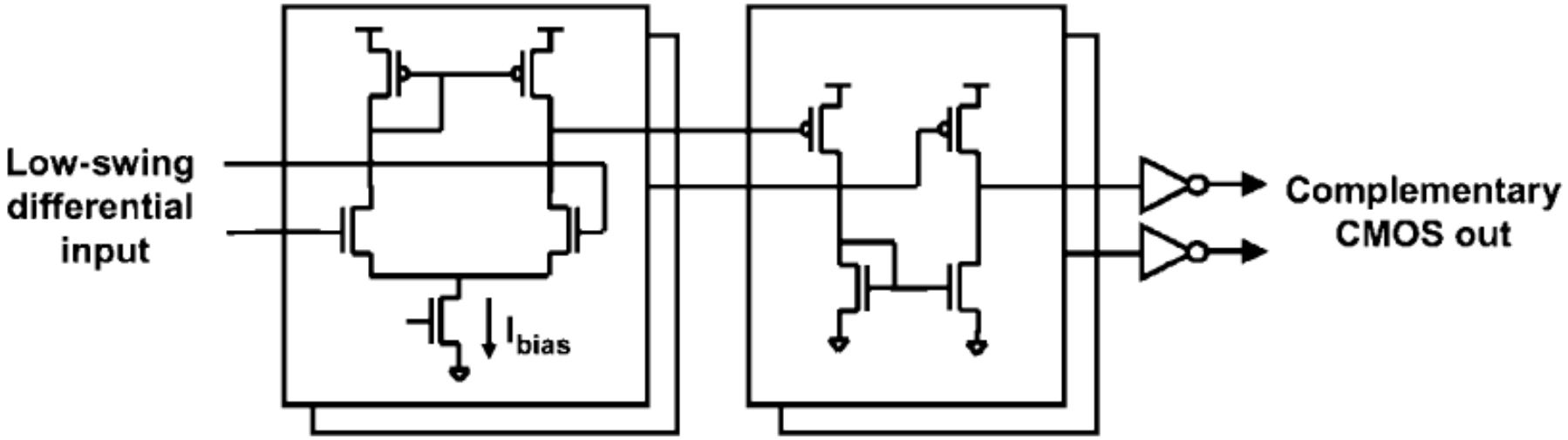
- CML2CMOS Converters
- Multi-Phase Generation
- Multi-Phase Calibration

CML2CMOS Converter (1)

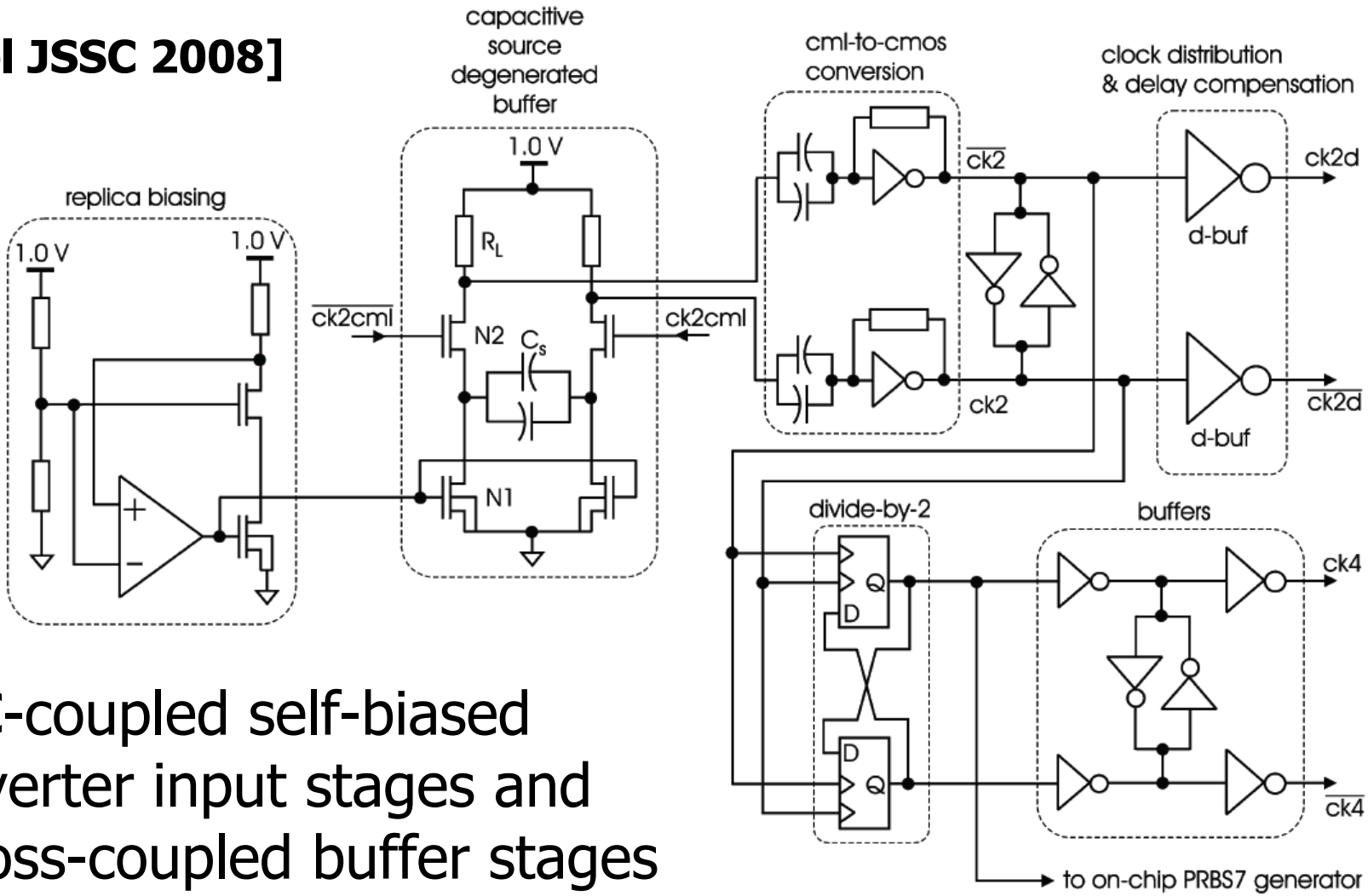
[Balamurugan JSSC 2008]



- Differential input stage followed by high-swing output stage
- Can be sensitive to power-supply noise and reduce jitter benefits of low-swing distribution techniques
- Often require some type of duty-cycle control

CML2CMOS Converter (2)

[Kossel JSSC 2008]



- AC-coupled self-biased inverter input stages and cross-coupled buffer stages can help improve duty cycle performance

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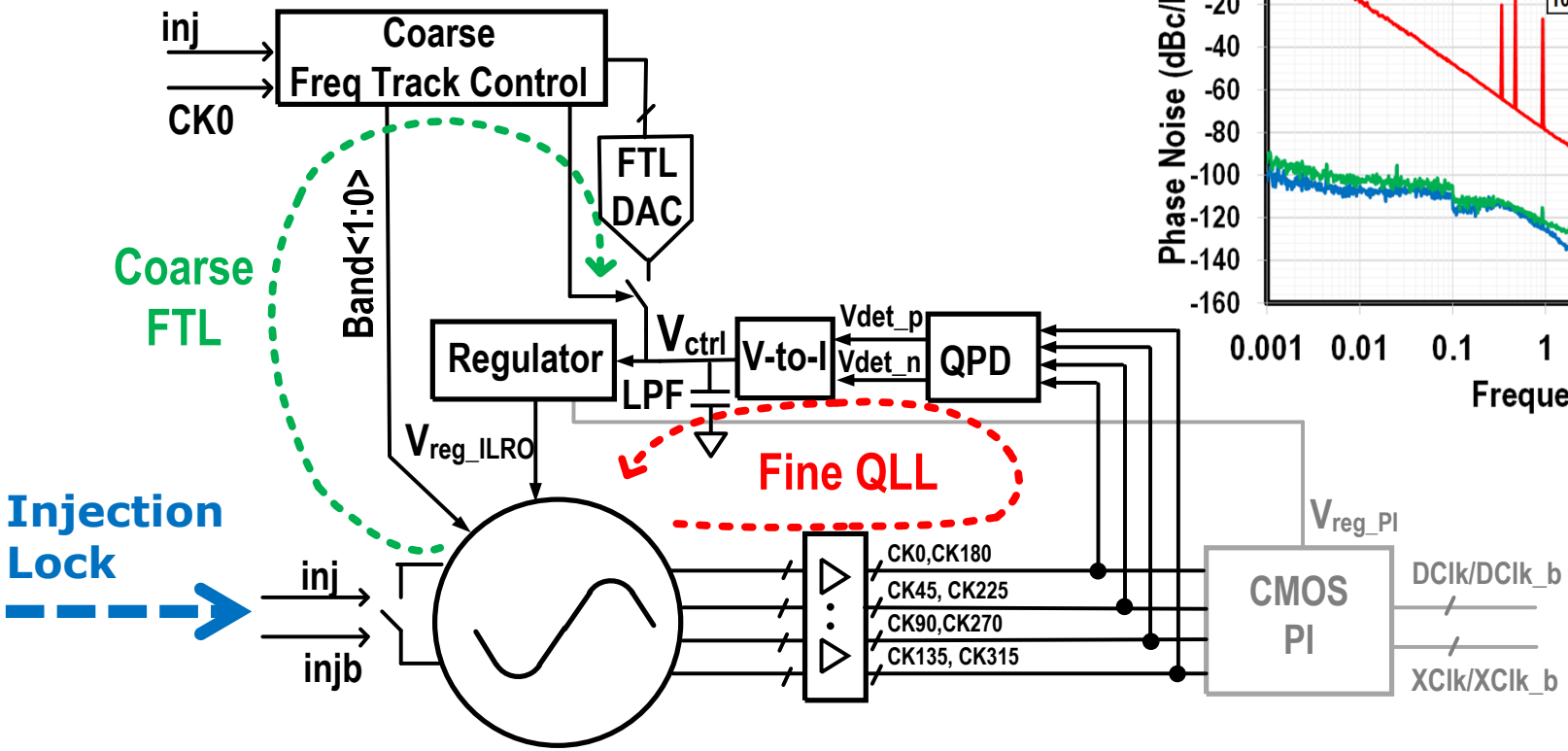
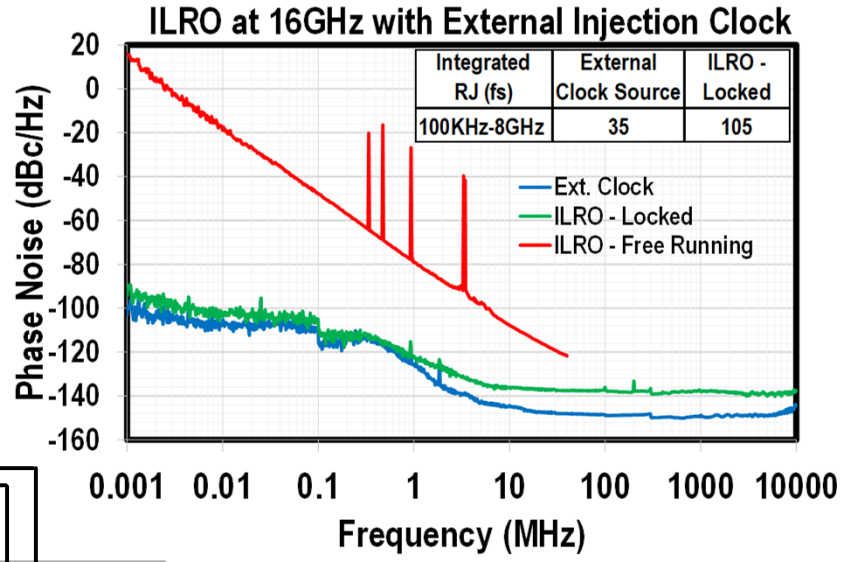
ILO-Based Multi-Phase Clock Generation

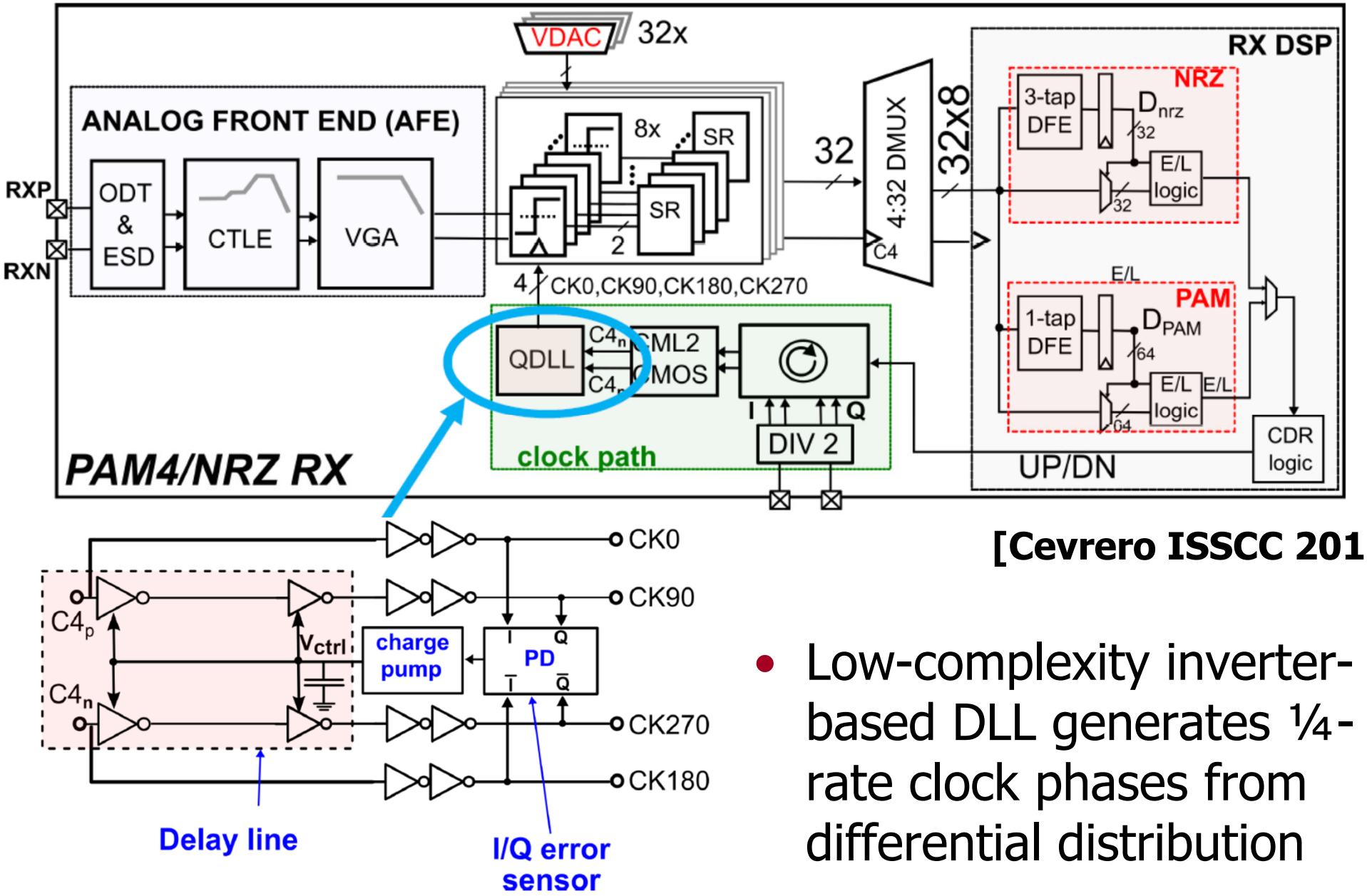
[Chen, ISSCC 2018]





- ILO generates multiple output phases from differential injected clock
- Coarse frequency tuning loop ensures that the ILO will lock
- Fine quadrature-locked loop minimizes phase error

IBM 100Gb/s PAM4 QDLL Phase Generation



[Cevrero ISSCC 2019]

- Low-complexity inverter-based DLL generates ¼-rate clock phases from differential distribution

Agenda

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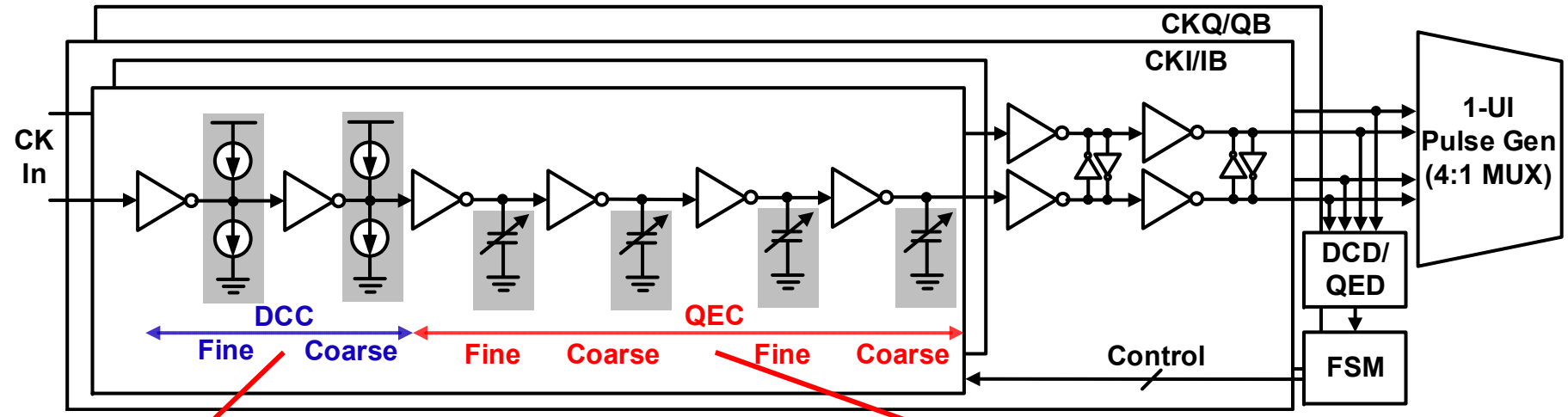
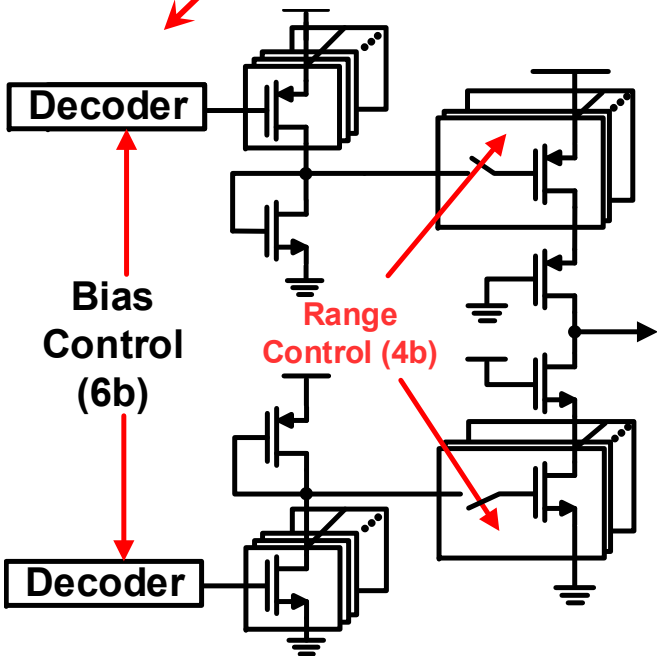
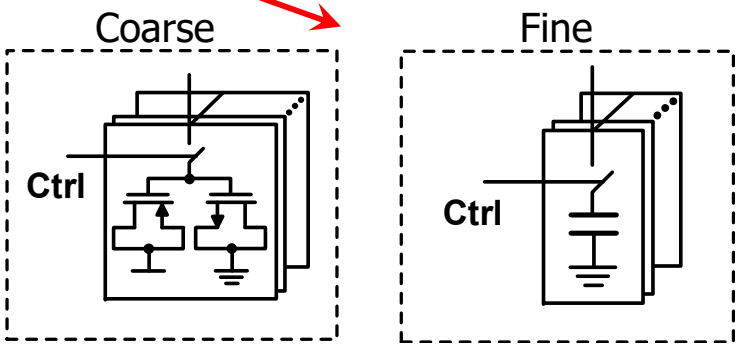
Clock Error Calibration Loop



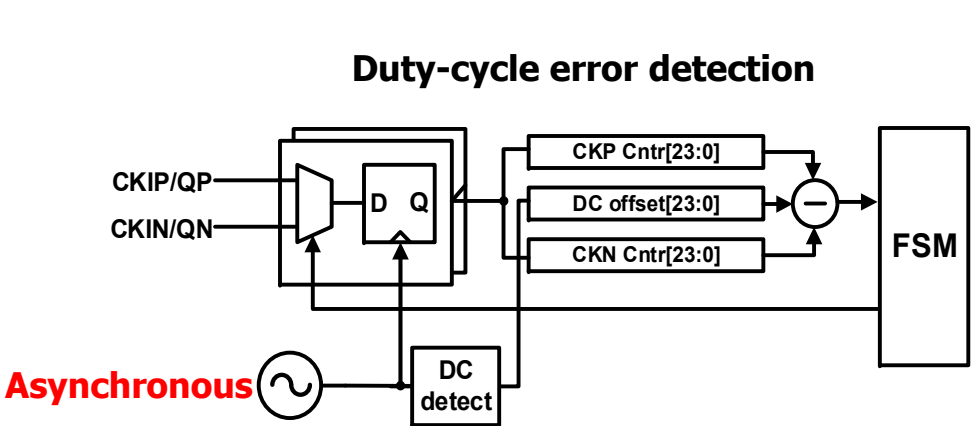


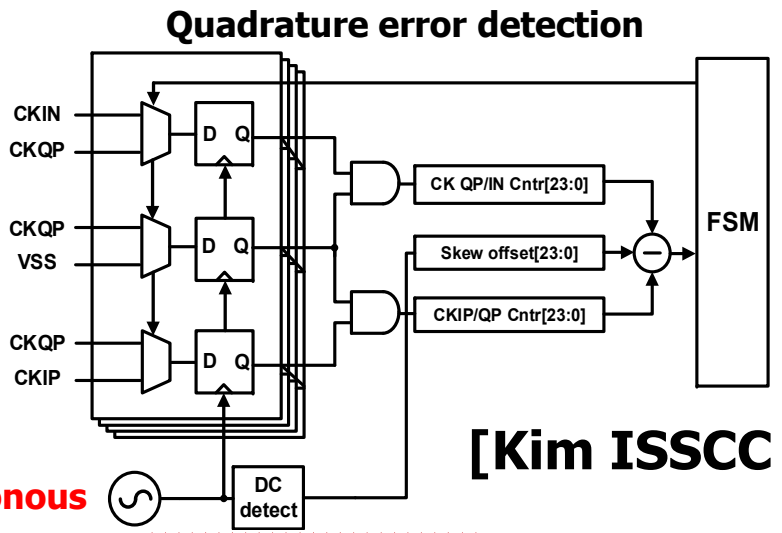


[Kim ISSCC 2019]

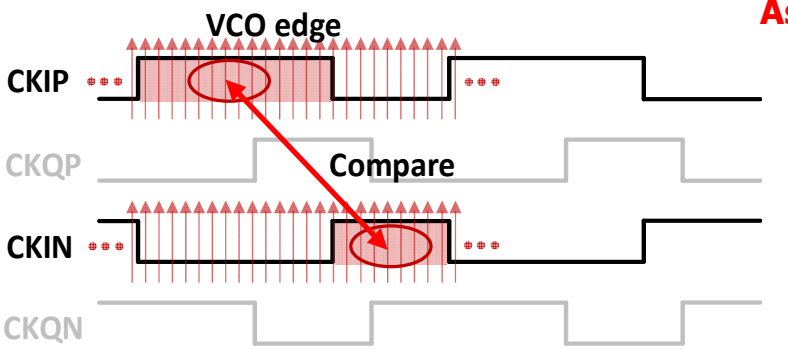
- 2-stage DCC & 4-stage QEC w/ 2-stage x-coupled buffers
- DCC with current injection and QEC with C-DAC

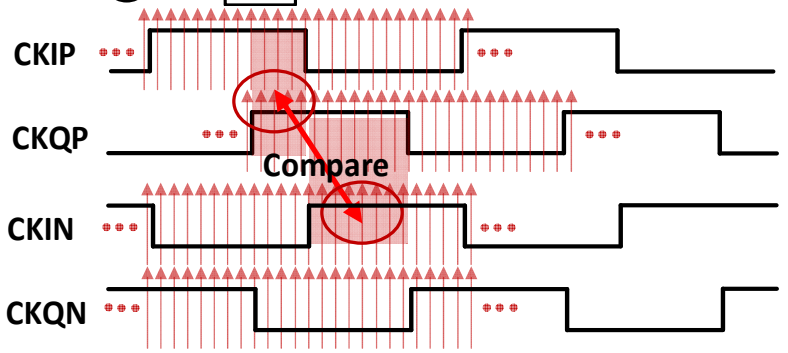
Asynchronous Sampling Error Detection





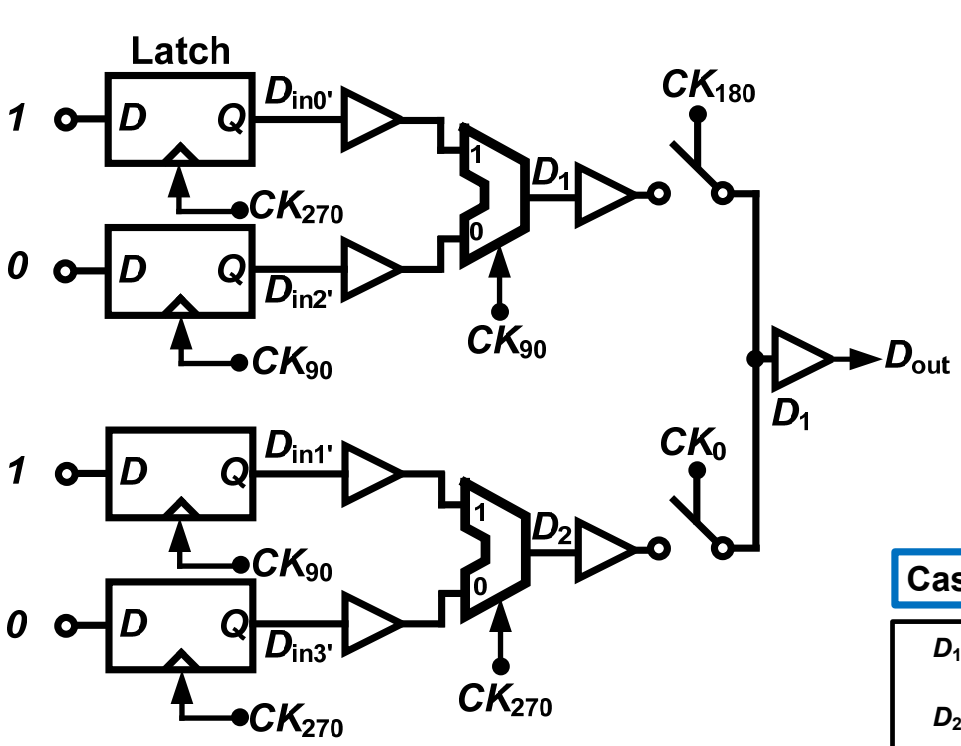
[Kim ISSCC 2019]

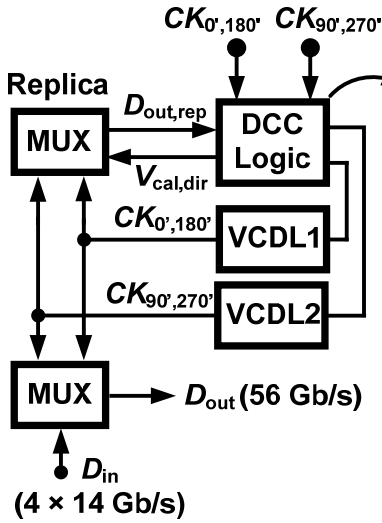


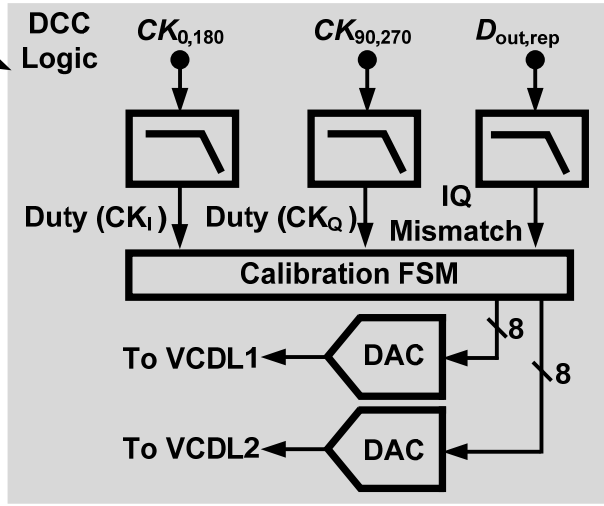


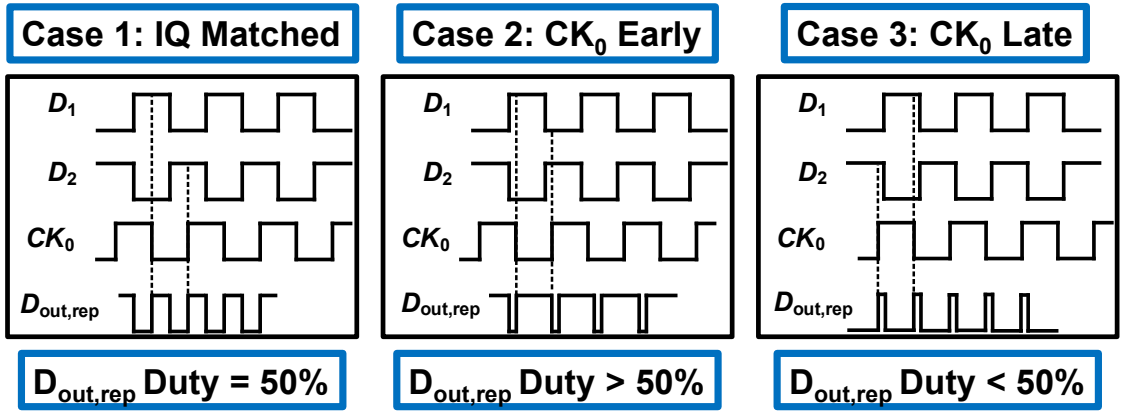
- Asynchronous VCO samples final ¼-rate clocks
- Duty cycle error minimized w/ equal P/N count
- Quadrature error minimized w/ equal IP*QP/QP*IN count

Background Quadrature Clock Calibration





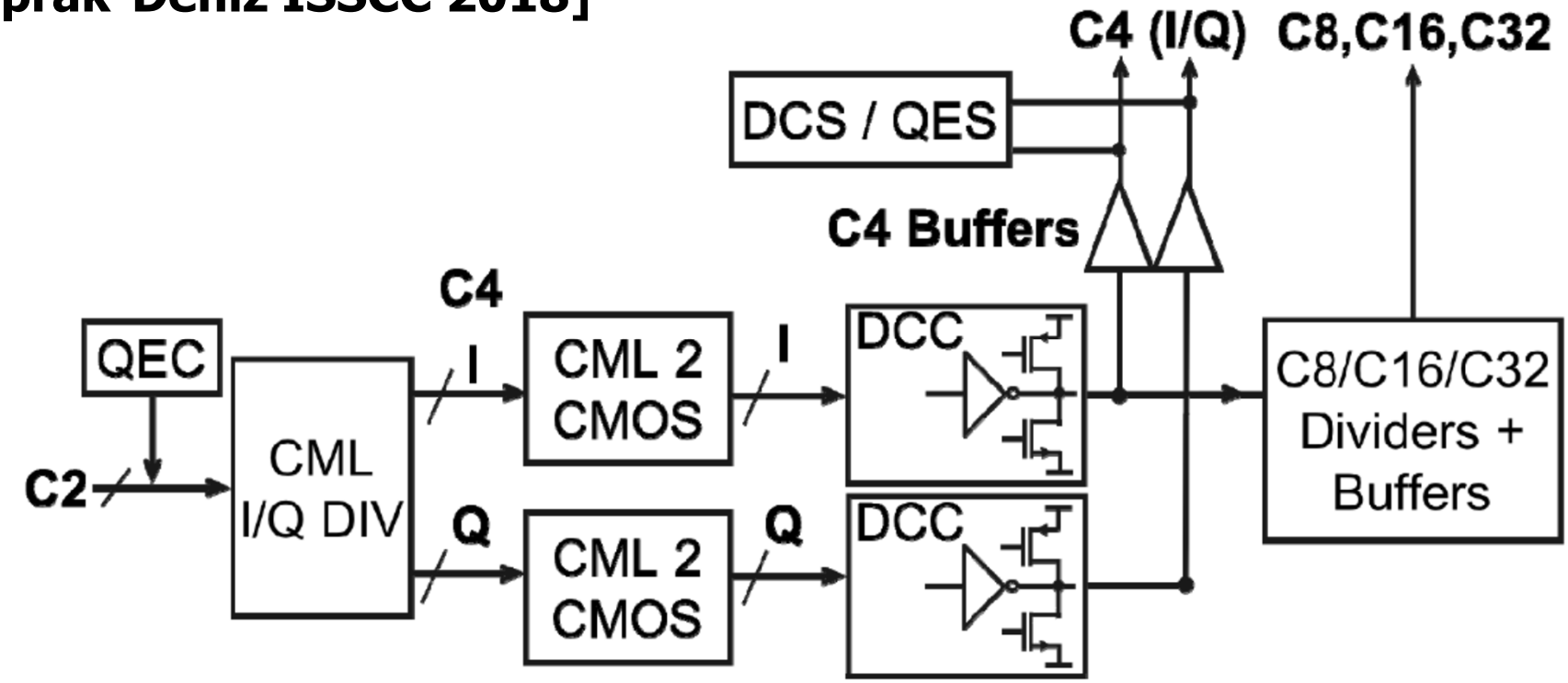




- Duty cycle error detected by low-pass filtering clocks
- IQ mismatch is detected by monitoring output duty cycle of replica mux
- Information is used to control independent I/Q VCDLs

128Gb/s PAM4 TX Clock Generation

[Toprak-Deniz ISSCC 2018]

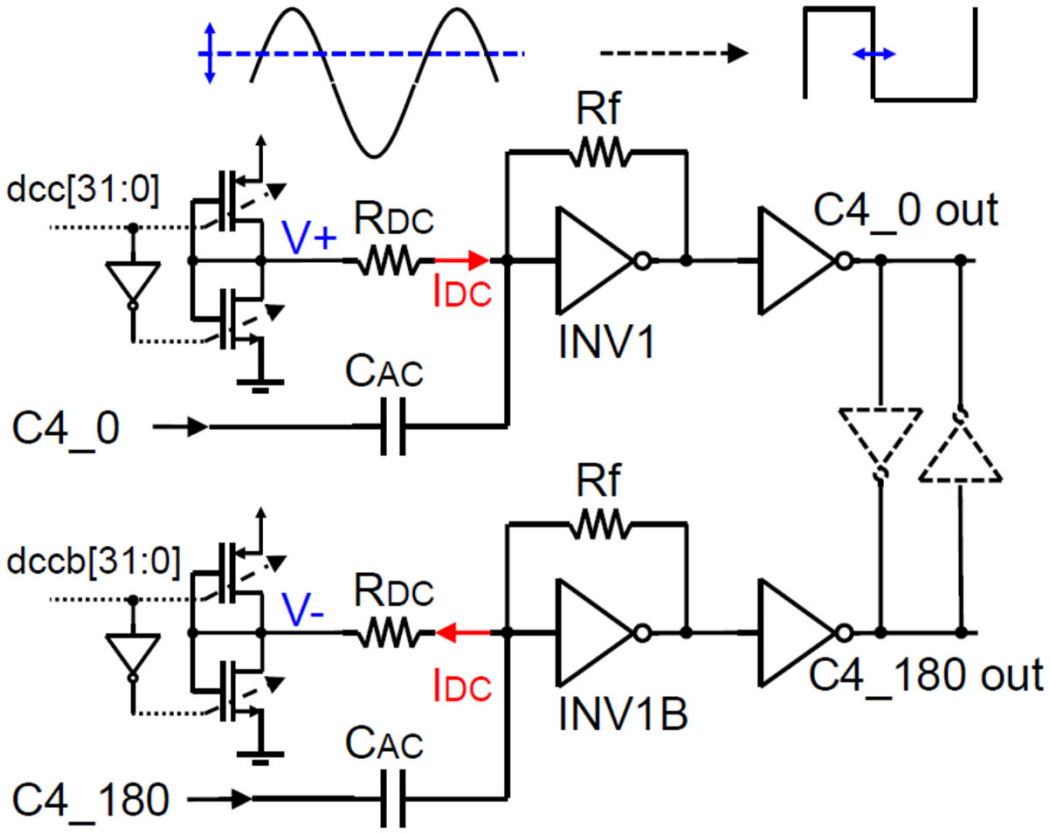


- DCC with current injection buffers
- QEC with differential offset voltage in half-rate CML divider

DCC w/ Inverter Trip Point Adjustment

- Clocks are AC-coupled to input inverters that are biased at the trip point with feedback resistors
- I_{DC} injected at inverter input shifts trip point and output duty cycle
- Monotonic control achieved with pull-up/down diodes
- R_{DC} can also be adjusted to change tuning range

[Menolfi ISSCC 2018]



Clock Generation & Distribution Take-Away Points

- Low-noise clock distribution is necessary in high-performance serial links
- Jitter amplification must be avoided in multi-lane clock distribution
- Efficient multi-phase generation and calibration is necessary for ¼-rate front-ends