

ECEN689: Special Topics in High-Speed Links Circuits and Systems Spring 2010

Lecture 14: RX Comparator Circuits



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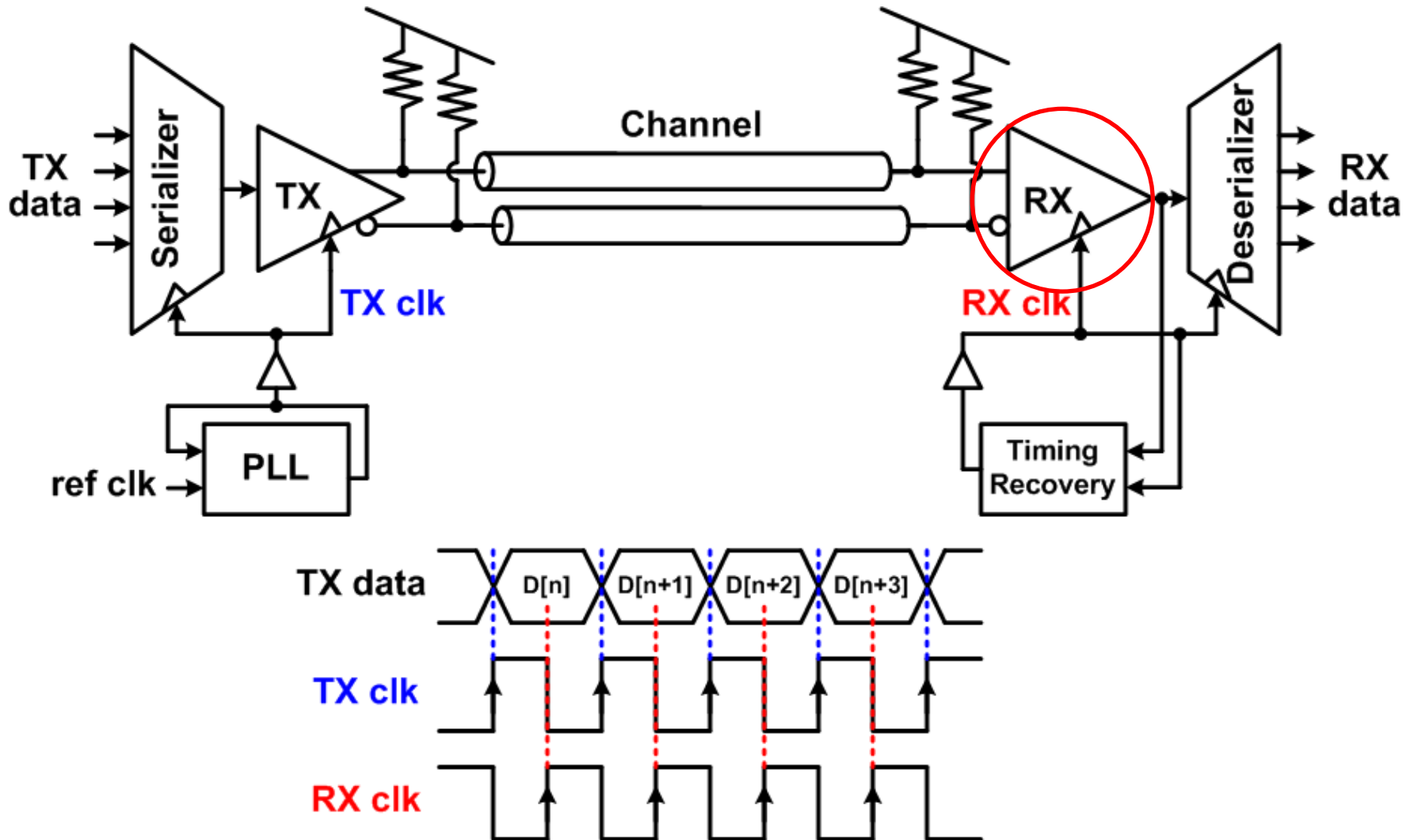
Announcements

- HW3 due now
- HW4 will be posted shortly
 - Involves transistor-level circuit design
 - Use 90nm or more advanced CMOS technology
 - Instructions on how to access 90nm CMOS models on website for students who don't already have access to a design kit
- Exam 1 is March 12
 - 9:10-10:10AM (10 extra minutes)
 - Closed book w/ one standard note sheet
 - 8.5"x11" front & back
 - Bring your calculator
- Reading
 - Dally 11.1-11.3
 - Papers posted on TX drivers and RX comparator analysis

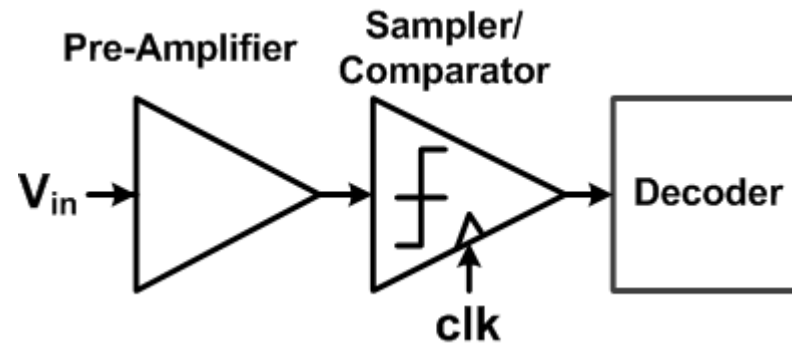
Agenda

- RX Circuits
 - Clocked comparators
 - Circuits
 - Characterization techniques
 - Integrating receivers
 - RX sensitivity
 - Offset correction
 - Demultiplexing receivers

High-Speed Electrical Link System

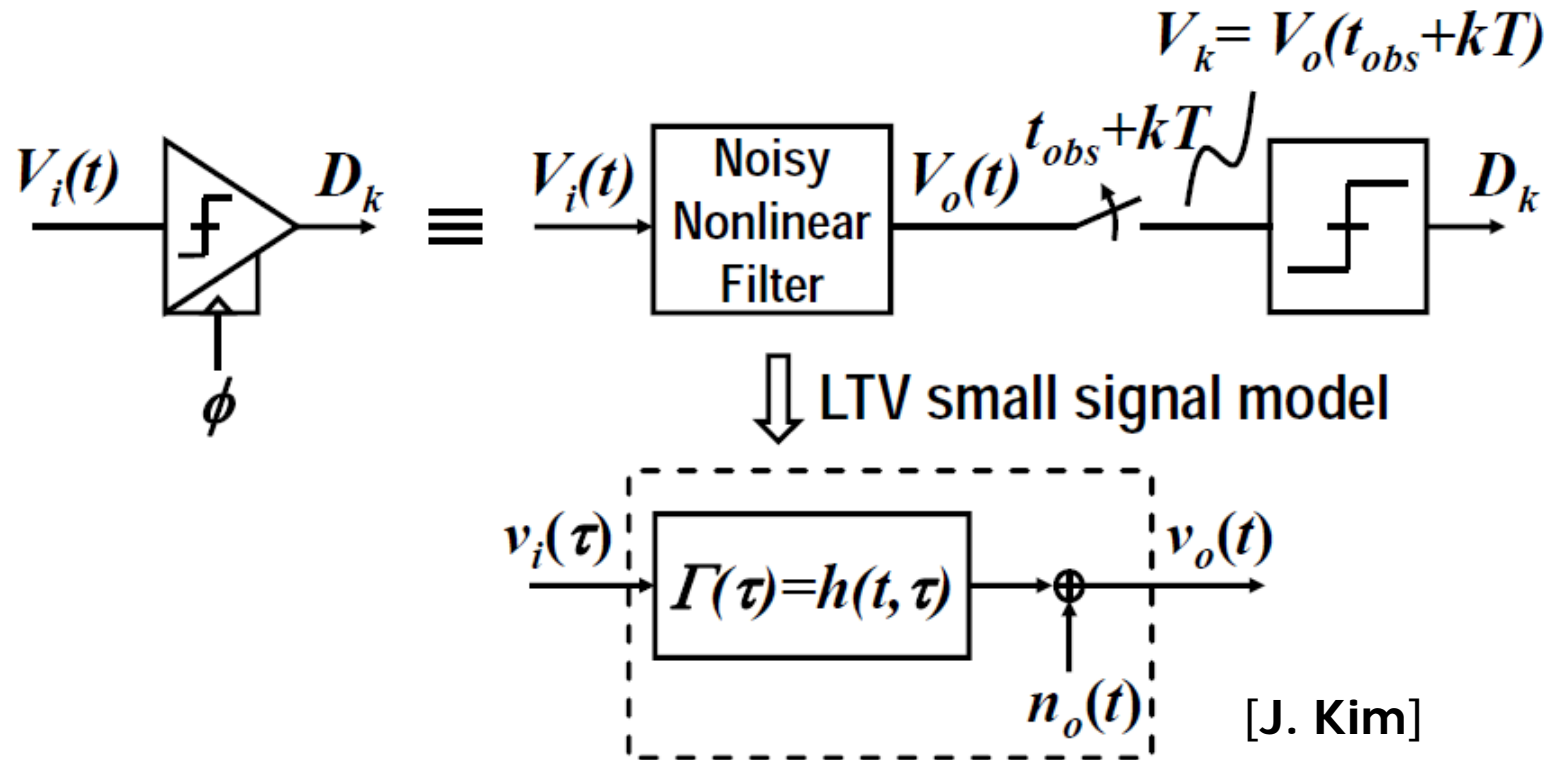


RX Block Diagram



- RX must sample the signal with high timing precision and resolve input data to logic levels with high sensitivity
- Input pre-amp can improve signal gain and improve input referred noise
 - Can also be used for equalization, offset correction, and fix sampler common-mode
 - Must provide gain at high-bandwidth corresponding to full data rate
- Comparator can be implemented with static amplifiers or clocked regenerative amplifiers
 - Clocked regenerative amplifiers are more power efficient for high gain
- Decoder used for advanced modulation (PAM4, Duo-binary)

Clocked Comparator LTV Model



- Comparator can be viewed as a noisy nonlinear filter followed by an ideal sampler and slicer (comparator)
- Small-signal comparator response can be modeled with an ISF $\Gamma(\tau) = h(t, \tau)$

Clocked Comparator ISF

- Comparator ISF is a subset of a time-varying impulse response $h(t, \tau)$ for LTV systems:

$$y(t) = \int_{-\infty}^{\infty} h(t, \tau) \cdot x(\tau) d\tau$$

- $h(t, \tau)$: system response at t to a unit impulse arriving at τ
- For LTI systems, $h(t, \tau) = h(t - \tau)$ (convolution)
- ISF $\Gamma(\tau) = h(t_o, \tau)$
 - For comparators, t_o is before decision is made
 - Output voltage of comparator

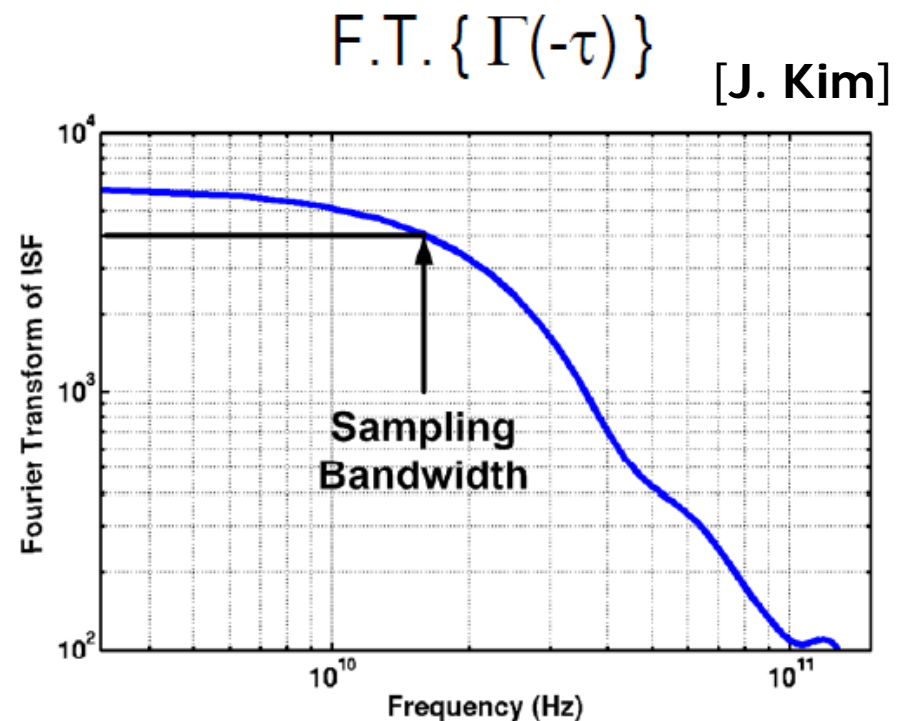
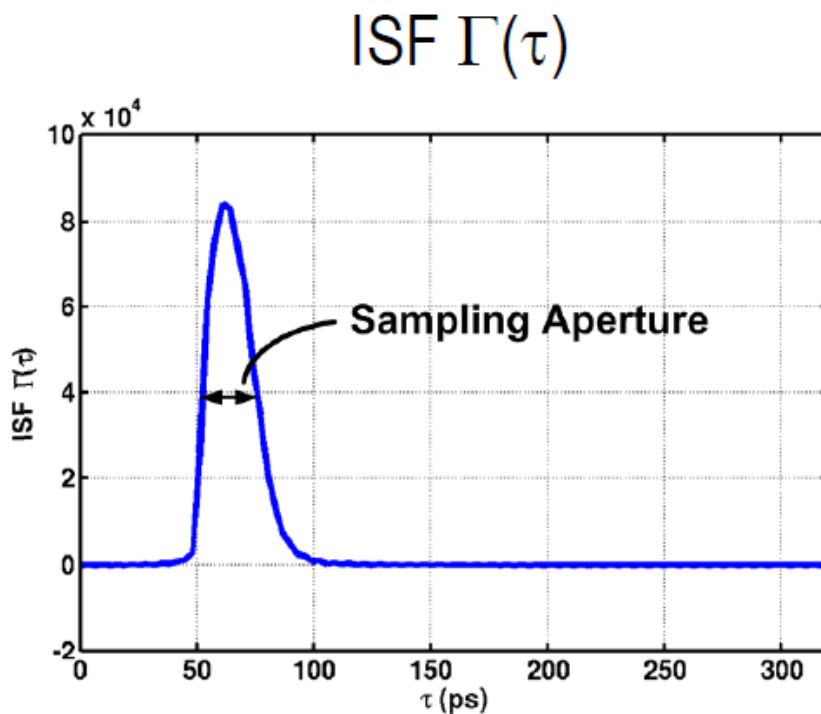
$$v_o(t_{obs}) = \int_{-\infty}^{\infty} v_i(\tau) \cdot \Gamma(\tau) d\tau$$

- Comparator decision

$$D_k = \text{sgn}(v_k) = \text{sgn}(v_o(t_{obs} + kT)) = \text{sgn}\left(\int_{-\infty}^{\infty} v_i(\tau) \cdot \Gamma(\tau) d\tau\right)$$

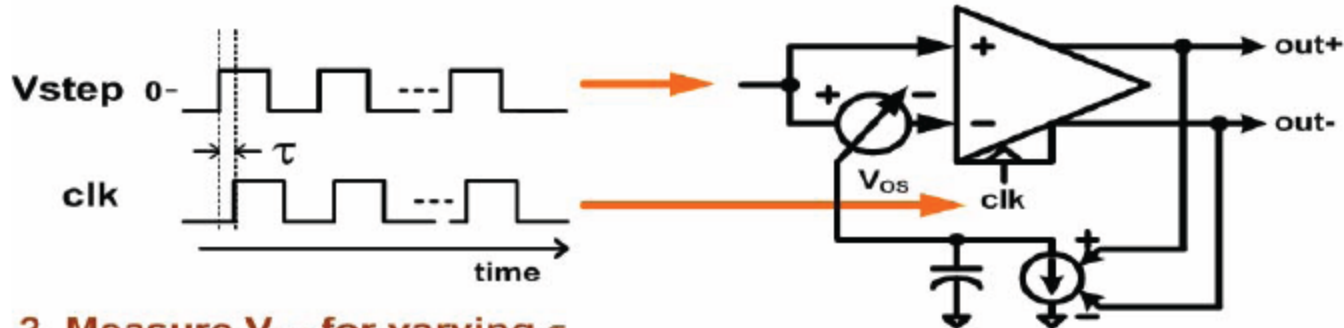
Clocked Comparator ISF

- ISF shows sampling aperture or timing resolution
- In frequency domain, it shows sampling gain and bandwidth



Characterizing Comparator ISF

1. Find Metastable $V_{ms}(\tau) = V_{os}(t \rightarrow \infty, \tau)$ such that $V(out+) = V(out-)$



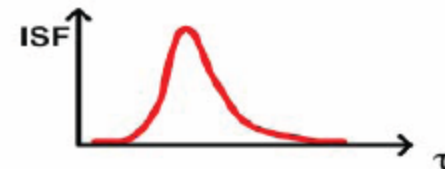
2. Measure V_{MS} for varying τ



3. Derive ISF

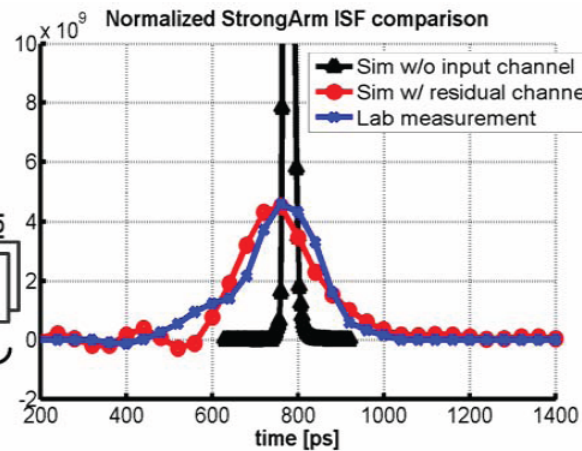
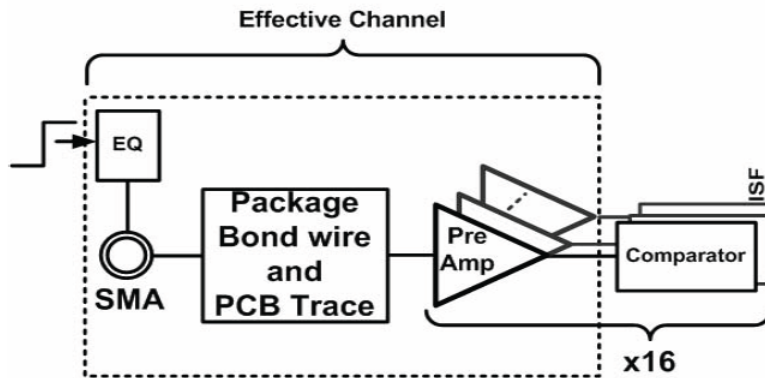
$$SSF_{norm}(\tau) = \frac{V_{MS}(\tau) - V_L}{V_H - V_L}$$

$$ISF_{norm}(\tau) = \frac{d}{d\tau} SSF_{norm}(\tau)$$

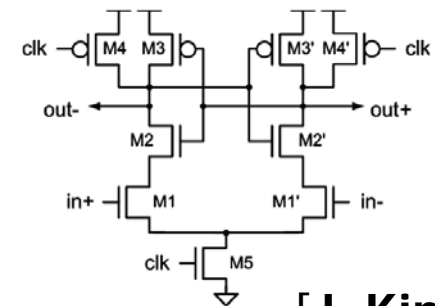


[Jeeradit VLSI 2008]

Comparator ISF Measurement Setup



Strong-Arm Latch



[J. Kim]

StrongARM Comparator

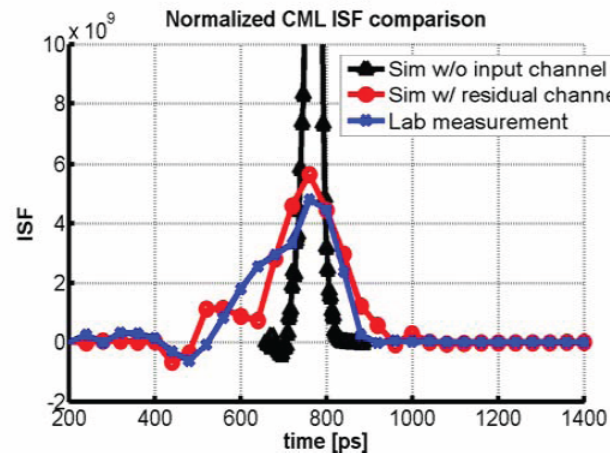
	Aperture Time [ps]	Sampling BW [GHz]	Sampling Gain [dB]
Sim w/o Channel	23	14.9	67.6
Sim w Channel	300	1.4	56.6
Lab	280	1.4	N/A

CML Comparator

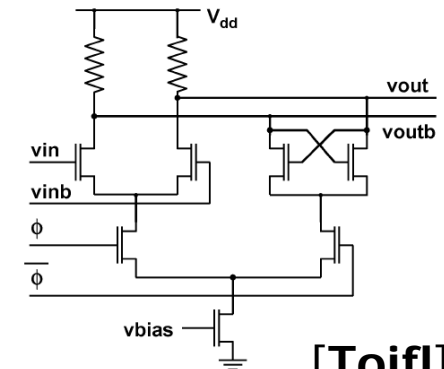
	Aperture Time [ps]	Sampling BW [GHz]	Sampling Gain [dB]
Sim w/o Channel	50	6.8	88.8
Sim w Channel	300	1.4	58.0
Lab	280	1.4	N/A

Note: the aperture time is defined as the width that contains 80% of the sensitivity similar to [1]

[Jeeradit VLSI 2008]



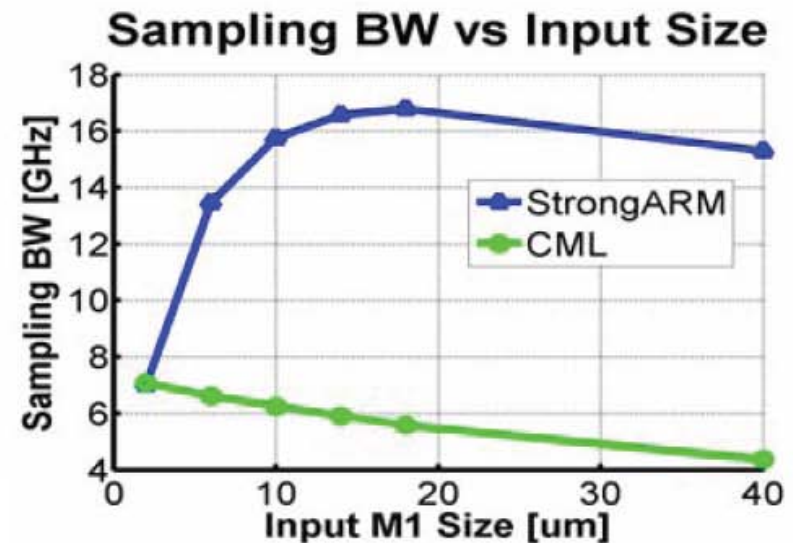
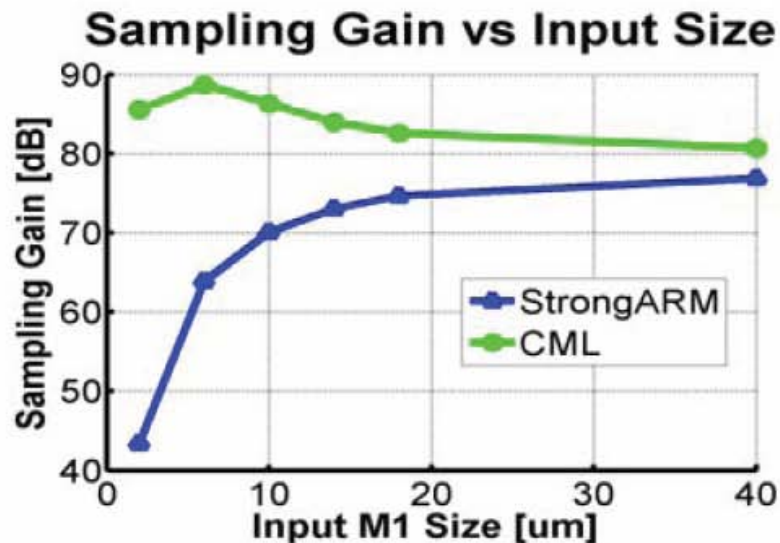
CML Latch



[Toifl]

Comparison of SA & CML Comparator (1)

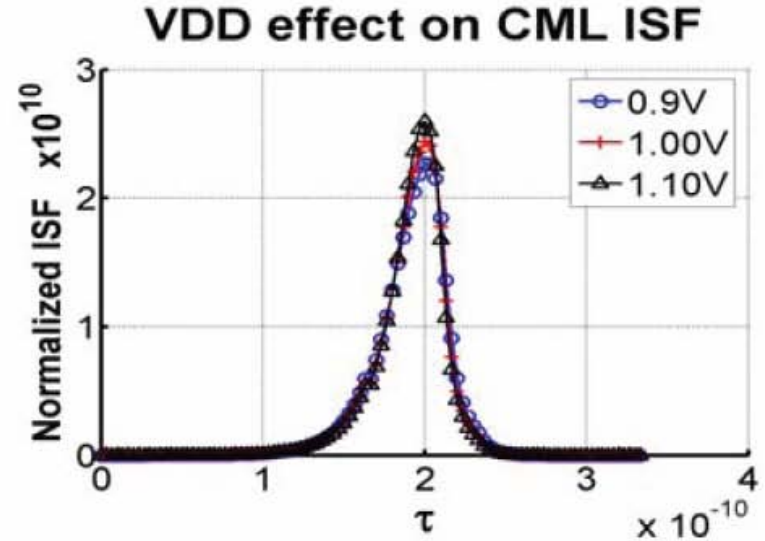
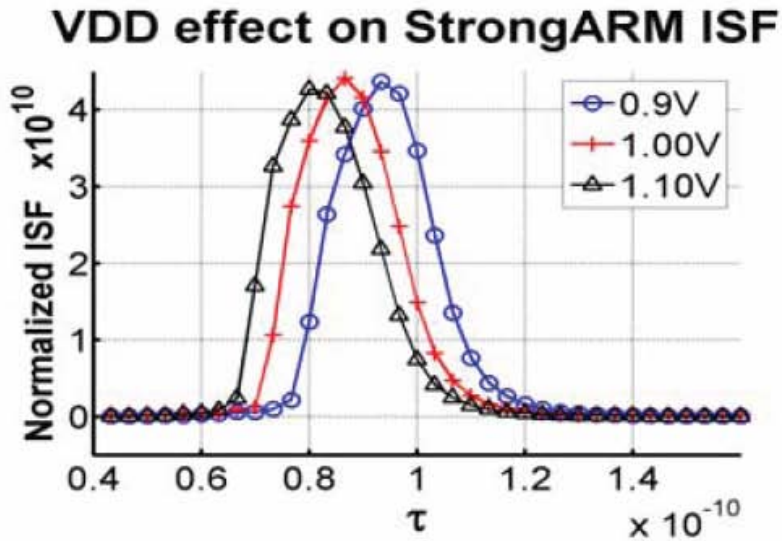
[Jeeradit VLSI 2008]



- CML latch has higher sampling gain with small input pair
- StrongARM latch has higher sampling bandwidth
 - For CML latch increasing input pair also directly increases output capacitance
 - For SA latch increasing input pair results in transconductance increasing faster than capacitance

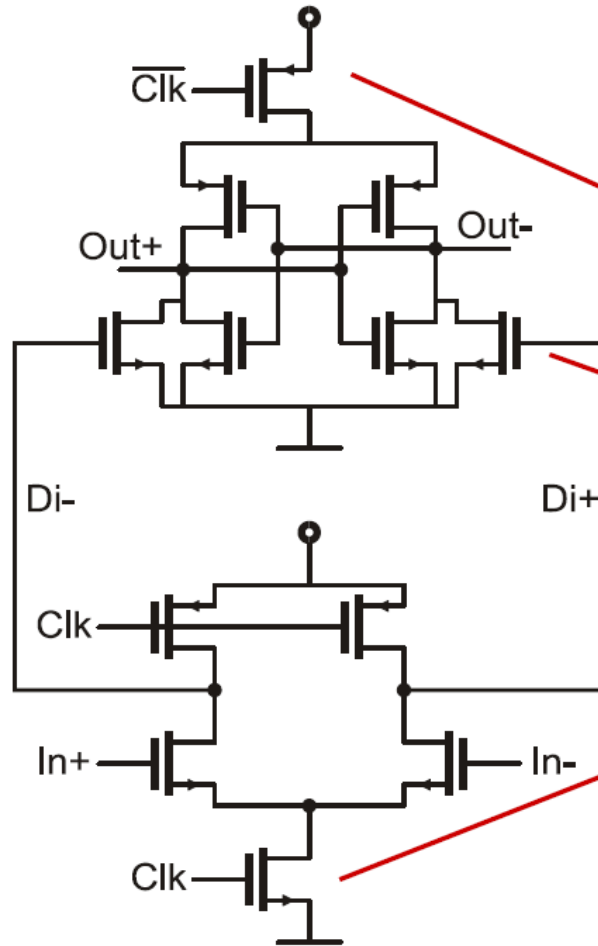
Comparison of SA & CML Comparator (2)

[Jeeradit VLSI 2008]



- Sampling time of SA latch varies with VDD, while CML isn't affected much

Low-Voltage SA – Schinkel ISSCC 2007

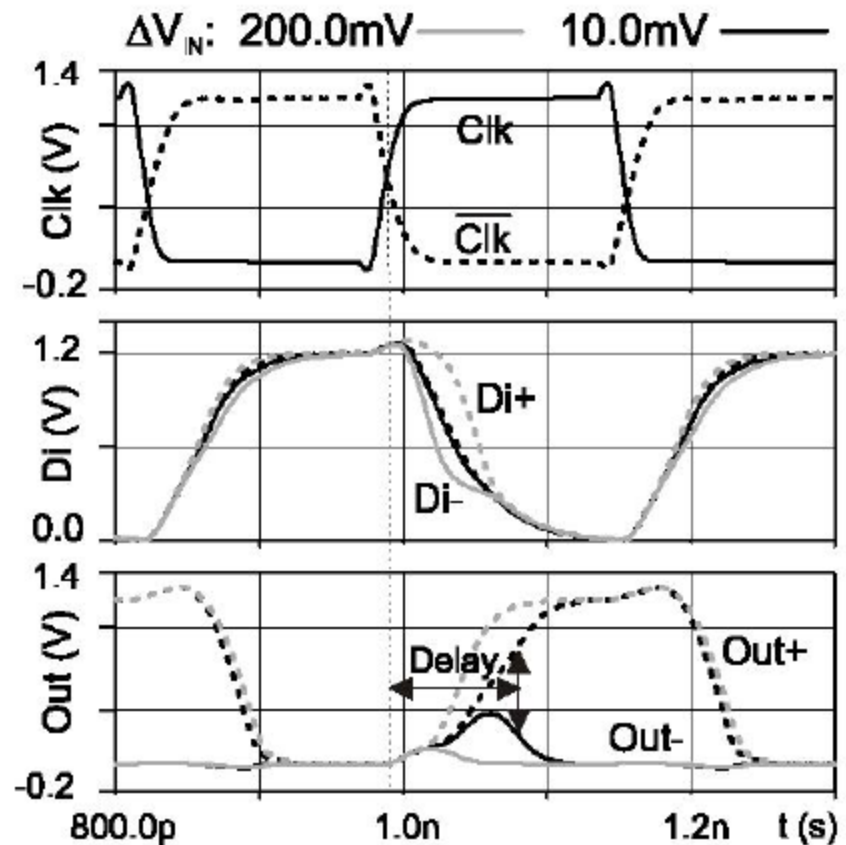
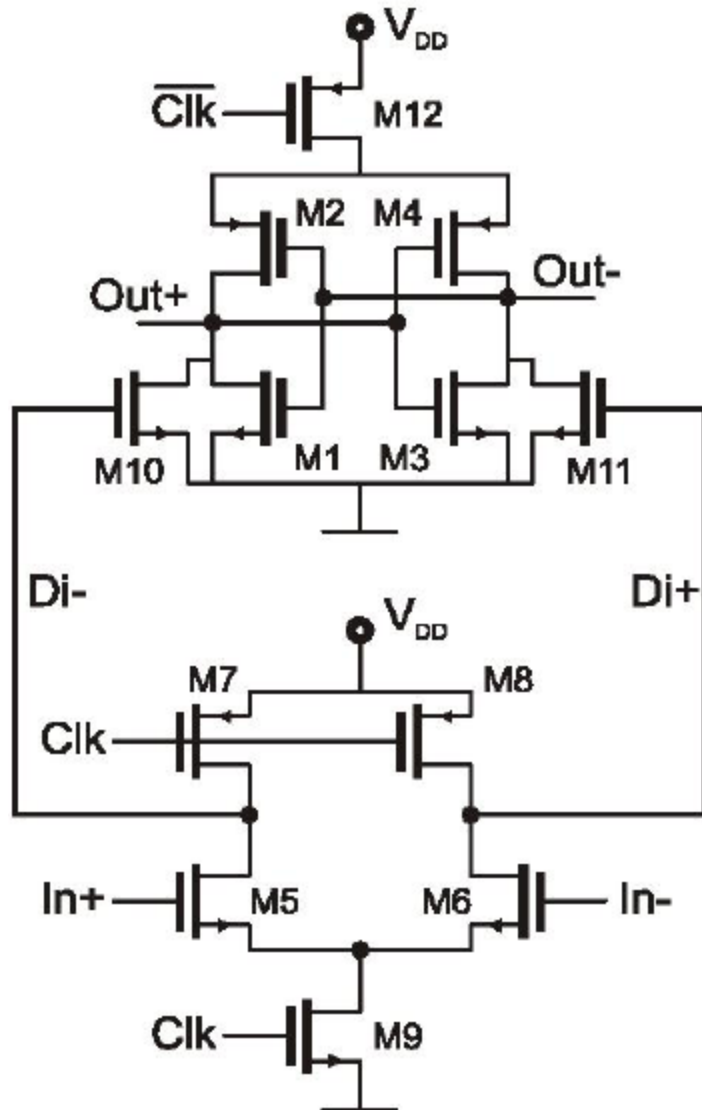


Advantages:

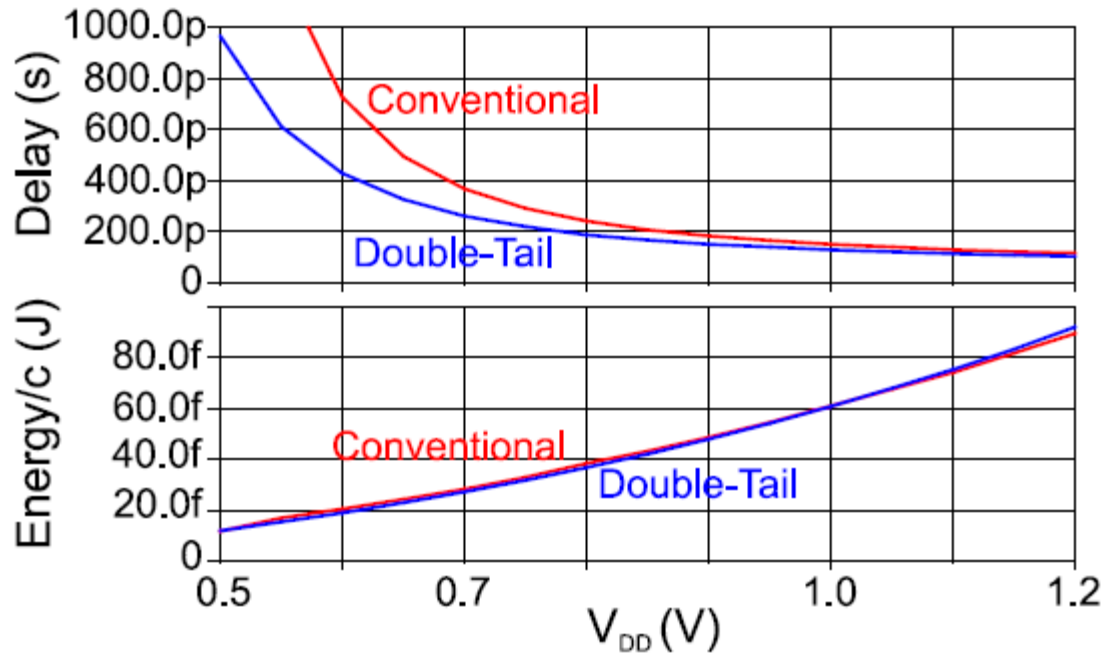
- Less stacking
- Wide tail for fast latching
- More isolation between in- and output
- Small tail \rightarrow input stage in weak inversion \rightarrow less offset from latch

- Does require clk & clk_b
 - How sensitive is it to skew?

Low-Voltage SA – Schinkel ISSCC 2007



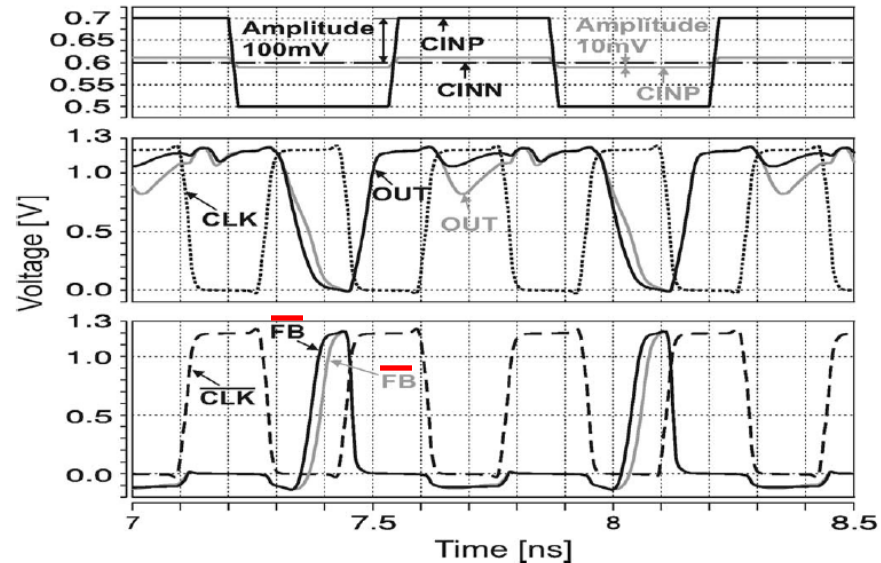
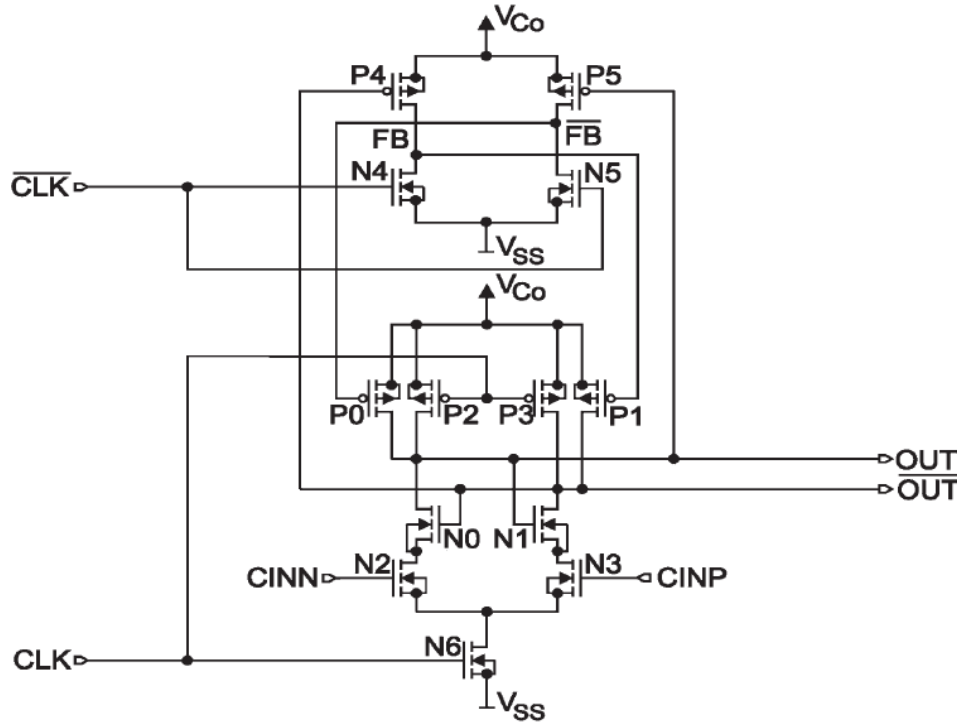
Low-Voltage SA – Schinkel ISSCC 2007



90nm CMOS simulations. $\Delta V_{in}=50\text{mV}$.

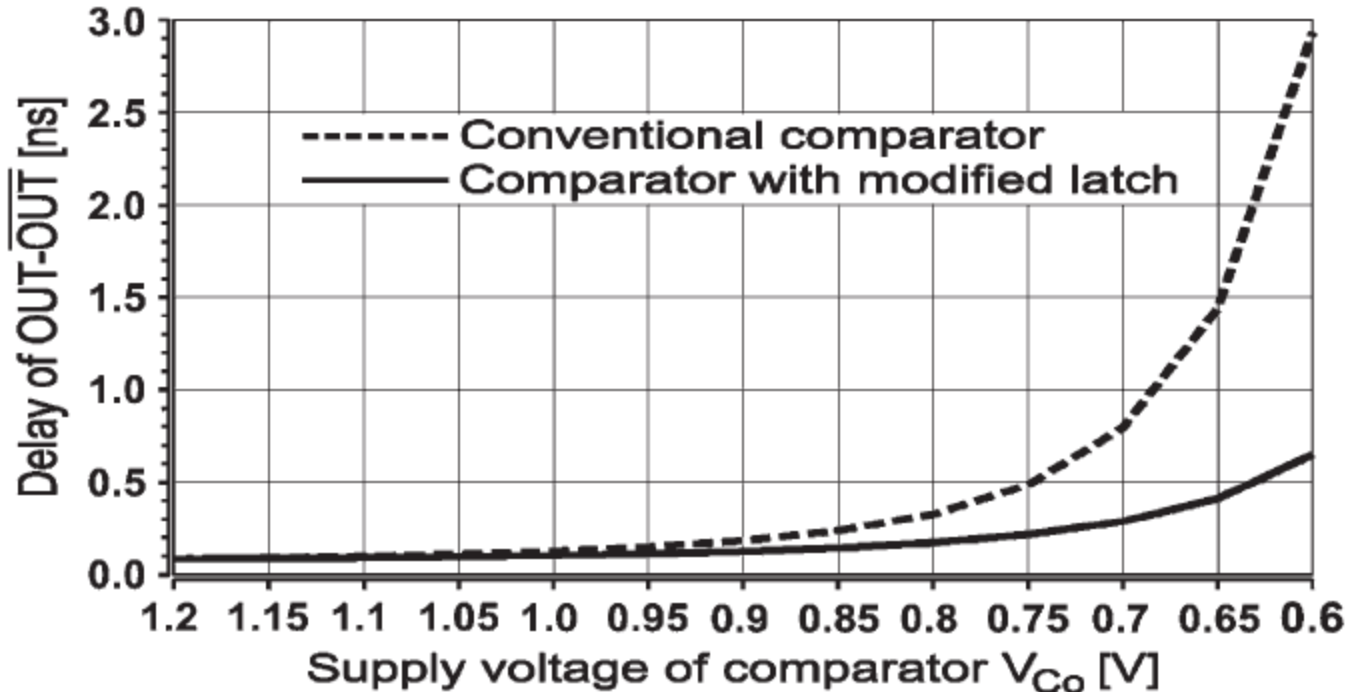
Circuits designed for equal offset $\sigma_{os}=10\text{mV}$ at $V_{cm}=1.1\text{V}$

Low-Voltage SA – Goll TCAS2 2009

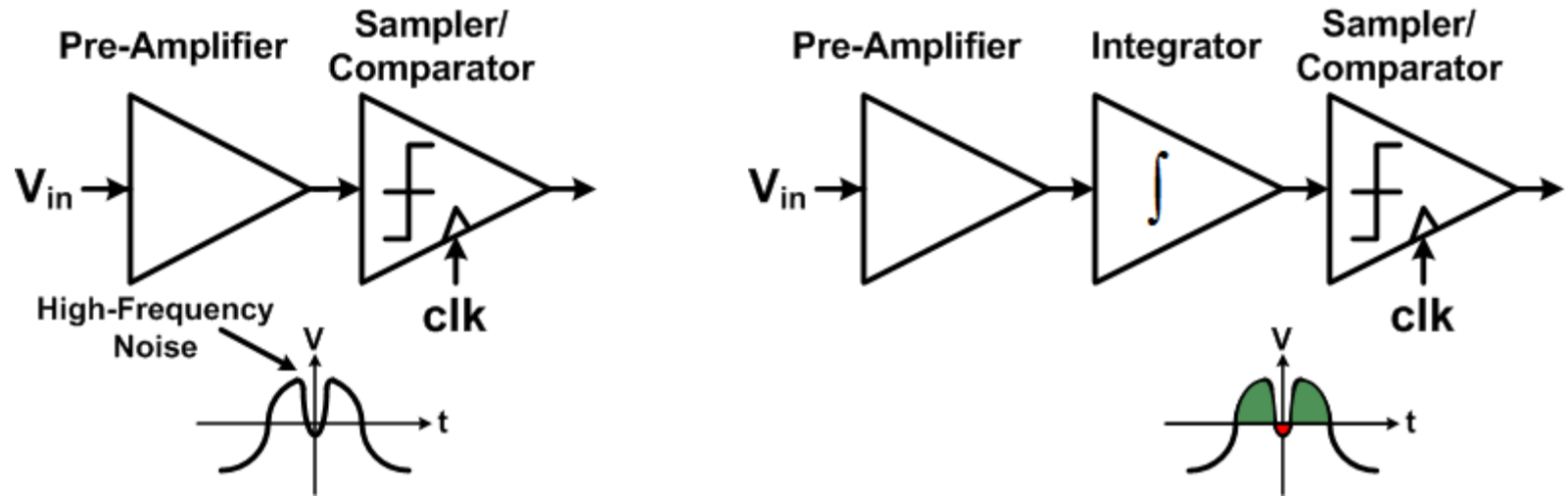


- Similar stacking to conventional SA latch
- However, now P0 and P1 are initially on during evaluation which speeds up operation at lower voltages
- Does require clk & clk_b
 - How sensitive is it to skew?

Low-Voltage SA – Goll TCAS2 2009

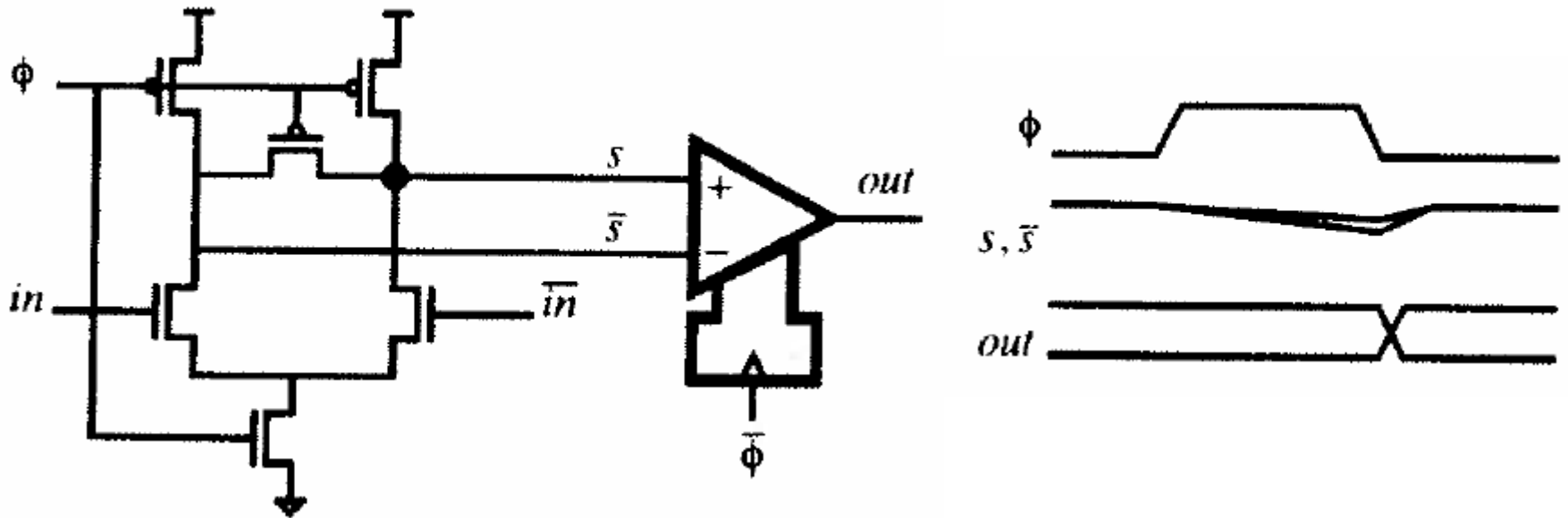


Integrating RX & High-Frequency Noise



- A small aperture time is desired in most receiver samplers
- However, high-frequency noise can degrade performance at sampling time
 - Can be an issue in single-ended systems with excessive LdI/dt switching noise
- Integrating the input signal over a sampling interval reduces the high-frequency noise impact

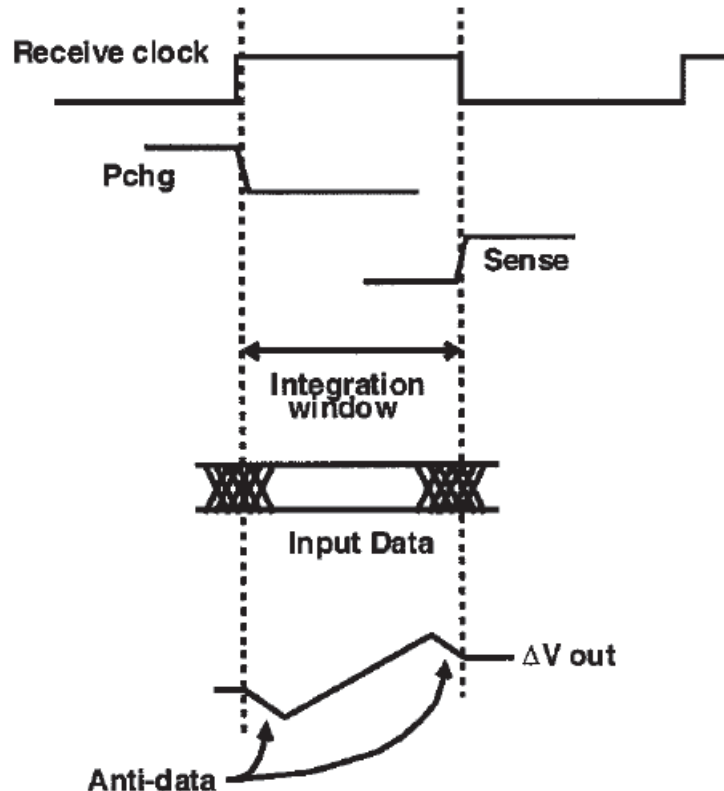
Integrating Amplifier



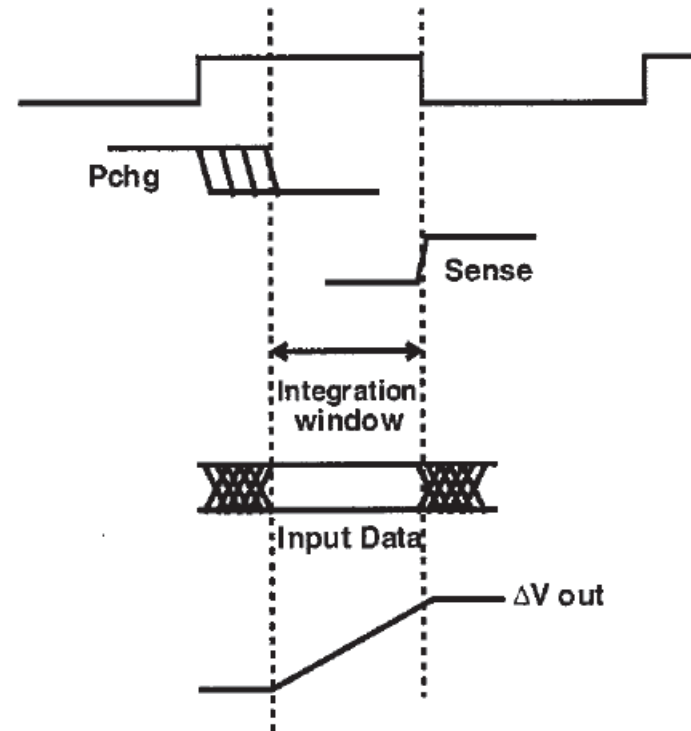
- Differential input voltage converted to a differential current that is integrated on the sense nodes' capacitance

Windowed Integration

No time windowing –
Integrating over complete bit



Windowed Integration



[Zerbe JSSC 2001]

- Windowing integration time can minimize transition noise and maximize integration of valid data

RX Sensitivity

- RX sensitivity is a function of the input referred noise, offset, and minimum latch resolution voltage

$$v_S^{pp} = 2v_n^{rms} \sqrt{SNR} + v_{min} + v_{offset*}$$

- Gaussian (unbounded) input referred noise comes from input amplifiers, comparators, and termination
 - A minimum signal-to-noise ratio (SNR) is required for a given bit-error-rate (BER)

$$\text{For BER} = 10^{-12} (\sqrt{SNR} = 7)$$

- Minimum latch resolution voltage comes from hysteresis, finite regeneration gain, and bounded noise sources

$$\text{Typical } v_{min} < 5mV$$

- Input offset is due to circuit mismatch (primarily V_{th} mismatch) & is most significant component if uncorrected

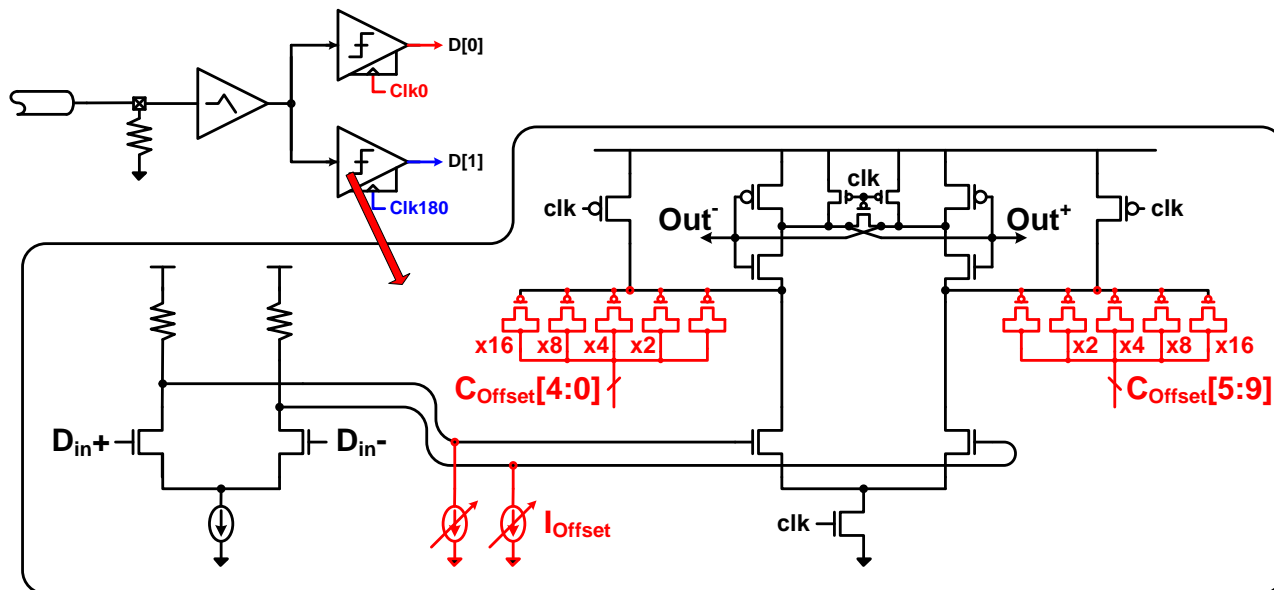
RX Sensitivity & Offset Correction

- RX sensitivity is a function of the input referred noise, offset, and min latch resolution voltage

$$v_S^{pp} = 2v_n^{rms} \sqrt{SNR} + v_{min} + v_{offset}^* \quad \text{Typical Values : } v_n^{rms} = 1mV_{rms}, v_{min} + v_{offset}^* < 6mV$$

$$\text{For BER} = 10^{-12} (\sqrt{SNR} = 7) \Rightarrow v_S^{pp} = 20mV_{pp}$$

- Circuitry is required to reduce input offset from a potentially large uncorrected value (>50mV) to near 1mV



Next Time

- Receiver Circuits
 - Demultiplexing receivers
- Equalization theory and circuits