ECEN689: Special Topics in High-Speed Links Circuits and Systems Spring 2010

Lecture 13: RX Circuits

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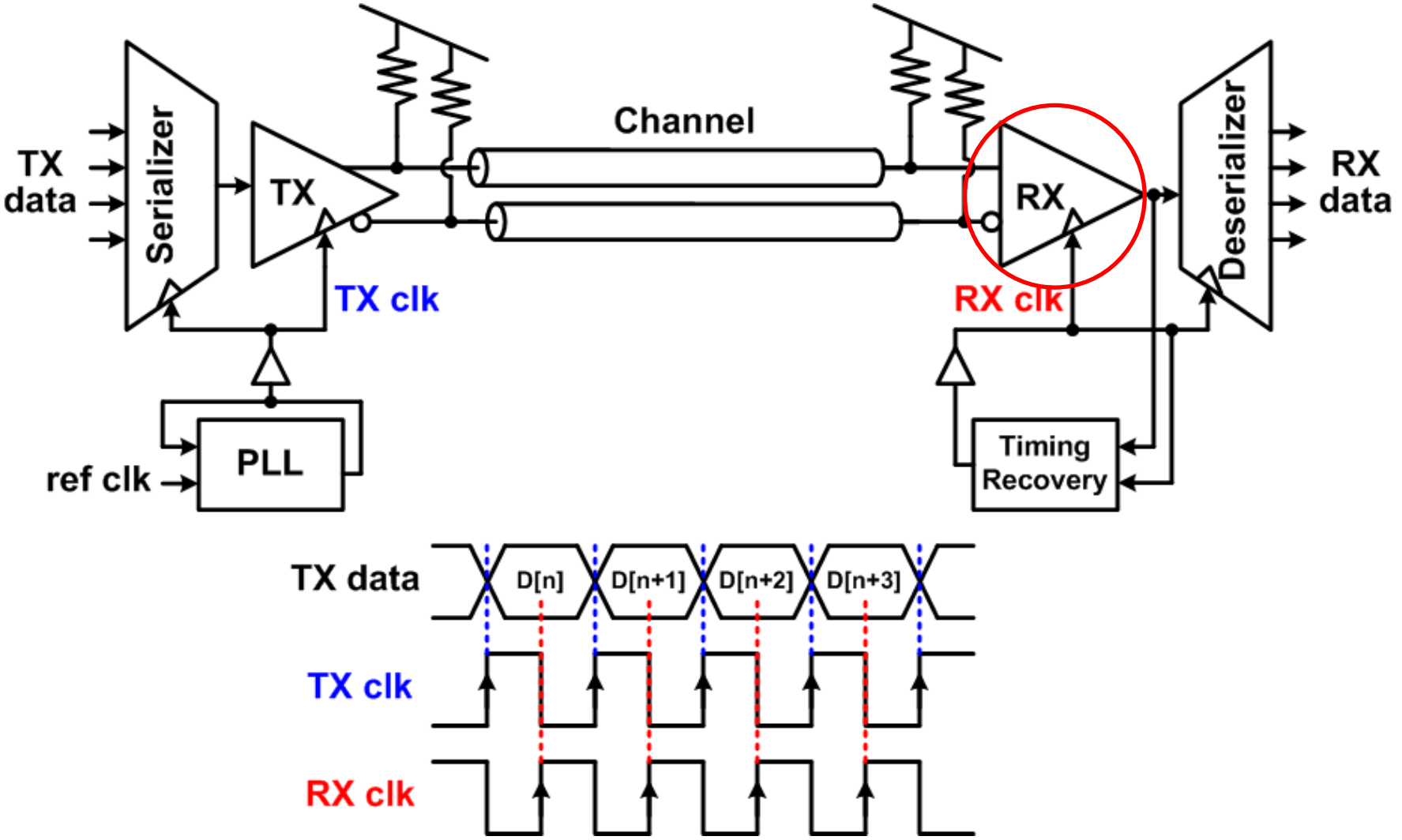
Announcements

- HW3 is posted on website and due Wednesday
- Exam 1 is scheduled for March 12
  - 9:10-10:10AM (10 extra minutes)
  - Closed book w/ one standard note sheet
    - 8.5”x11” front & back
  - Bring your calculator
- Reading
  - Dally 11.1-11.3
  - Papers posted on TX drivers and RX comparator analysis

Agenda

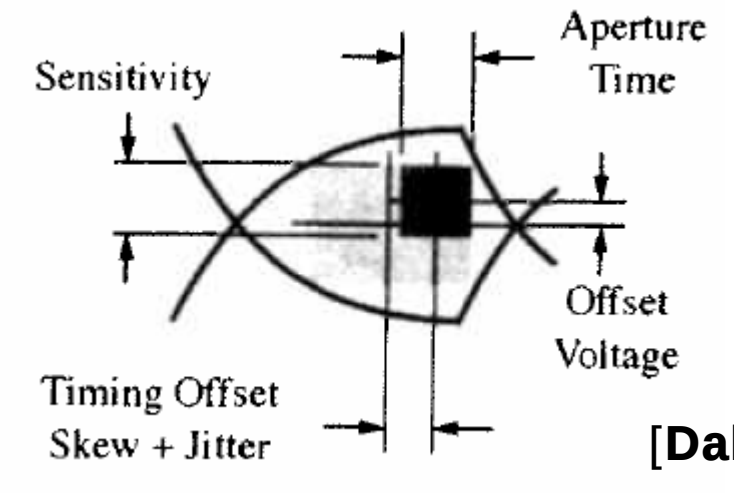
- RX Circuits
  - RX parameters
  - RX static amplifiers
  - Clocked comparators
    - Circuits
    - Characterization techniques
  - Integrating receivers
  - RX sensitivity
    - Offset correction

High-Speed Electrical Link System



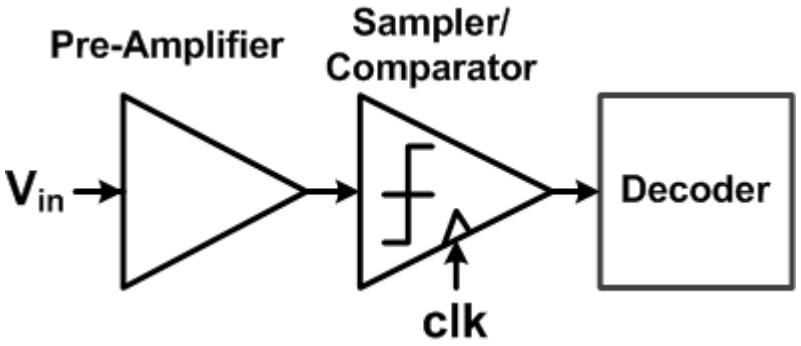
Receiver Parameters

- RX sensitivity, offsets in voltage and time domain, and aperture time are important parameters
- Minimum eye width is determined by aperture time plus peak-to-peak timing jitter
- Minimum eye height is determined by sensitivity plus peak-to-peak voltage offset



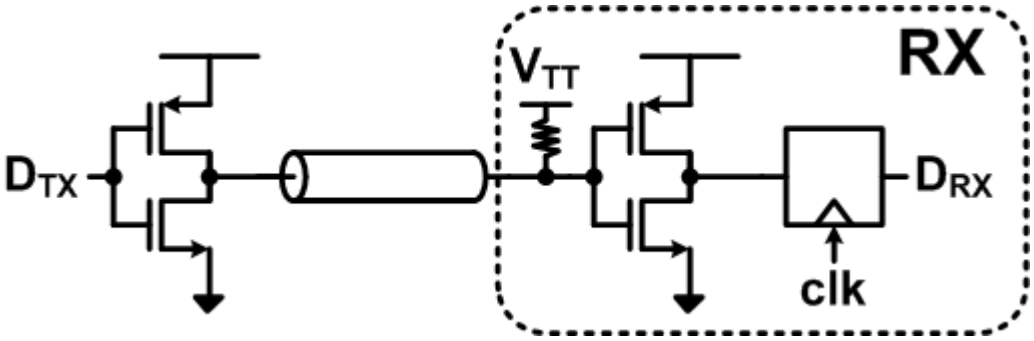
[**Dally**]

RX Block Diagram



- RX must sample the signal with high timing precision and resolve input data to logic levels with high sensitivity
- Input pre-amp can improve signal gain and improve input referred noise
  - Can also be used for equalization, offset correction, and fix sampler common-mode
  - Must provide gain at high-bandwidth corresponding to full data rate
- Comparator can be implemented with static amplifiers or clocked regenerative amplifiers
  - Clocked regenerative amplifiers are more power efficient for high gain
- Decoder used for advanced modulation (PAM4, Duo-binary)

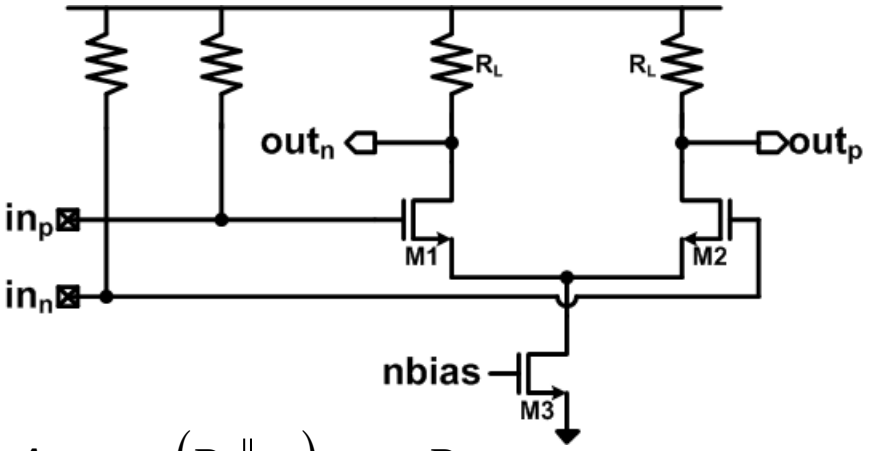
RX Static Amplifiers – Single-Ended Inverter



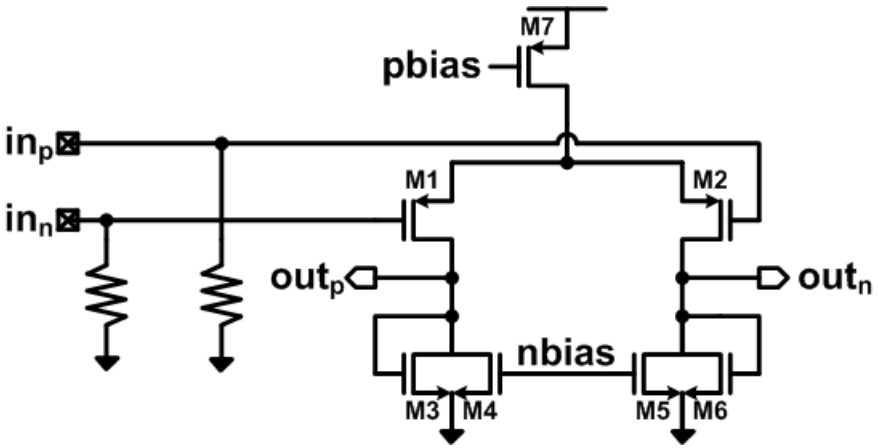
- CMOS inverter is one of the simplest RX pre-amplifier structures
- Termination voltage, V_{TT}, should be placed near inverter trip-point
- Issues:
  - Limited gain (<20)
  - High PVT variation results in large input referred offset
  - Single-ended operation makes it both sensitive to and generate supply noise

RX Static Differential Amplifiers

- Differential input amplifiers often used as input stage in high performance serial links
  - Rejects common-mode noise
  - Sets input common-mode for preceding comparator
- Input stage type (n or p) often set by termination scheme
- High gain-bandwidth product necessary to amplify full data rate signal
- Offset correction and equalization can be merged into the input amplifier



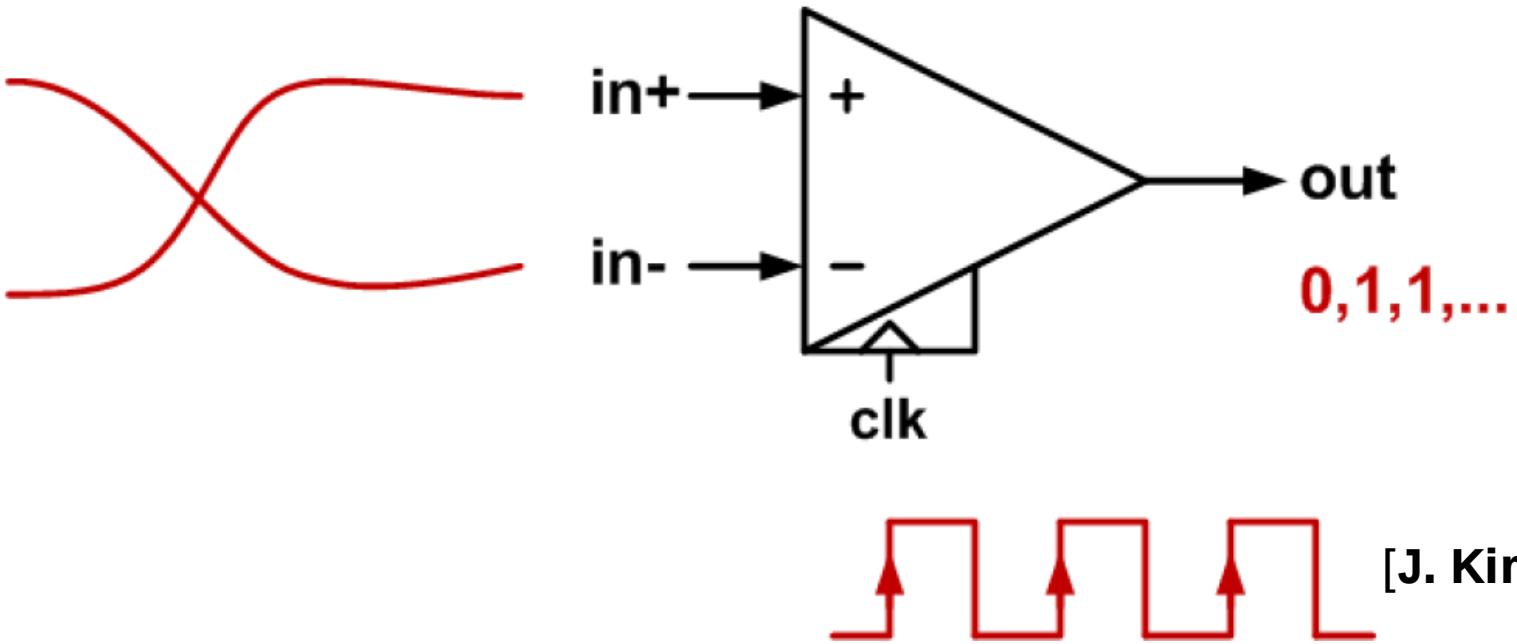
$$A_v = g_{m1}\left(R_L \| r_{o1}\right) \approx g_{m1} R_L$$



$$A_v = \frac{g_{m1}}{g_{m3} + g_{o3} + g_{o4} + g_{o1}} \approx \frac{g_{m1}}{g_{m3}}$$

RX Clocked Comparators

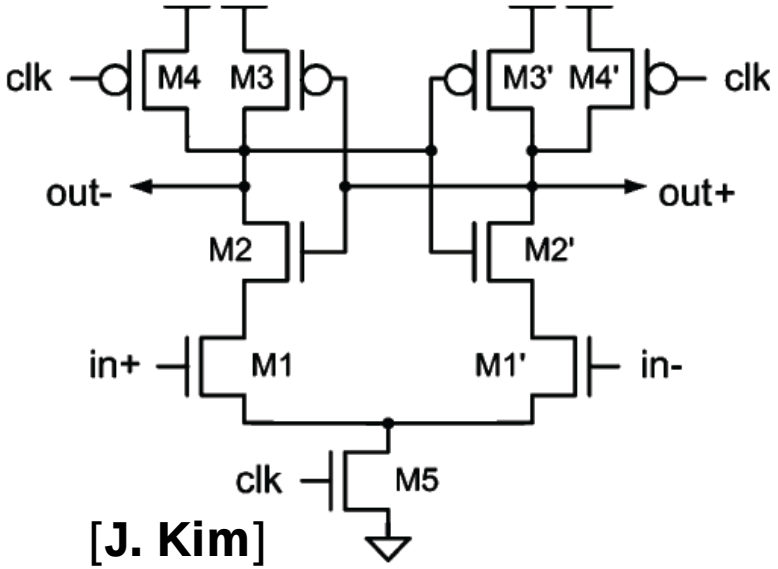
- Also called regenerative amplifier, sense-amplifier, flip-flop, latch
- Samples the continuous input at clock edges and resolves the differential to a binary 0 or 1



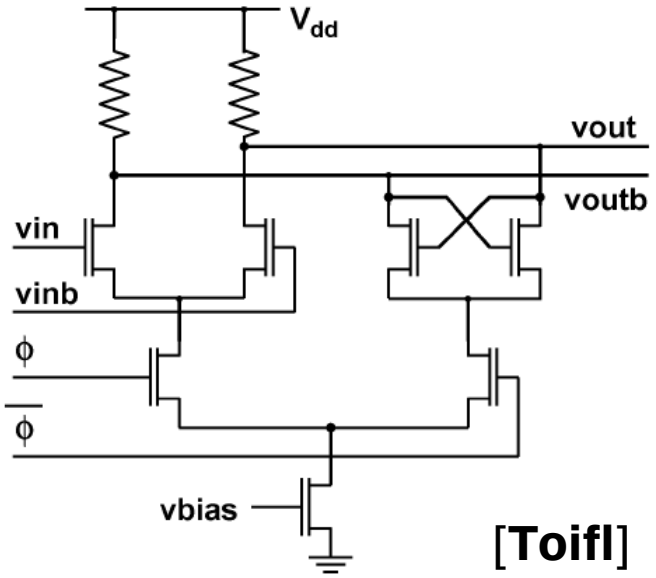
Important Comparator Characteristics

- Offset and hysteresis
- Sampling aperture, timing resolution, uncertainty window
- Regeneration gain, voltage sensitivity, metastability
- Random decision errors, input-referred noise

Dynamic Comparator Circuits



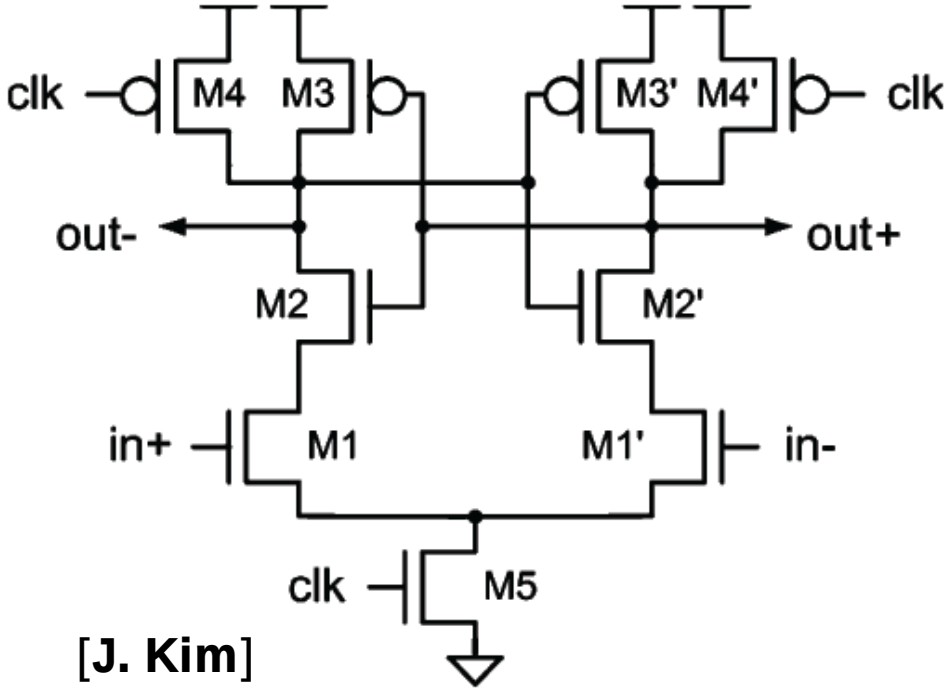
Strong-Arm Latch

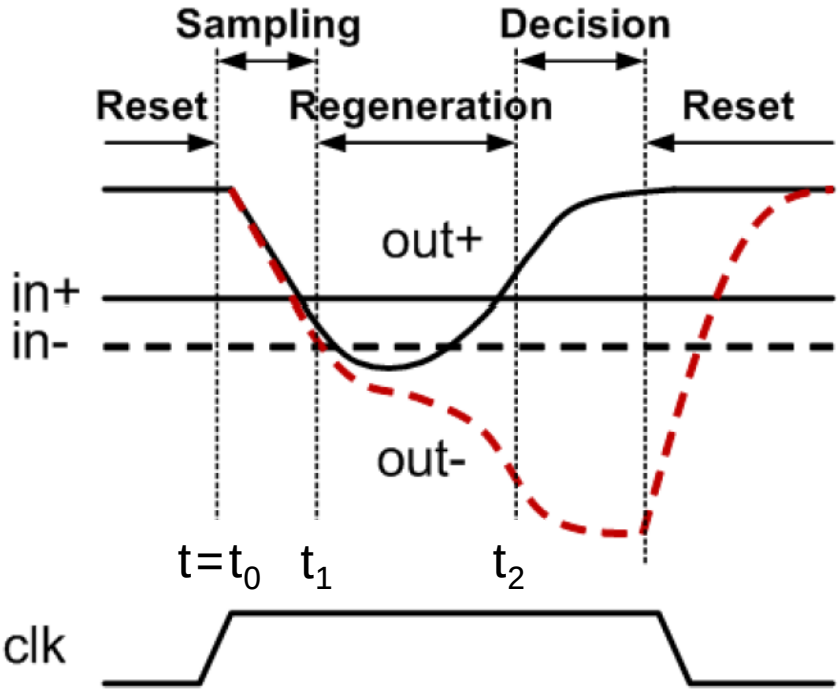


CML Latch

- To form a flip-flop
  - After strong-arm latch, cascade an R-S latch
  - After CML latch, cascade another CML latch
- Strong-Arm flip-flop has the advantage of no static power dissipation and full CMOS output levels

StrongARM Latch Operation [J. Kim TCAS1 2009]





- 4 operating phases: reset, sampling, regeneration, and decision

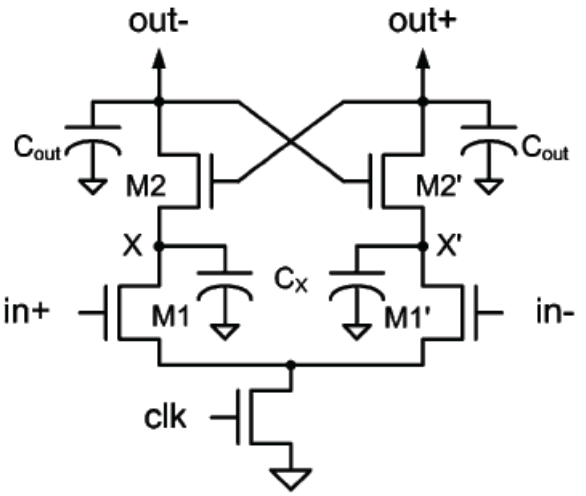
StrongARM Latch Operation – Sampling Phase [J. Kim TCAS1 2009]

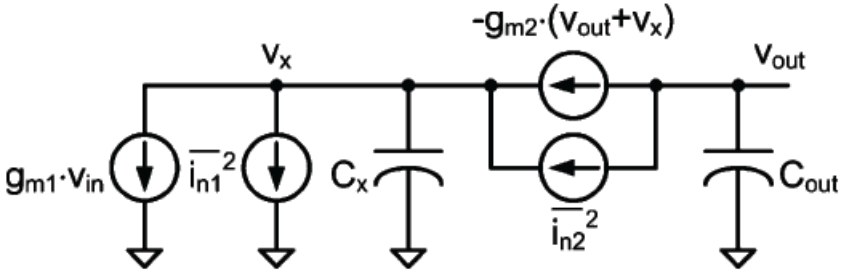
- Sampling phase starts when clk goes high, t_0, and ends when PMOS transistors turn on, t_1
- M1 pair discharges X/X'
- M2 pair discharges out+/-

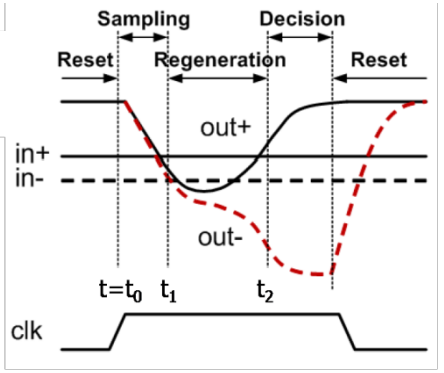
$$\frac{v_{out}(s)}{v_{in}(s)} = \frac{g_{m1}g_{m2}}{sC_{out}C_x\left(s + \frac{g_{m2}(C_{out}-C_x)}{C_{out}C_x}\right)}$$

$$\cong \frac{g_{m1}g_{m2}}{s^2 C_{out}C_x} = \frac{1}{s^2\tau_{s1}\tau_{s2}}$$

where $\tau_{s1} \equiv C_x/g_{m1}$, $\tau_{s2} \equiv C_{out}/g_{m2}$





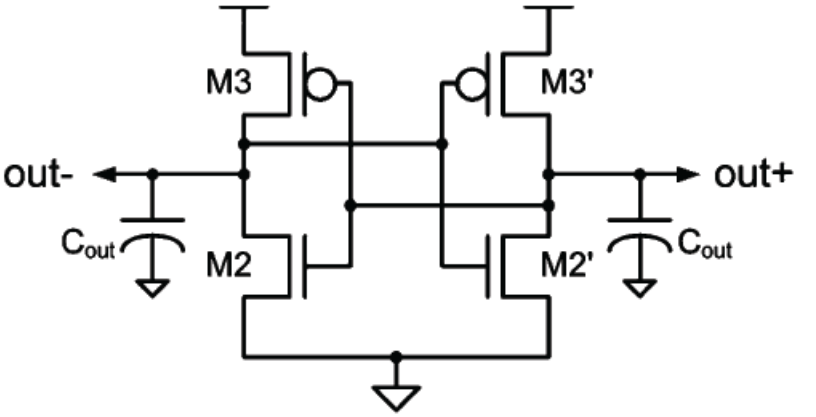


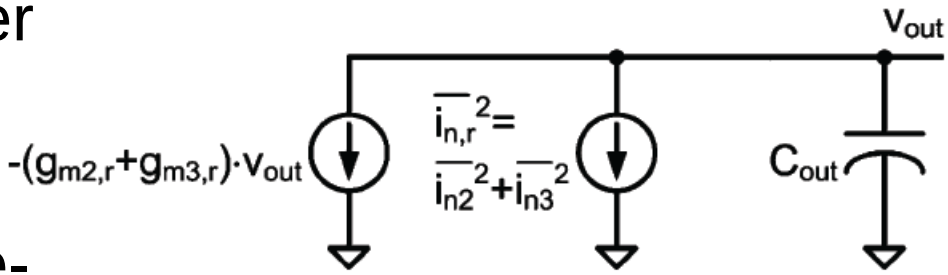
StrongARM Latch Operation – Regeneration [J. Kim TCAS1 2009]

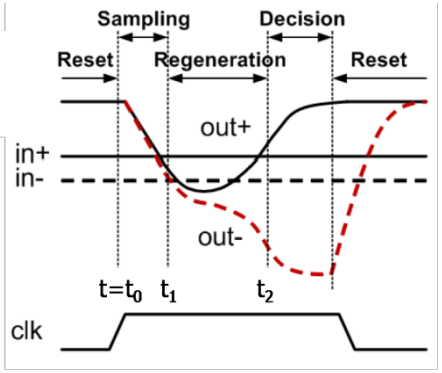
- Regeneration phase starts when PMOS transistors turn on, t_1, until decision time, t_2
- Assume M1 is in linear region and circuit no longer sensitive to v_{in}
- Cross-coupled inverters amplify signals via positive-feedback:

$$G_R = \exp\left(\frac{t_2 - t_1}{\tau_R}\right)$$

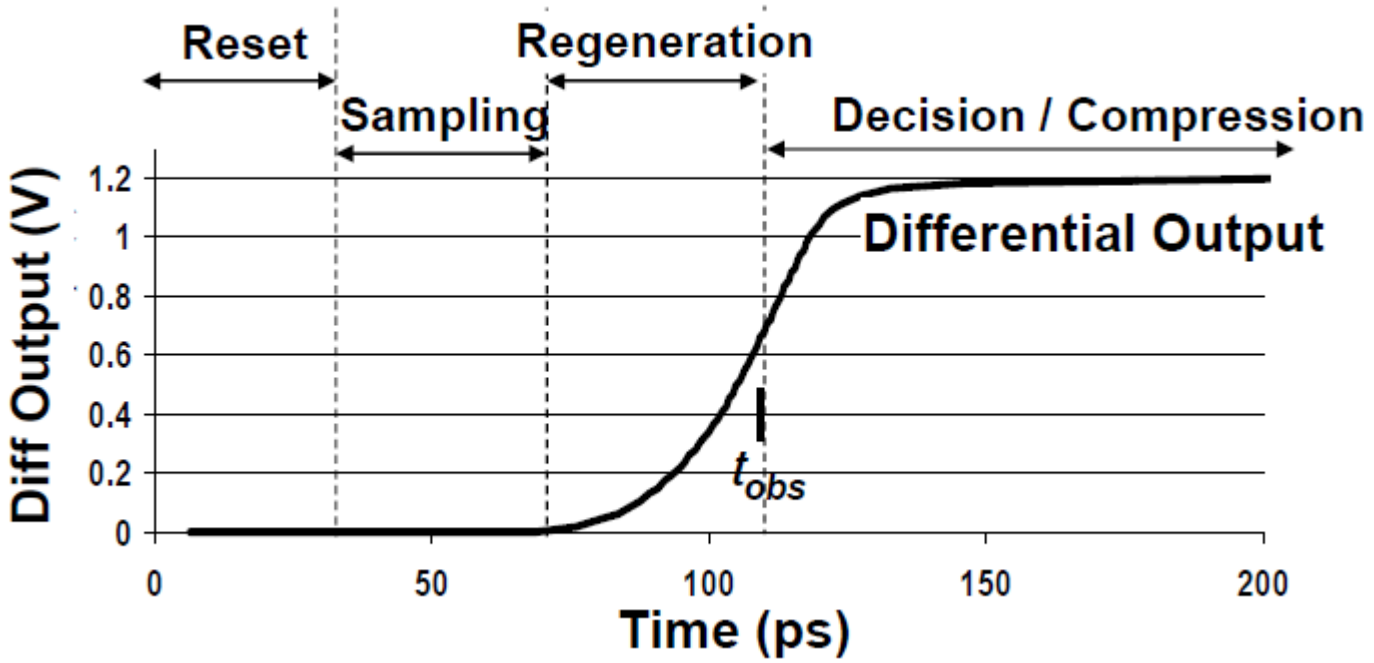
$$\tau_R = C_{out} / \left(g_{m2,r} + g_{m3,r}\right)$$







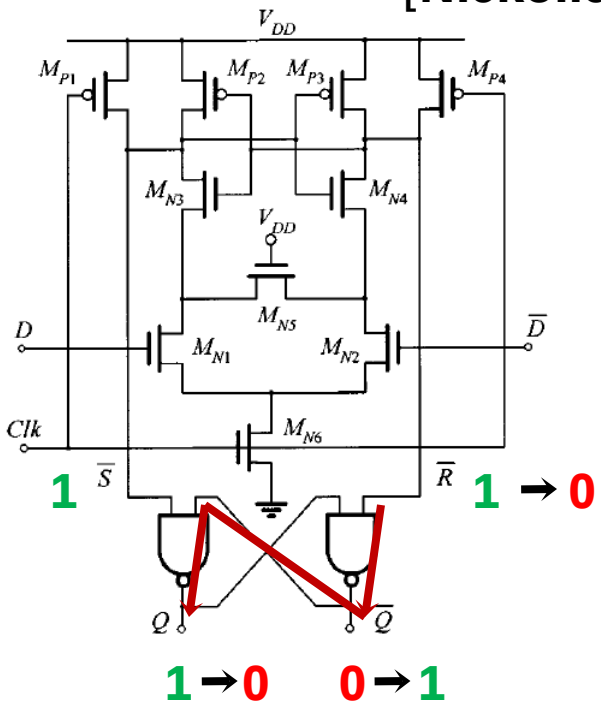
StrongARM Latch Operation – Diff. Output [J. Kim TCAS1 2009]



Conventional RS Latch

- RS latch holds output data during latch pre-charge phase
- Conventional RS latch rising output transitions first, followed by falling transition

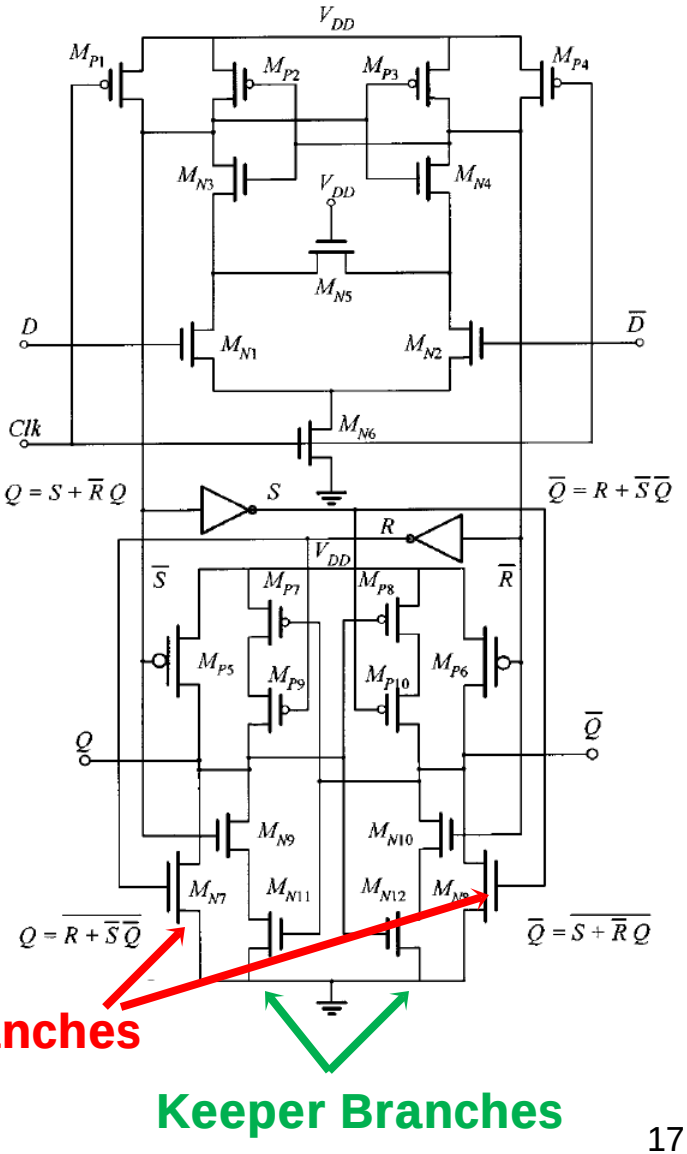
[Nickolic]



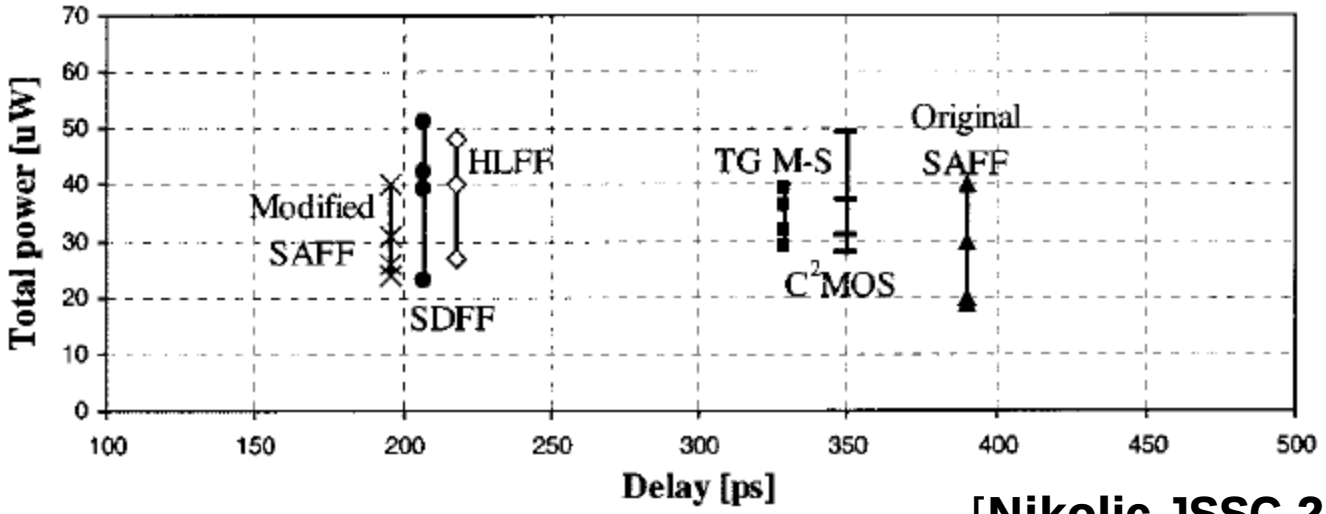
Optimized RS Latch

[Nikolic JSSC 2000]

- Optimizing RS latch for symmetric pull-up and pull-down paths allows for considerable speed-up
- Optimized RS latch consists of large driver transistors that perform the data transitions and small keeper transistors forming a cross-coupled inverter during the pre-charge state
- During evaluation, only one large driver transistor is activated to change output data and the keeper path is disabled
- During pre-charge, large driver transistors are tri-stated and small keeper cross-coupled inverter activated to hold the data

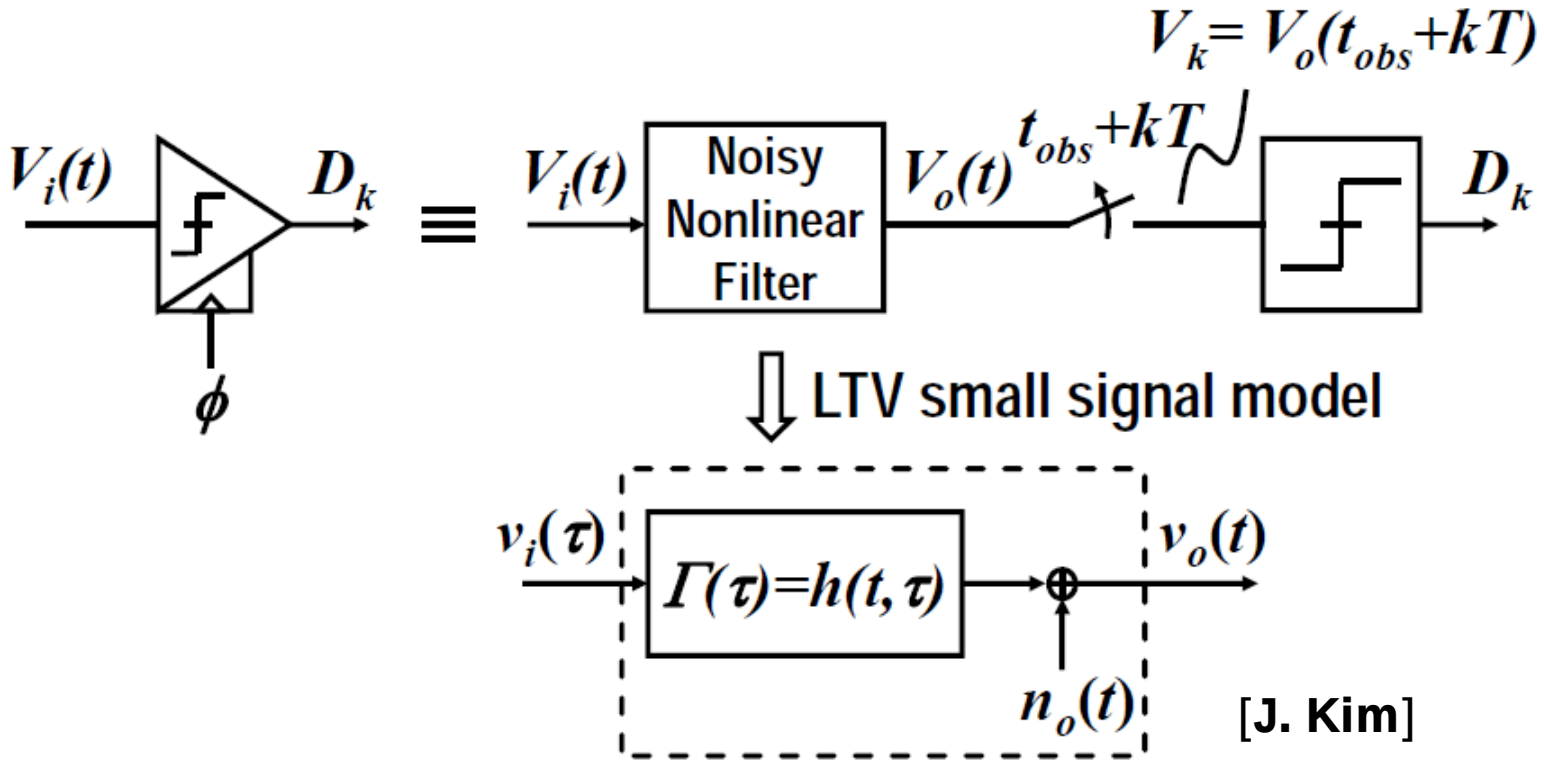


Delay Improvement w/ Optimized RS Latch



[**Nikolic JSSC 2000**]

Clocked Comparator LTV Model



- Comparator can be viewed as a noisy nonlinear filter followed by an ideal sampler and slicer (comparator)
- Small-signal comparator response can be modeled with an ISF $\Gamma(\tau) = h(t,\tau)$

Clocked Comparator ISF

- Comparator ISF is a subset of a time-varying impulse response $h(t,\tau)$ for LTV systems:

$$y(t) = \int_{-\infty}^{\infty} h(t,\tau) \cdot x(\tau) d\tau$$

  - $h(t,\tau)$: system response at t to a unit impulse arriving at τ
  - For LTI systems, $h(t,\tau)=h(t-\tau)$ (convolution)
- ISF $\Gamma(\tau)=h(t_0,\tau)$
  - For comparators, t_0 is before decision is made
  - Output voltage of comparator

$$v_o(t_{obs}) = \int_{-\infty}^{\infty} v_i(\tau) \cdot \Gamma(\tau) d\tau$$

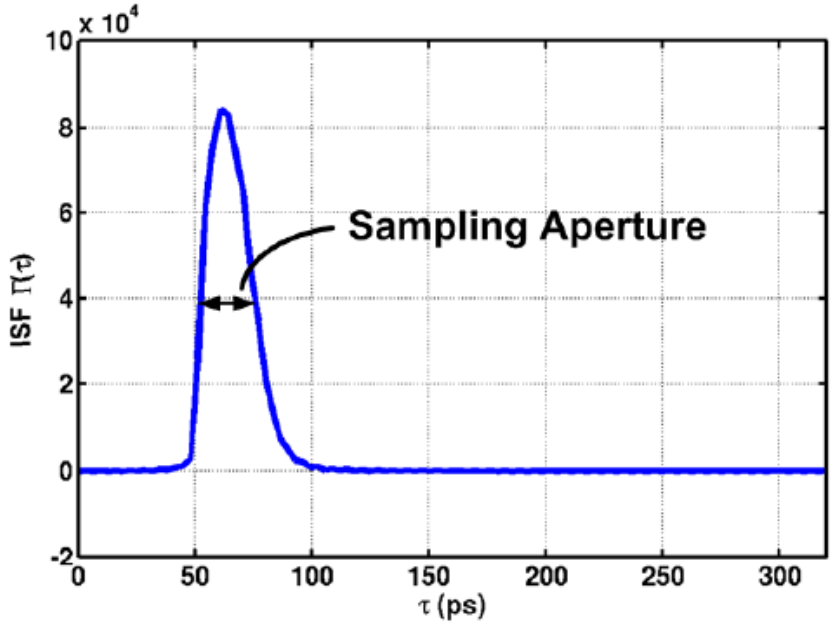
  - Comparator decision

$$D_k = \mathrm{sgn}(v_k) = \mathrm{sgn}(v_o(t_{obs} + kT)) = \mathrm{sgn}\left(\int_{-\infty}^{\infty} v_i(\tau) \cdot \Gamma(\tau) d\tau \right)$$

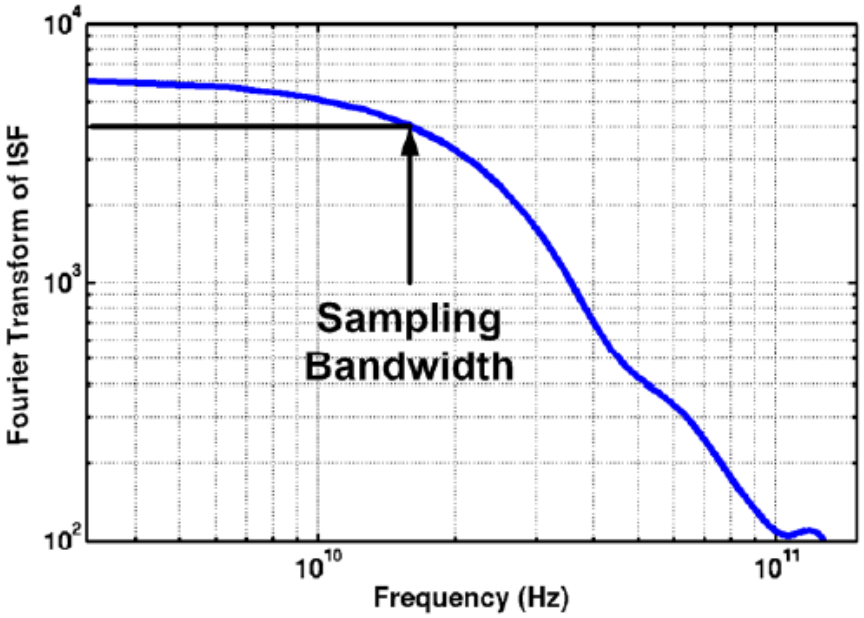
Clocked Comparator ISF

- ISF shows sampling aperture or timing resolution
- In frequency domain, it shows sampling gain and bandwidth

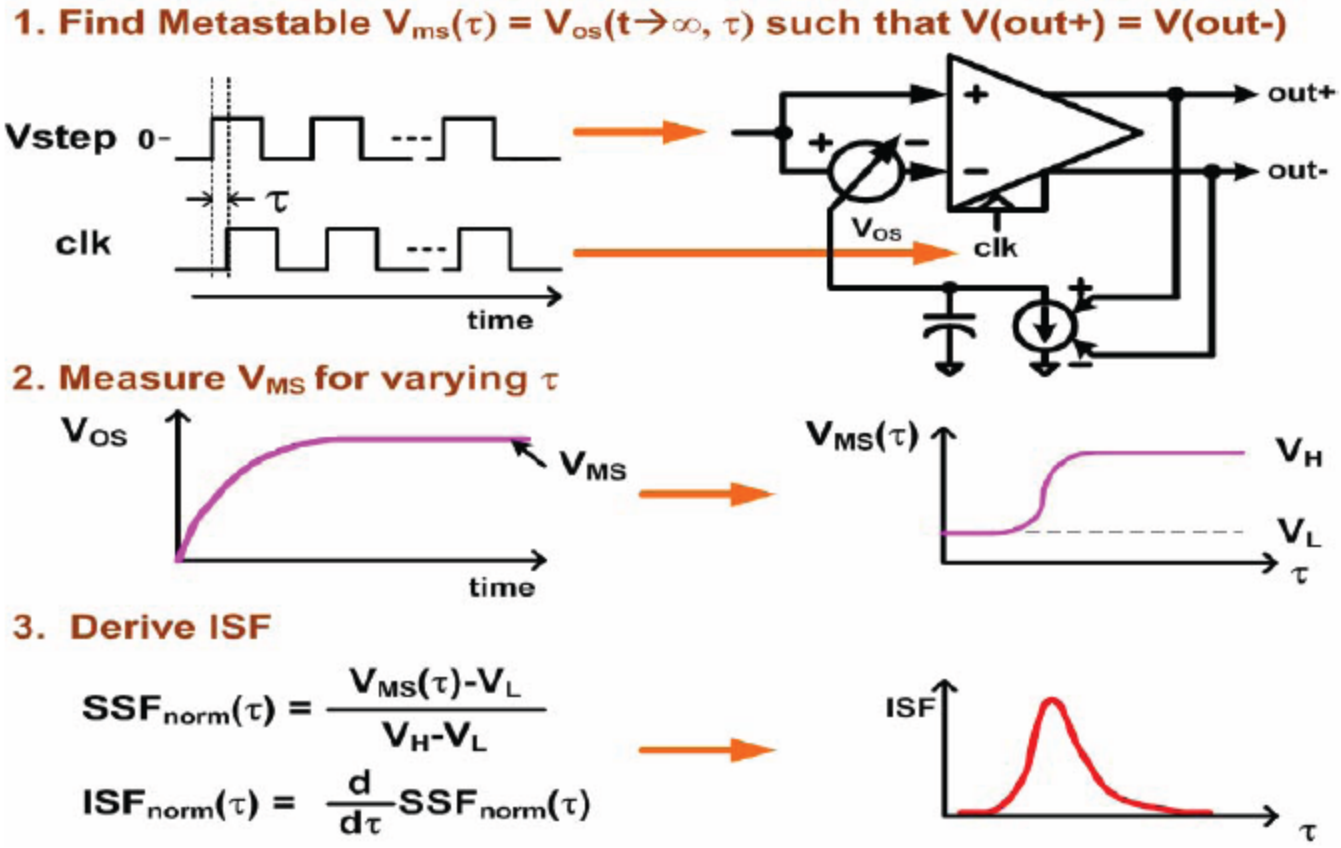
ISF $\Gamma(\tau)$



F.T. $\{\Gamma(-\tau)\}$ [J. Kim]

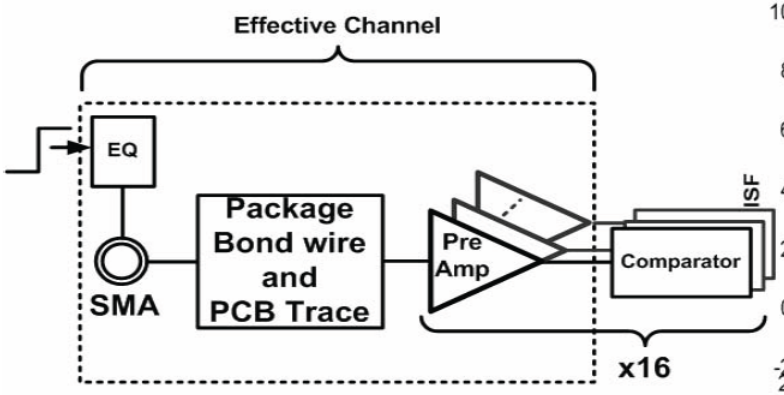


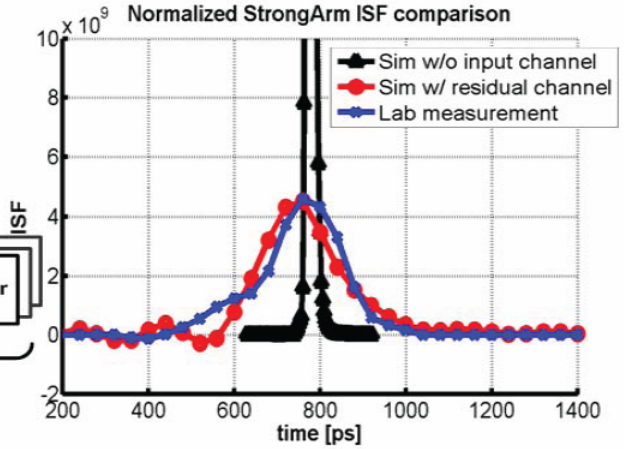
Characterizing Comparator ISF



[**Jeeradit VLSI 2008**]

Comparator ISF Measurement Setup





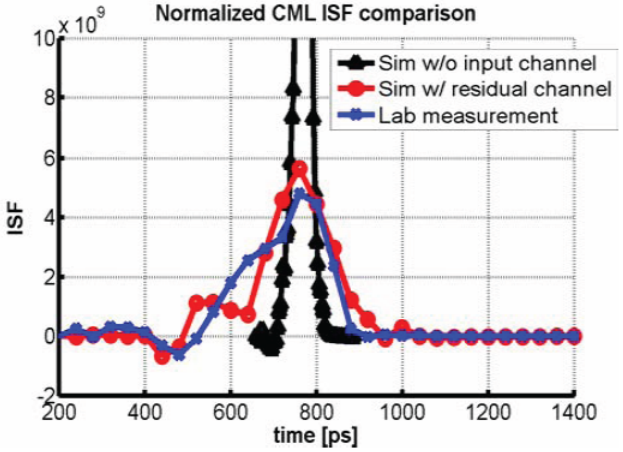
StrongARM Comparator

	Aperture Time [ps]	Sampling BW [GHz]	Sampling Gain [dB]
Sim w/o Channel	23	14.9	67.6
Sim w Channel	300	1.4	56.6
Lab	280	1.4	N/A

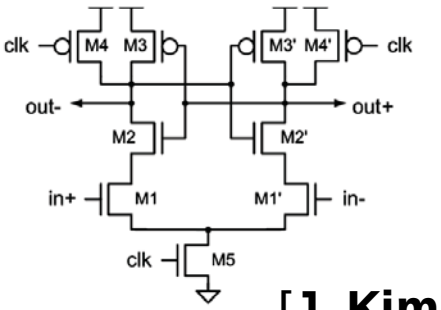
CML Comparator

	Aperture Time [ps]	Sampling BW [GHz]	Sampling Gain [dB]
Sim w/o Channel	50	6.8	88.8
Sim w Channel	300	1.4	58.0
Lab	280	1.4	N/A

Note: the aperture time is defined as the width that contains 80% of the sensitivity similar to [1]

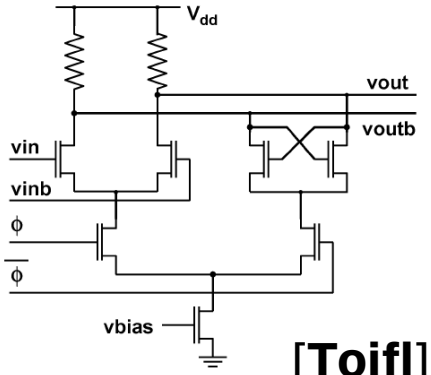


Strong-Arm Latch



[J. Kim]

CML Latch

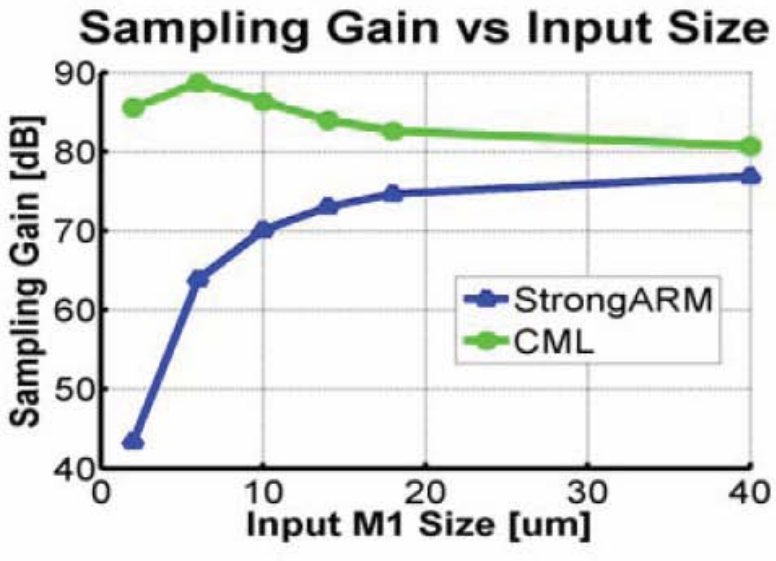


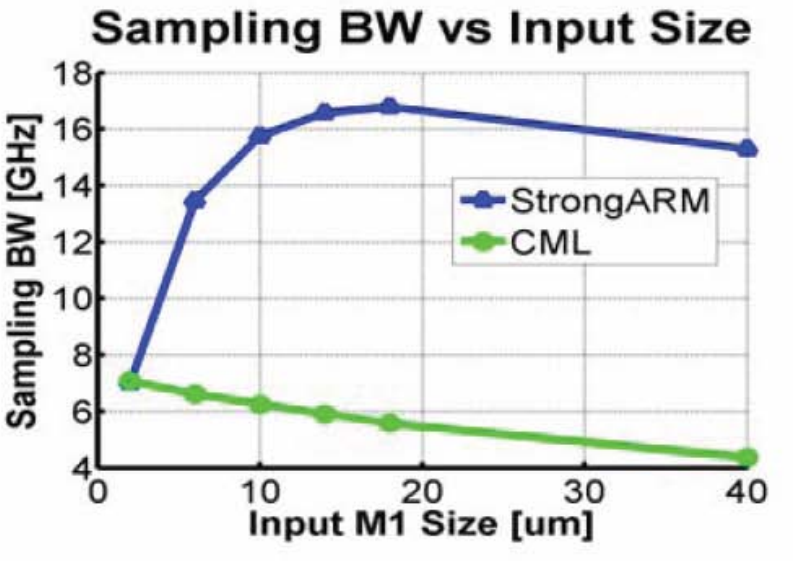
[Toifl]

[Jeeradit VLSI 2008]

Comparison of SA & CML Comparator (1)

[**Jeeradit VLSI 2008**]

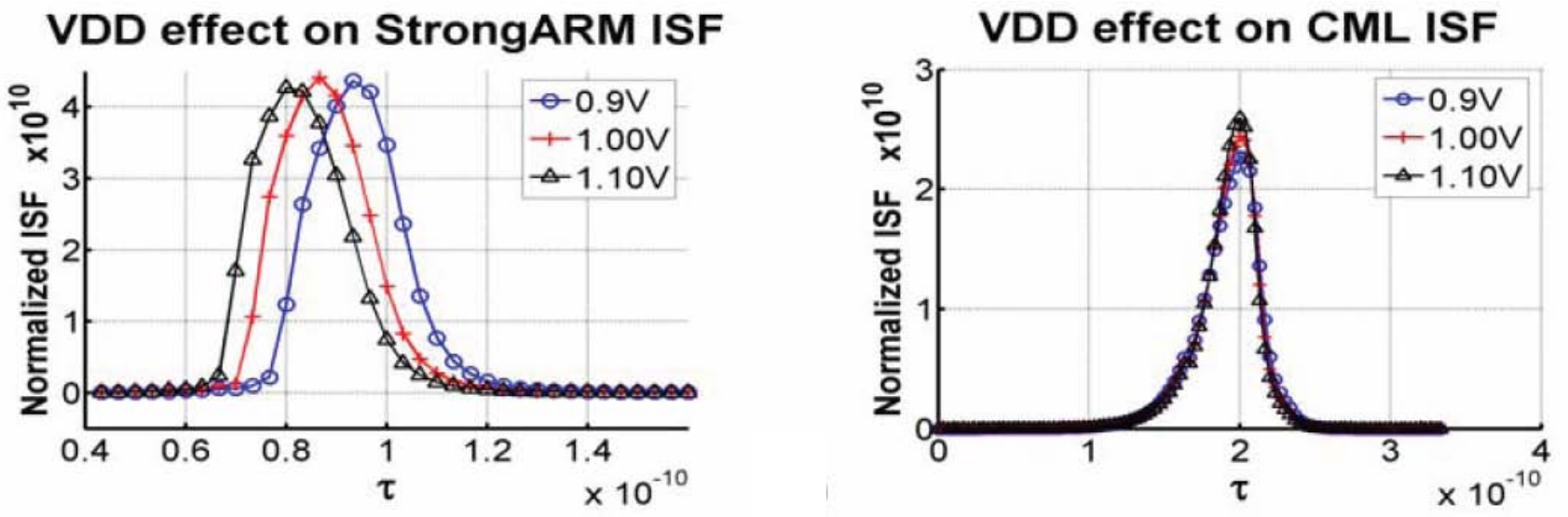




- CML latch has higher sampling gain with small input pair
- StrongARM latch has higher sampling bandwidth
  - For CML latch increasing input pair also directly increases output capacitance
  - For SA latch increasing input pair results in transconductance increasing faster than capacitance

Comparison of SA & CML Comparator (2)

[**Jeeradit VLSI 2008**]



- Sampling time of SA latch varies with VDD, while CML isn't affected much

Next Time

- Receiver Circuits
  - Clocked comparators
    - Other topologies
  - Integrating receivers
  - RX sensitivity
    - Offset correction