Lecture 12: CDRs
Announcements

• Lab 6 due Apr 12
• Project Preliminary Report due Apr 19
• Project Final Report due Apr 29
Agenda

• CDR overview
• CDR phase detectors
• Single-loop analog PLL-based CDR
• Dual-loop CDRs
• Phase interpolators
• CDR jitter properties
Embedded Clock I/O Circuits

- **TX PLL**
- **TX Clock Distribution**
- **CDR**
  - Per-channel PLL-based
  - Dual-loop w/ Global PLL &
    - Local DLL/PI
    - Local Phase-Rotator PLLs
  - Global PLL requires RX clock distribution to individual channels
A clock and data recovery system (CDR) produces the clocks to sample incoming data.

- The clock(s) must have an effective frequency equal to the incoming data rate:
  - 10GHz for 10Gb/s data rate
  - OR, multiple clocks spaced at 100ps
  - Additional clocks may be used for phase detection

- Sampling clocks should have the proper phase relationship with the incoming data for sufficient timing margin to achieve the desired bit-error-rate (BER)
- CDR should exhibit small effective jitter

[Razavi]
Embedded Clocking (CDR)

PLL-based CDR

- Clock frequency and optimum phase position are extracted from incoming data
- Phase detection continuously running
- Jitter tracking limited by CDR bandwidth
  - With technology scaling we can make CDRs with higher bandwidths and the jitter tracking advantages of source synchronous systems is diminished
- Possible CDR implementations
  - Stand-alone PLL
  - “Dual-loop” architecture with a PLL or DLL and phase interpolators (PI)
  - Phase-rotator PLL

Dual-Loop CDR

Frequency Synthesis PLL

- 800MHZ Ref Clk
- 5-stage coupled VCO
- PLL[4:0] (16Gb/s)
- PLL[4:0] (3.2GHz)

Phase-Interpolation Pairs

- 5:1 MUX
- 10
- 15

Source Synchronous System

- 5 Mux/Interpolator Pairs

Phase-Recovery Loop

- CP
- PFD
- 5 Mux/Interpolators
- FSM sel
- RX PD early/late
Agenda

- CDR overview
- CDR phase detectors
- Single-loop analog PLL-based CDR
- Dual-loop CDRs
- Phase interpolators
- CDR jitter properties
A primary difference between CDRs and PLLs is that the incoming data signal is not periodic like the incoming reference clock of a PLL.

A CDR phase detector must operate properly with missing transition edges in the input data sequence.
CDR Phase Detectors

- CDR phase detectors compare the phase between the input data and the recovered clock sampling this data and provides information to adjust the sampling clocks’ phase.
- Phase detectors can be linear or non-linear.
- Linear phase detectors provide both **sign and magnitude** information regarding the sampling phase error:
  - Hogge
- Non-linear phase detectors provide **only sign** information regarding the sampling phase error:
  - Alexander or 2x-Oversampled or Bang-Bang
  - Oversampling (>2)
  - Baud-Rate
Hogge Phase Detector

- Linear phase detector
- With a data transition and assuming a full-rate clock
  - The late signal produces a signal whose pulse width is proportional to the phase difference between the incoming data and the sampling clock
  - A Tb/2 reference signal is produced with a Tb/2 delay
- If the clock is sampling early, the late signal will be shorter than Tb/2 and vice-versa

[Razavi]
Hogge Phase Detector

- For phase transfer 0 rad is w.r.t optimal Tb/2 (π) spacing between sampling clock and data
  - $\phi_e = \phi_{in} - \phi_{clk} - \pi$

- TD is the transition density – no transitions, no information
  - A value of 0.5 can be assumed for random data

(Late – Tb/2 ref) Output Pulse Width

$K_{PD} = \frac{1}{\pi}(TD)$
PLL-Based CDR with a Hogge PD

- XOR outputs can directly drive the charge pump
- Need a relatively high-speed charge pump
Alexander (2x-Oversampled) Phase Detector

- Most commonly used CDR phase detector
- Non-linear (Binary) “Bang-Bang” PD
  - Only provides sign information of phase error (not magnitude)
- Phase detector uses 2 data samples and one “edge” sample
- Data transition necessary
  \[ D_n \oplus D_{n+1} \]
  - If “edge” sample is same as second bit (or different from first), then the clock is sampling “late”
    \[ E_n \oplus D_n \]
  - If “edge” sample is same as first bit (or different from second), then the clock is sampling “early”
    \[ E_n \oplus D_{n+1} \]
Alexander Phase Detector Characteristic (No Noise)

- Phase detector only outputs phase error sign information in the form of a late OR early pulse whose width doesn’t vary.
- Phase detector gain is ideally infinite at zero phase error.
  - Finite gain will be present with noise, clock jitter, sampler metastability, ISI.

[Diagram showing output pulse width vs. phase error, labeled as (Late – Early) by Lee]
Alexander Phase Detector Characteristic (With Noise)

- Total transfer characteristic is the convolution of the ideal PD transfer characteristic and the noise PDF
- Noise linearizes the phase detector over a phase region corresponding to the peak-to-peak jitter

\[ K_{PD} \approx \frac{2}{J_{PP}} (TD) \]

- TD is the transition density – no transitions, no information
  - A value of 0.5 can be assumed for random data
Mueller-Muller Baud-Rate Phase Detector

- Baud-rate phase detector only requires one sample clock per symbol (bit)

- Mueller-Muller phase detector commonly used

- Attempting to equalize the amplitude of samples taken before and after a pulse

Locked Condition: \( h(\tau_k - T_b) = h(\tau_k + T_b) \)

Early Clock: \( h(\tau_k - T_b) < h(\tau_k + T_b) \)

Late Clock: \( h(\tau_k - T_b) > h(\tau_k + T_b) \)
Mueller-Muller Baud-Rate Phase Detector

MM-PD is measuring the effective

\[ h_1 - h_{-1} \]

which can be computed by

\[ E[y_k \cdot d_{k-1}] - E[y_k \cdot d_{k+1}] \]

- If this is positive, then the effective post-cursor ISI is too high and we are sampling too early
- If this is negative, then the effective pre-cursor ISI is too high and we are sampling too late

Locked Condition: \( h(\tau_k - T_b) = h(\tau_k + T_b) \)

Early Clock: \( h(\tau_k - T_b) < h(\tau_k + T_b) \)

Late Clock: \( h(\tau_k - T_b) > h(\tau_k + T_b) \)
Comparing the current sample versus the desired reference level ($e_n$) and correlating that with the appropriate data sample ($d_n$) gives pre/post-cursor information.

This requires additional error samplers with $|V_{REF}|$ thresholds.

- $e_n$ gives $d_{n-1}$ post-cursor ($h_1$) information.
- $e_{n-1}$ gives $d_n$ pre-cursor ($h_{-1}$) information.
Mueller-Muller Baud-Rate Phase Detector

- Simplified MM-PD only considers transition patterns
- If consecutive error samples are different, phase error polarity is given by $e_j$
Agenda

- CDR overview
- CDR phase detectors
- Single-loop analog PLL-based CDR
- Dual-loop CDRs
- Phase interpolators
- CDR jitter properties
Analog PLL-based CDR

Model of PD

Model of Loop Filter

Model of VCO

"Linearized" \( K_{PD} \)

\[ \phi_{out} = \frac{s \cdot K_P \cdot K_{PD} \cdot K_{VCO} + K_i \cdot K_{PD} \cdot K_{VCO}}{s^2 + s \cdot K_P \cdot K_{PD} \cdot K_{VCO} + K_i \cdot K_{PD} \cdot K_{VCO}} \]

\[ \phi_{in} \]

[Lee]

\[ K_P = I_C \cdot R \quad K_i = \frac{I_C}{C} \quad \omega_n = \sqrt{K_i \cdot K_{PD} \cdot K_{VCO}} \quad \zeta = \frac{K_P}{K_i} \cdot \frac{\omega_n}{2} \]
Analog PLL-based CDR

- CDR “bandwidth” will vary with input phase variation amplitude with a non-linear phase detector
- Final performance verification should be done with a time-domain non-linear model

[Lee]
56Gb/s PAM4 Analog PLL-based CDR

- Quarter-rate architecture
- 3 data samplers for PAM4 detection
- 1 edge sampler for CDR and DFE adaptation
- 1 error sampler for threshold adaptation

[Roshan-Zamir JSSC 2019]
56Gb/s PAM4 Analog PLL-based CDR

- PLL-based CDR to reduce power consumption
- Bang-bang phase detector works on symmetric PAM4 transitions to minimize detection errors
- Parallel charge pumps minimize logic and loop delay

[Roshan-Zamir JSSC 2019]
56Gb/s PAM4 Analog PLL-based CDR

- LC-VCO w/ additional source LC filter improves phase noise
- 8-phase quarter-rate clock
  - CML divider
  - 2X oversampling clock

[Roshan-Zamir JSSC 2019]
Agenda

- CDR overview
- CDR phase detectors
- Single-loop analog PLL-based CDR
- Dual-loop CDRs
- Phase interpolators
- CDR jitter properties
Single-Loop CDR Issues

- Phase detectors have limited frequency acquisition range
  - Results in long lock times or not locking at all
  - Can potentially lock to harmonics of correct clock frequency
- VCO frequency range variation with process, voltage, and temperature can exceed PLL lock range if only a phase detector is employed
Phase Interpolatorator (PI) Based CDR

- Frequency synthesis loop can be a global PLL

- Can be difficult to distribute multiple phases long distance
  - Need to preserve phase spacing
  - Clock distribution power increases with phase number
  - If CDR needs more than 4 phases consider local phase generation

![Diagram showing 1/4 Rate Dual-Loop CDR](image-url)
DLL Local Phase Generation

- Only differential clock is distributed from global PLL
- Delay-Locked Loop (DLL) locally generates the multiple clock phases for the phase interpolators
  - DLL can be per-channel or shared by a small number (4)
- Same architecture can be used in a forwarded-clock system
  - Replace frequency synthesis PLL with forwarded-clock signals

\[ \frac{1}{4} \text{ Rate Dual-Loop CDR} \]

- Frequency Synthesis PLL
- CP
- PFD
- Ref Clk
- Differential PLL output (180°)

- Local DLL
  - \( \Phi_{PLL}[0] \)
  - \( \Phi_{PLL}[0] \)
- Differential PLL output (180°)

- 4:1 MUX
- 4 Differential Mux/Interpolator Pairs
- \( \Psi[3:0] \) & \( \Psi'[3:0] \)
- 8 phases spaced at 45°

- RX PD
- early/late
- FSM
- sel

Phase-Recovery Loop
Phase Rotator PLL

- Phase interpolators can be expensive in terms of power and area.
- Phase rotator PLL places one interpolator in PLL feedback to adjust all VCO output phases simultaneously.
- Now frequency synthesis and phase recovery loops are coupled.
  - Need PLL bandwidth greater than phase loop.
    - Useful in filtering VCO noise.
Agenda

- CDR overview
- CDR phase detectors
- Single-loop analog PLL-based CDR
- Dual-loop CDRs
- Phase interpolators
- CDR jitter properties
Phase Interpolators

- Phase interpolators realize digital-to-phase conversion (DPC)
- Produce an output clock that is a weighted sum of two input clock phases
- Common circuit structures
  - Tail current summation interpolation
  - Voltage-mode interpolation
- Interpolator code mapping techniques
  - Sinusoidal
  - Linear
Sinusoidal Phase Interpolation

- Arbitrary phase shift can be generated with linear summation of I/Q clock signal

\[
X_I = A \sin(\omega t)
\]

\[
X_Q = A \sin(\omega t - \pi / 2) = -A \cos(\omega t)
\]

\[
Y = A \sin(\omega t - \phi)
\]

\[
= A \cos(\phi) \sin(\omega t) - A \sin(\phi) \cos(\omega t)
\]

\[
= \cos(\phi)X_I + \sin(\phi)X_Q = a_1X_I + a_2X_Q
\]

\[
Y = A \sin(\omega t - \phi) = a_1X_I + a_2X_Q
\]

where \( a_1 = \cos(\phi) \) and \( a_2 = \sin(\phi) \)

\[
a_1^2 + a_2^2 = 1
\]
Sinusoidal vs Linear Phase Interpolation

- It can be difficult to generate a circuit that implements sinusoidal weighting
  \[ a_1^2 + a_2^2 = 1 \]
- In practice, a linear weighting is often used
  \[ a_1 + a_2 = 1 \]
Phase Interpolator Model

- Interpolation linearity is a function of the phase spacing, $\Delta t$, to output time constant, $RC$, ratio.
- Important that interpolator output time constant is not too small (fast) for phase mixing quality.

$[\text{Weinlader}]$

Small output $\tau$

Large output $\tau$
Phase Interpolator Model

w/ ideal step inputs

\[ V_o(t) = V_{cc} + R \cdot I \cdot \left( (1 - \alpha) \cdot u(t) \cdot \left( e^{\frac{t}{RC}} - 1 \right) + \alpha \cdot u(t - \Delta t) \cdot \left( e^{\frac{t - \Delta t}{RC}} - 1 \right) \right) \]

w/ finite input transition time

\[ V_o(t) = V_{cc} + (1 - \alpha) \cdot \frac{I_{max} \cdot t}{\Delta t} \cdot R \cdot \alpha \cdot [u(t) - u(t - \Delta t)] \cdot \left( e^{\frac{t}{RC}} - 1 \right) + \]

\[ \alpha \cdot \frac{I_{max} \cdot t}{\tau_r} \cdot R \cdot [u(t - \Delta t) - u(t - 3\Delta t)] \cdot \left( e^{\frac{t - \Delta t}{RC}} - 1 \right). \]

For more details see D. Weinlader’s Stanford PhD thesis
Tail-Current Summation PI

[Bulzacchelli JSSC 2006]

- Control of I/Q polarity allows for full 360° phase rotation with phase step determined by resolution of weighting DAC
- For linearity over a wide frequency range, important to control either input or output time constant (slew rate)
For linearity over a wide frequency range, important to control either input or output time constant (slew rate)
Delay-Locked Loop (DLL)

- DLLs lock delay of a voltage-controlled delay line (VCDL)
- Typically lock the delay to 1 or ½ input clock cycles
  - If locking to ½ clock cycle the DLL is sensitive to clock duty cycle
- DLL does not self-generate the output clock, only delays the input clock

[Sidiropoulos JSSC 1997]
Voltage-Controlled Delay Line

[Sidiropoulos]
DLL Delay Transfer Function

\[ D_O(s) = (D_I(s) - D_O(s)) \cdot F_{REF} \cdot \frac{I_{CH}}{sC_1} \cdot K_{DL} \]

\[ \frac{D_O(s)}{D_I(s)} = \frac{1}{1 + s/\omega_N} \]

\[ \omega_N = I_{CH} \cdot K_{DL} \cdot F_{REF} \cdot \frac{1}{C_1} \]

- First-order loop as delay line doesn’t introduce a (low-frequency) pole
- The delay between reference and feedback signal is low-pass filtered
- Unconditionally stable as long as continuous-time approximation holds, i.e. \( \omega_n < \omega_{ref}/10 \)
Agenda

• CDR overview
• CDR phase detectors
• Single-loop analog PLL-based CDR
• Dual-loop CDRs
• Phase interpolators
• CDR jitter properties
  • Jitter transfer
  • Jitter generation
  • Jitter tolerance
CDR Jitter Model

\[
\frac{\phi_{out}}{\phi_{in}} = \frac{s \cdot K_P \cdot K_{PD} \cdot K_{VCO} + K_i \cdot K_{PD} \cdot K_{VCO}}{s^2 + s \cdot K_P \cdot K_{PD} \cdot K_{VCO} + K_i \cdot K_{PD} \cdot K_{VCO}}
\]

\[
K_P = I_C \cdot R \quad K_i = \frac{I_C}{C} \quad \omega_n = \sqrt{K_i \cdot K_{PD} \cdot K_{VCO}} \quad \zeta = \frac{K_P}{K_i} \cdot \frac{\omega_n}{2}
\]
Jitter Transfer

- Jitter transfer is how much input jitter “transfers” to the output
  - If the PLL has any peaking in the phase transfer function, this jitter can actually be amplified

\[
\frac{\phi_{out}}{\phi_{in}} = \frac{s \cdot K_P \cdot K_{PD} \cdot K_{VCO} + K_i \cdot K_{PD} \cdot K_{VCO}}{s^2 + s \cdot K_P \cdot K_{PD} \cdot K_{VCO} + K_i \cdot K_{PD} \cdot K_{VCO}}
\]
Jitter Transfer Measurement

\[ JTF(f) = 20 \log \left( \frac{OutputJitter(f)}{InputJitter(f)} \right) \]

[TrV89] [RaO91] [Walker]
Jitter Transfer Specification

This specification is intended to control jitter peaking in long repeater chains.
Jitter Generation

- Jitter generation is how much jitter the CDR “generates”
  - Assumed to be dominated by VCO
  - Assumes jitter-free serial data input

VCO Phase Noise:

\[ H_{nyco}(s) = \frac{\phi_{out}}{\phi_{nyco}} = \frac{s^2}{s^2 + \left( \frac{K_{Loop}}{N} \right) RCs + \frac{K_{Loop}}{N}} = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \]

For CDR, \( N \) should be 1
Jitter Generation

High-Pass Transfer Function

- SONET specification:
  - rms output jitter ≤ 0.01 UI

Jitter accumulates up to time \( \propto \frac{1}{\text{PLL bandwidth}} \)

\[ \text{rms jitter} [\mu\text{s}] \]

\[ \sqrt{2\sigma_x} \]

\[ k \sqrt{\Delta T} \]

[McNeill]
Jitter Tolerance

- How much sinusoidal jitter can the CDR “tolerate” and still achieve a given BER?

\[
\phi_e(s) = \left(1 - \frac{\phi_{out}(s)}{\phi_{in}(s)}\right)\phi_{n.in}(s) \leq \frac{\text{Timing Margin}}{2}
\]

\[
JTOL(s) = 2\phi_{n.in}(s) = \frac{TM}{1 - \frac{\phi_{out}(s)}{\phi_{in}(s)}}
\]

[Sheikholeslami]

[Lee]
Random and sinusoidal jitter are added by modulating the BERT clock.

Deterministic jitter is added by passing the data through the channel.

For a given frequency, sinusoidal jitter amplitude is increased until the minimum acceptable BER (10^{-12}) is recorded.
Jitter Tolerance Measurement

\[ JTOL(s) = 2\phi_{n.in}(s) = \frac{TM}{1 - \frac{\phi_{out}(s)}{\phi_{in}(s)}} \]

Flat region is beyond CDR bandwidth

(within CDR bandwidth)
CDR Take-Away Points

- CDRs extract the proper clock frequency and phase position to sample the incoming data symbols
- Specialized phase detectors suited for random data symbols are required
- Dual-loop CDRs are often used to both optimize jitter performance and provide robust frequency acquisition
- Jitter tolerance is an important CDR metric that is improved with increased loop bandwidth
Next Time

- Forwarded-Clock Deskew Circuits
- Clock Distribution Techniques