ECEN689: Special Topics in High-Speed Links Circuits and Systems Spring 2010

Lecture 12: TX Multiplexer Circuits

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Announcements

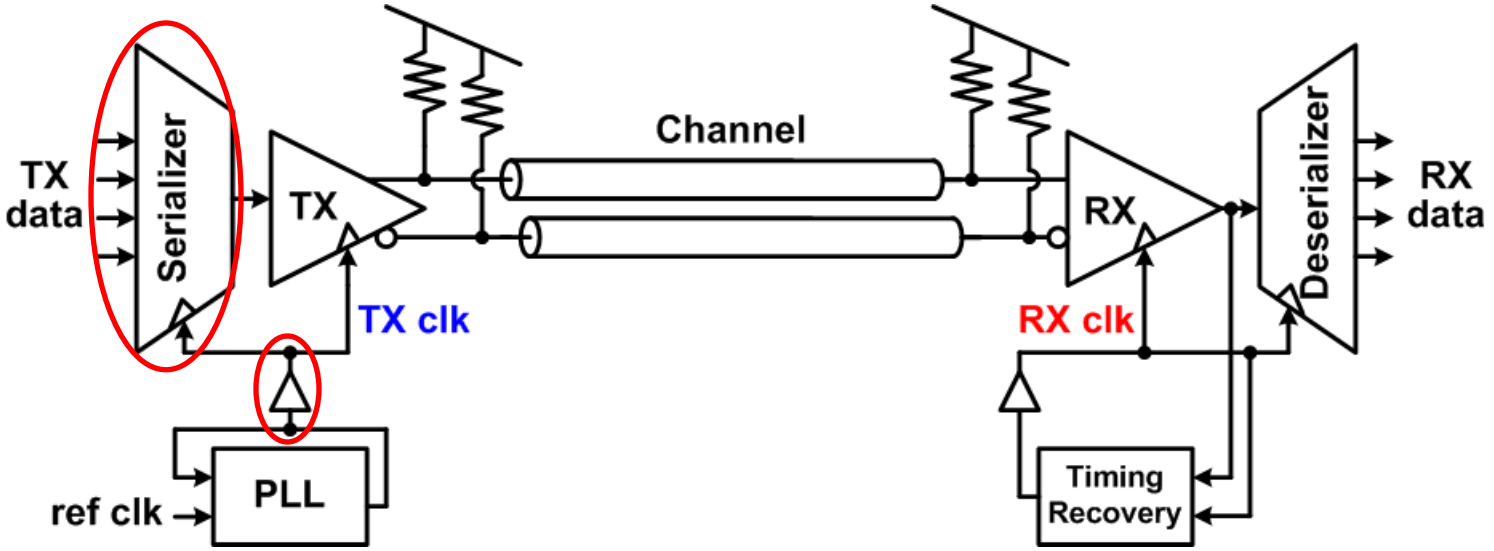
- HW3 is posted on website and due Wednesday
- Exam 1 is scheduled for March 12
  - 9:10-10:10AM (10 extra minutes)
  - Anybody have class directly after this one?
  - Closed book w/ one standard note sheet
    - 8.5”x11” front & back
  - Bring your calculator
- Reading
  - Dally 11.1-11.3
  - Will post some papers on TX drivers and RX comparator analysis

Agenda

- TX circuit speed limitations
  - Clock distribution
  - Multiplexing techniques
- RX Circuits

TX Circuit Speed Limitations

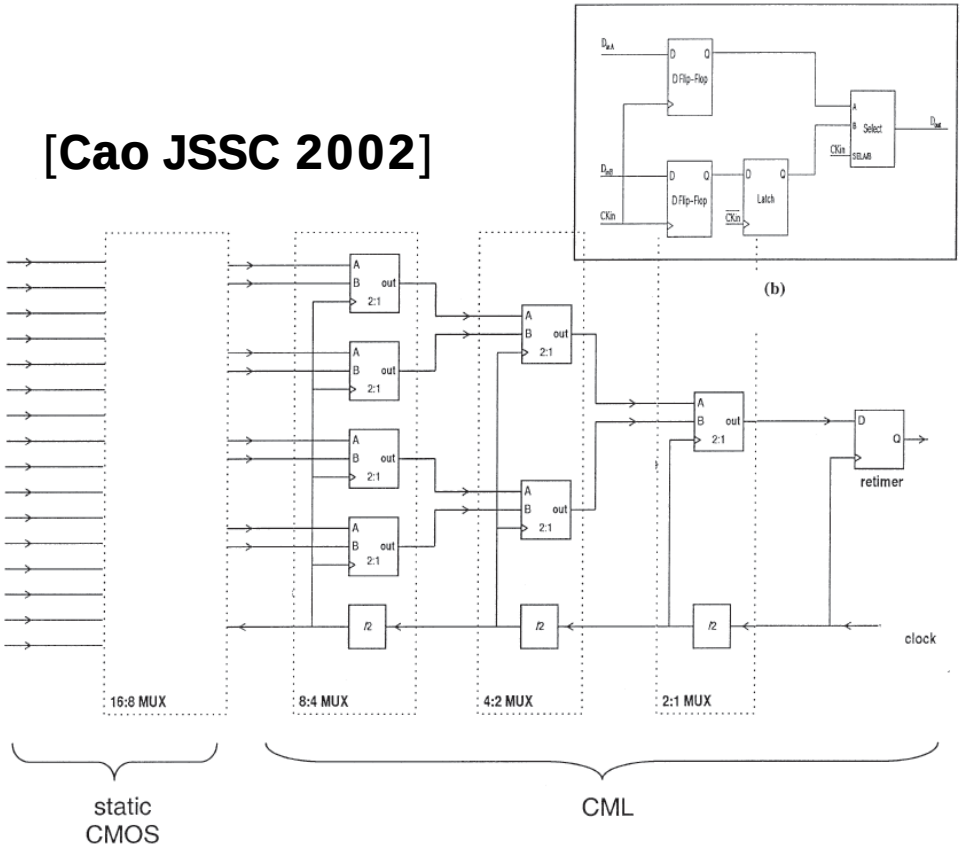
- High-speed links can be limited by both the channel and the circuits
- Clock generation and distribution is key circuit bandwidth bottleneck
- Multiplexing circuitry also limits maximum data rate



TX Multiplexer

- Tree-mux architecture with cascaded 2:1 stages often used
- CML logic sometimes used in last stages
  - Minimize CML to save power
- Full-rate architecture relaxes clock duty-cycle, but limits max data rate

[**Cao JSSC 2002**]

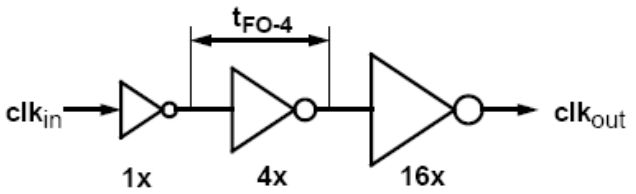


- 10Gb/s in 0.18μm CMOS
- Full-rate architecture
- 130mW!!

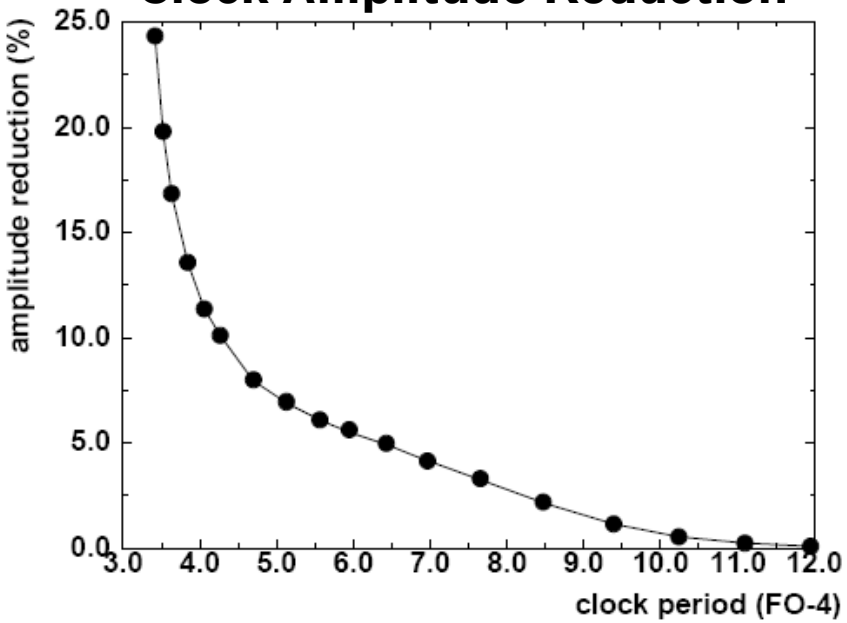
Clock Distribution Speed Limitations

- Max clock frequency that can be efficiently distributed is limited by clock buffers ability to propagate narrow pulses
- CMOS buffers are limited to a min clock period near 8FO4 inverter delays
  - About 4GHz in typical 90nm CMOS
  - Full-rate architecture limited to this data rate in Gb/s
- Need a faster clock → use faster clock buffers
  - CML
  - CML w/ inductive peaking

t_{FO4} in 90nm ~ 30ps



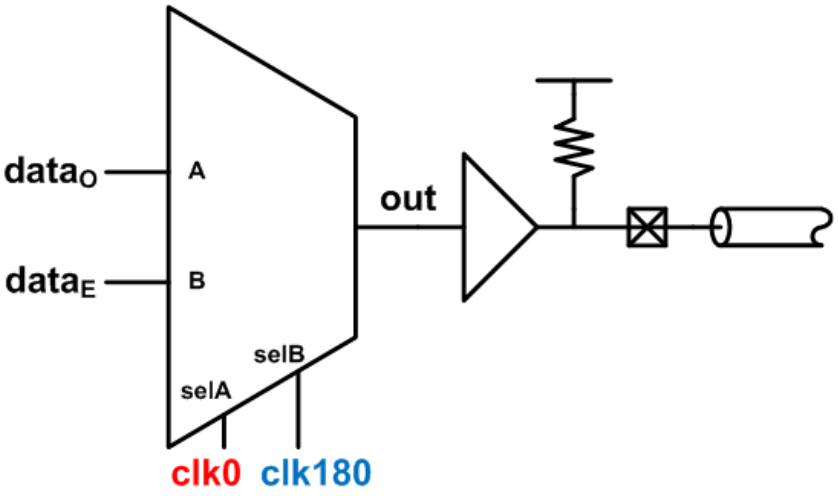
Clock Amplitude Reduction*

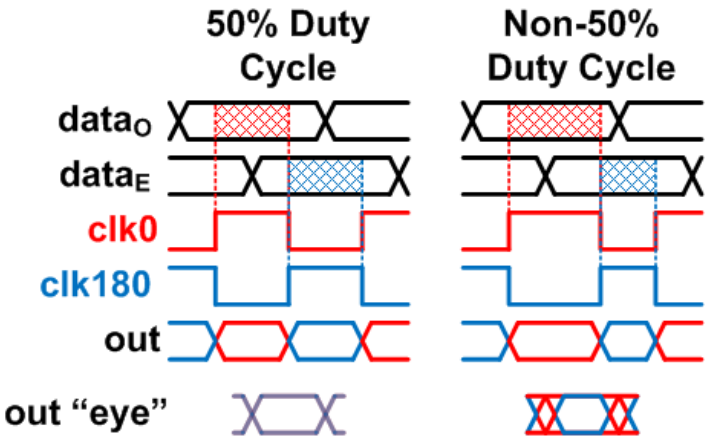


*C.-K. Yang, "Design of High-Speed Serial Links in CMOS," 1998.

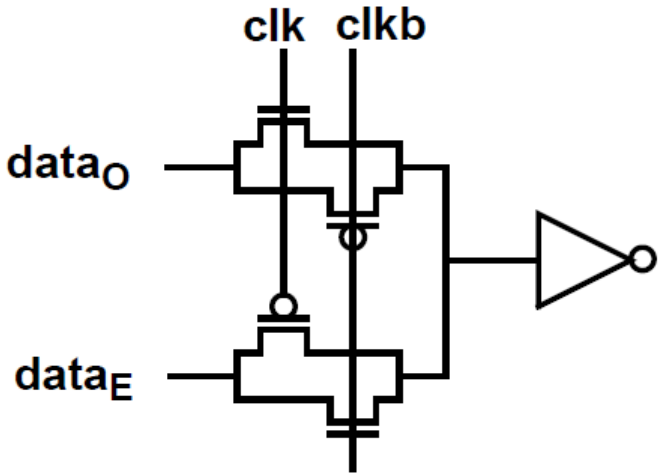
Multiplexing Techniques – ½ Rate

- Full-rate architecture is limited by maximum clock frequency to 8FO4 T_b
- To increase data rates eliminate final retiming and use multiple phases of a slower clock to mux data
- Half-rate architecture uses 2 clock phases separated by 180° to mux data
  - Allows for 4FO4T_b
  - 180° phase spacing (duty cycle) critical for uniform output eye





2:1 CMOS Mux



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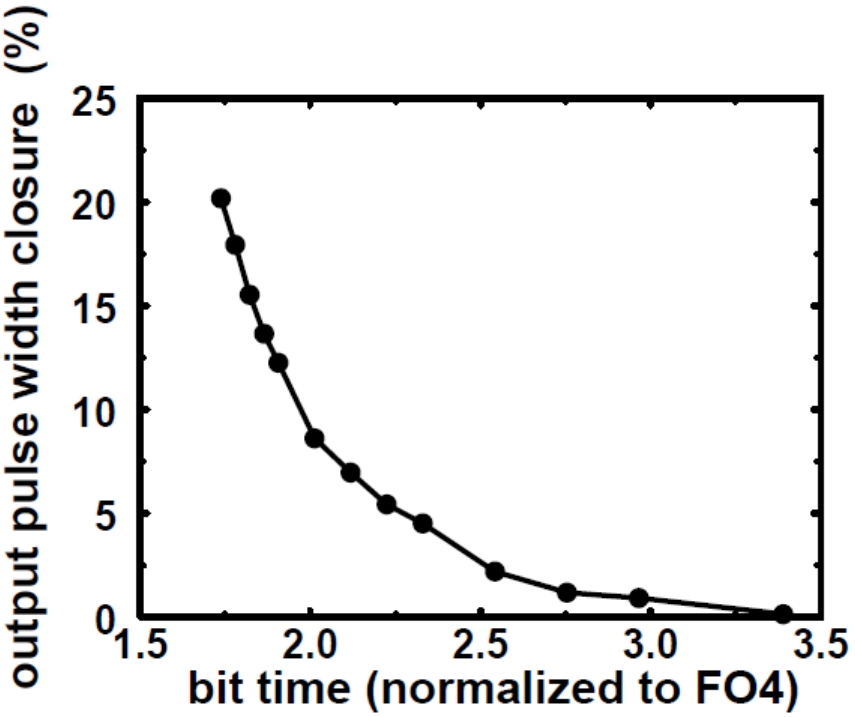
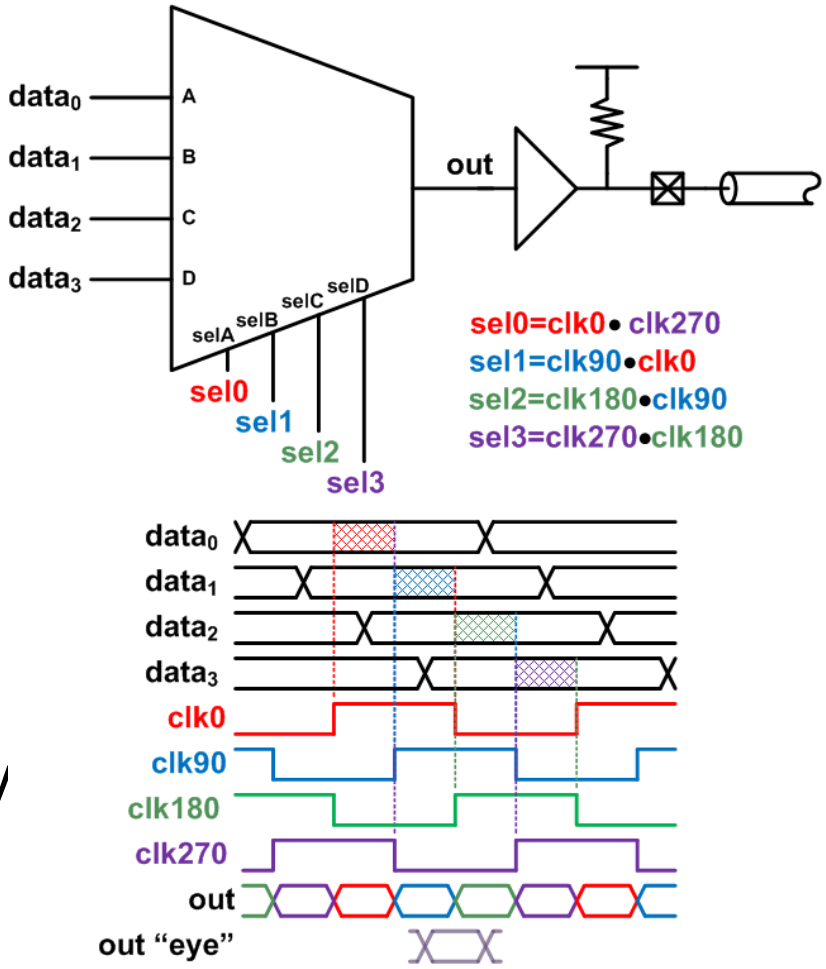


- 2:1 CMOS mux able to propagate a minimum pulse near 2FO4 T_b
- However, with a ½-rate architecture still limited by clock distribution to 4FO4 T_b
  - 8Gb/s in typical 90nm

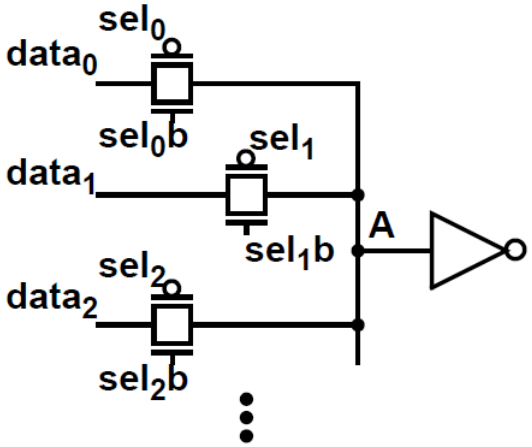
Increasing Multiplexing Factor – ¼ Rate

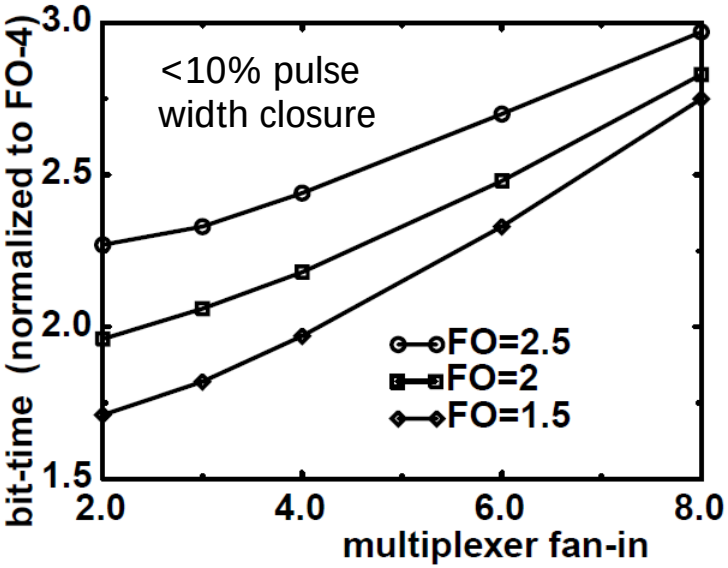
- Increase multiplexing factor to allow for lower frequency clock distribution
- ¼-rate architecture
  - 4-phase clock distribution spaced at 90° allows for 2FO4 Tb
  - 90° phase spacing and duty cycle critical for uniform output eye



Increasing Multiplexing Factor – Mux Speed

- Higher fan-in muxes run slower due to increased cap at mux node
- ¼-rate architecture
  - 4:1 CMOS mux can potentially achieve 2FO4 T_b with low fanout
    - An aggressive CMOS-style design has potential for 16Gb/s in typical 90nm CMOS
- 1/8-rate architecture
  - 8-phase clock distribution spaced at 45° allows for 1FO4 Tb
  - No way a CMOS mux can achieve this!!





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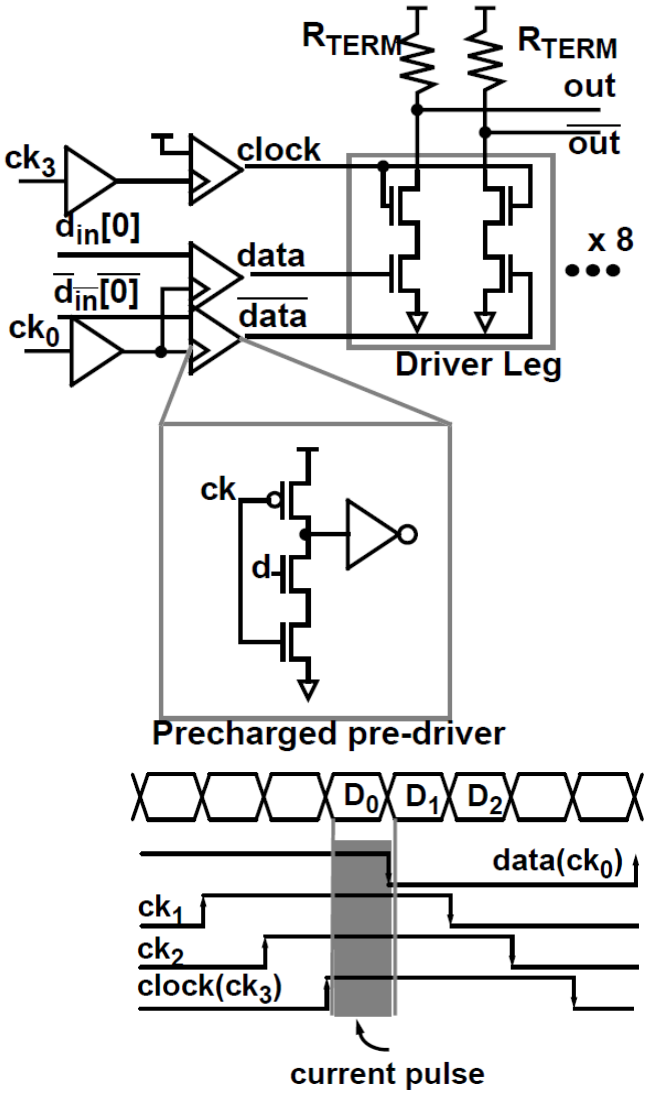
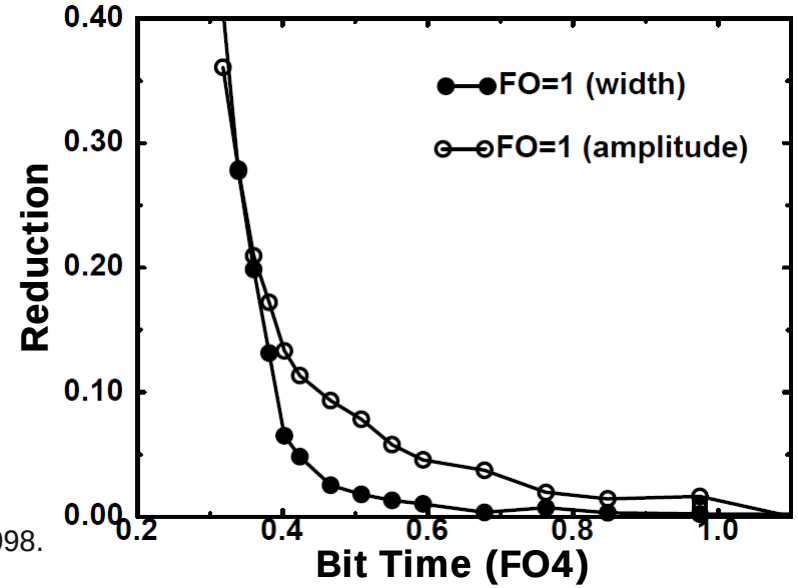
High-Order Current-Mode Output-Multiplexed



- 8:1 current-mode mux directly at output pad
- Makes sense if output time constant smaller than on-chip time constant

$$\tau_{out} = 25\Omega \times C_{out}$$

- Very sensitive to clock phase spacing
- Yang achieved 6Gb/s in 0.35μm CMOS
  - Equivalent to 33Gb/s in 90nm CMOS (now channel (not circuit) limited)



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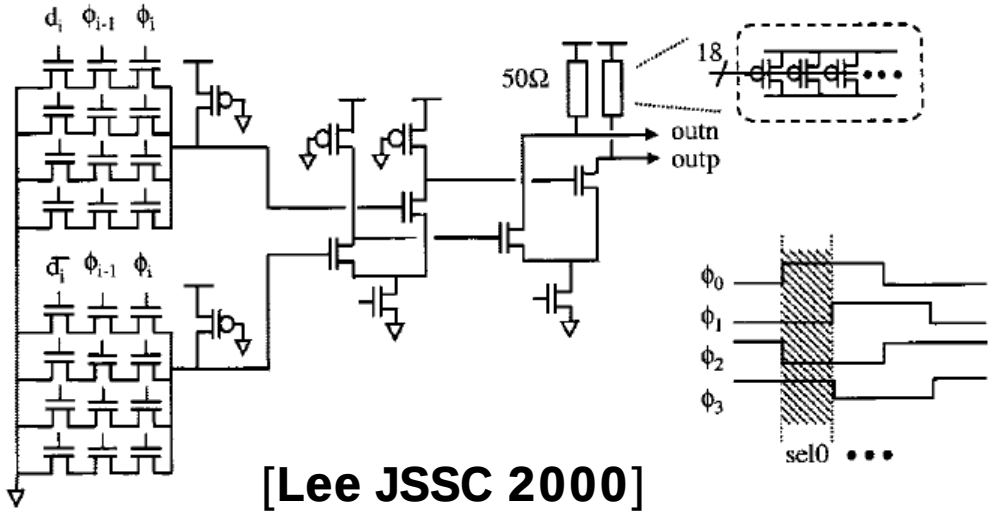
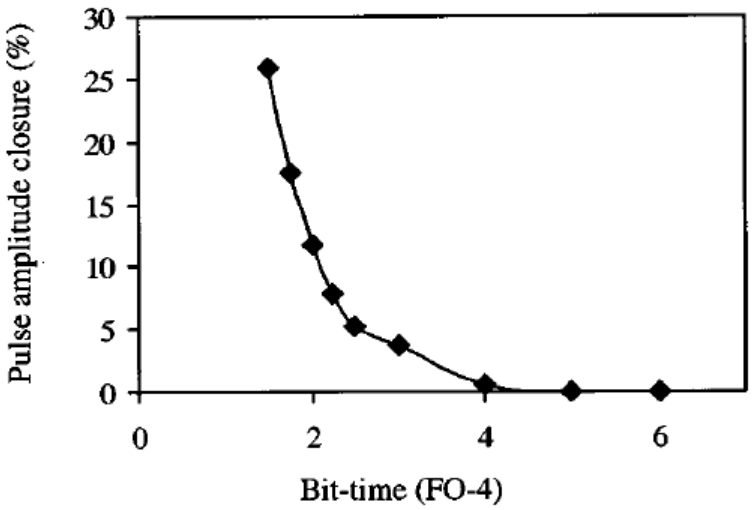
Current-Mode Input-Multiplexed

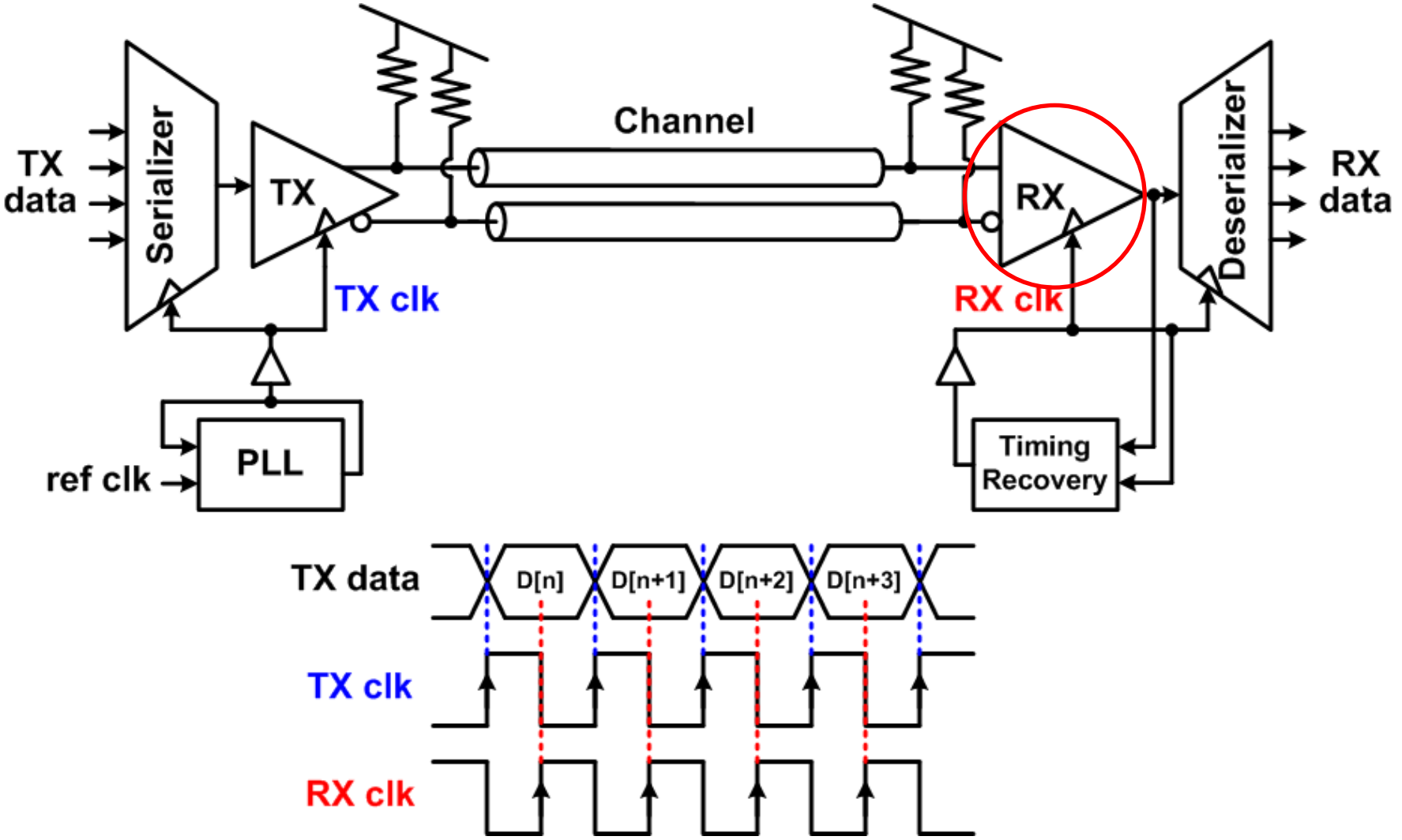


[**Lee JSSC 2000**]



- Reduces output capacitance relative to output-multiplexed driver
  - Easier to implement TX equalization
- Not sensitive to output stage current mismatches
- Reduces power due to each mux stage not having to be sized to deliver full output current

High-Speed Electrical Link System

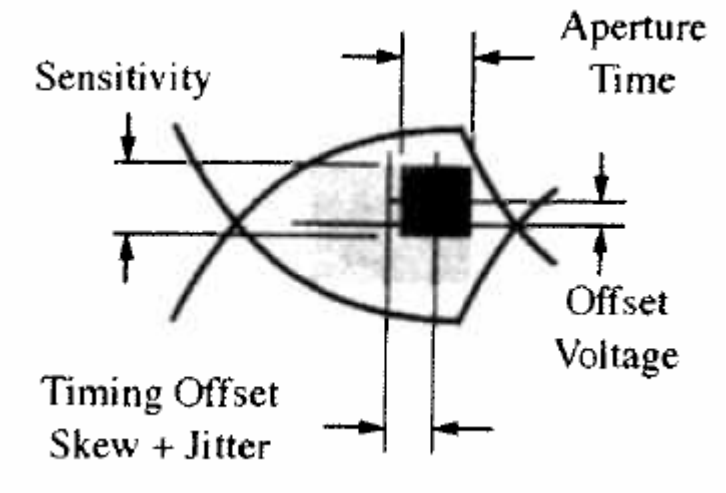


Receiver Circuits

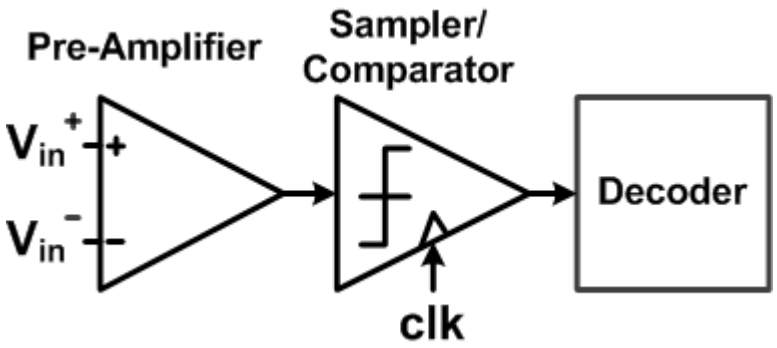
- RX parameters
- RX static amplifiers
- Clocked comparators
  - Circuits
  - Characterization techniques
- Integrating receivers
- RX sensitivity
  - Offset correction

Receiver Parameters

- RX sensitivity, offsets in voltage and time domain, and aperture time are important parameters
- Minimum eye width is determined by aperture time plus peak-to-peak timing jitter
- Minimum eye height is determined by sensitivity plus peak-to-peak voltage offset



RX Block Diagram



- RX must sample the signal with high timing precision and resolve input data to logic levels with high sensitivity
- Input pre-amp can improve signal gain and improve input referred noise
  - Can also be used for equalization, offset correction, and fix sampler common-mode
  - Must provide gain at high-bandwidth corresponding to full data rate
- Comparator can be implemented with static amplifiers or clocked regenerative amplifiers
  - Clocked regenerative amplifiers are more power efficient for high gain
- Decoder used for advanced modulation (PAM4, Duo-binary)

Next Time

- Receiver Circuits