ECEN720: High-Speed Links Circuits and Systems
Spring 2025

Lecture 11: Clocking Architectures & PLLs

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Announcements

- Lab Report 6 due Apr 3

- Project Preliminary Report due Apr 15

- Project Final Report due Apr 29

Agenda

- Clocking Architectures

- PLLs
  - Modeling
  - Noise transfer functions

References

- High-speed link clocking tutorial paper, PLL analysis paper, and PLL thesis posted on website

- Posted PLL models in project section

- Website has additional links on PLL and jitter tutorials

- Majority of today's PLL material comes from Fischette tutorial and M. Mansuri's PhD thesis (UCLA)
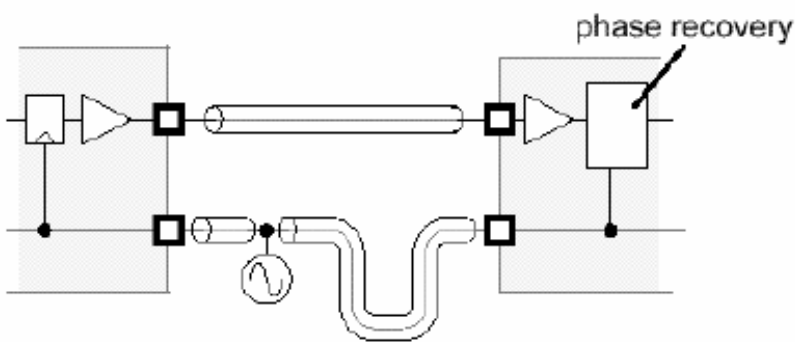
High-Speed Electrical Link System
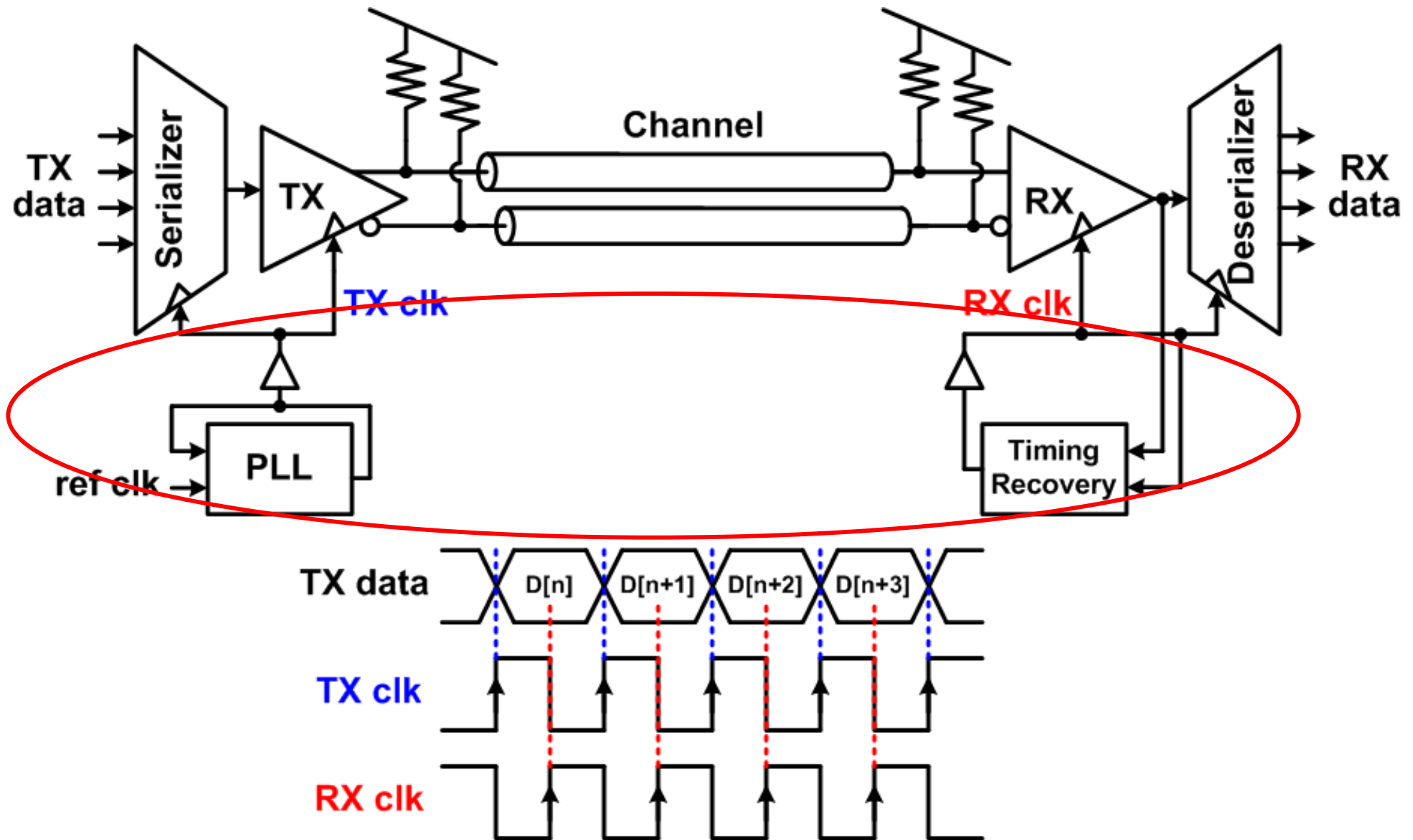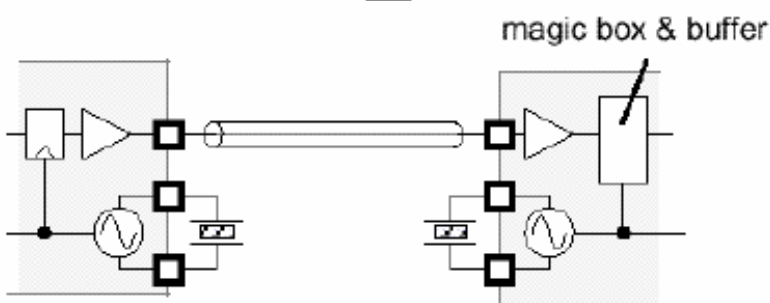
Clocking Terminology

[**Poulton**]
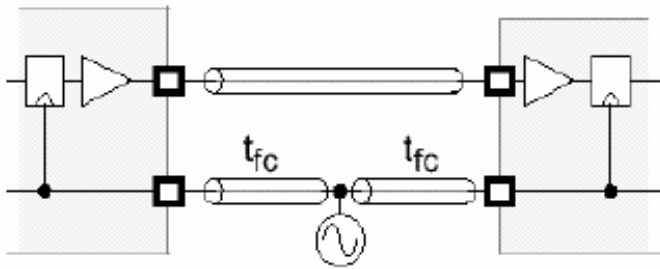
Synchronous
- Every chip gets same frequency AND phase
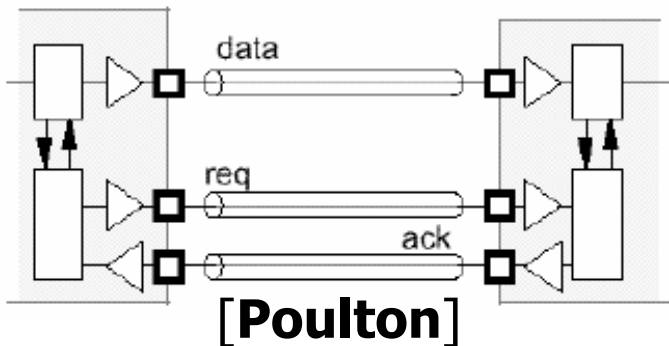- Used in low-speed busses

Mesochronous
- Same frequency, but unknown phase
- Requires phase recovery circuitry
  - Can do with or without full CDR
- Used in fast memories, internal system interfaces, MAC/Packet interfaces

Plesiochronous
- Almost the same frequency, resulting in slowly drifting phase
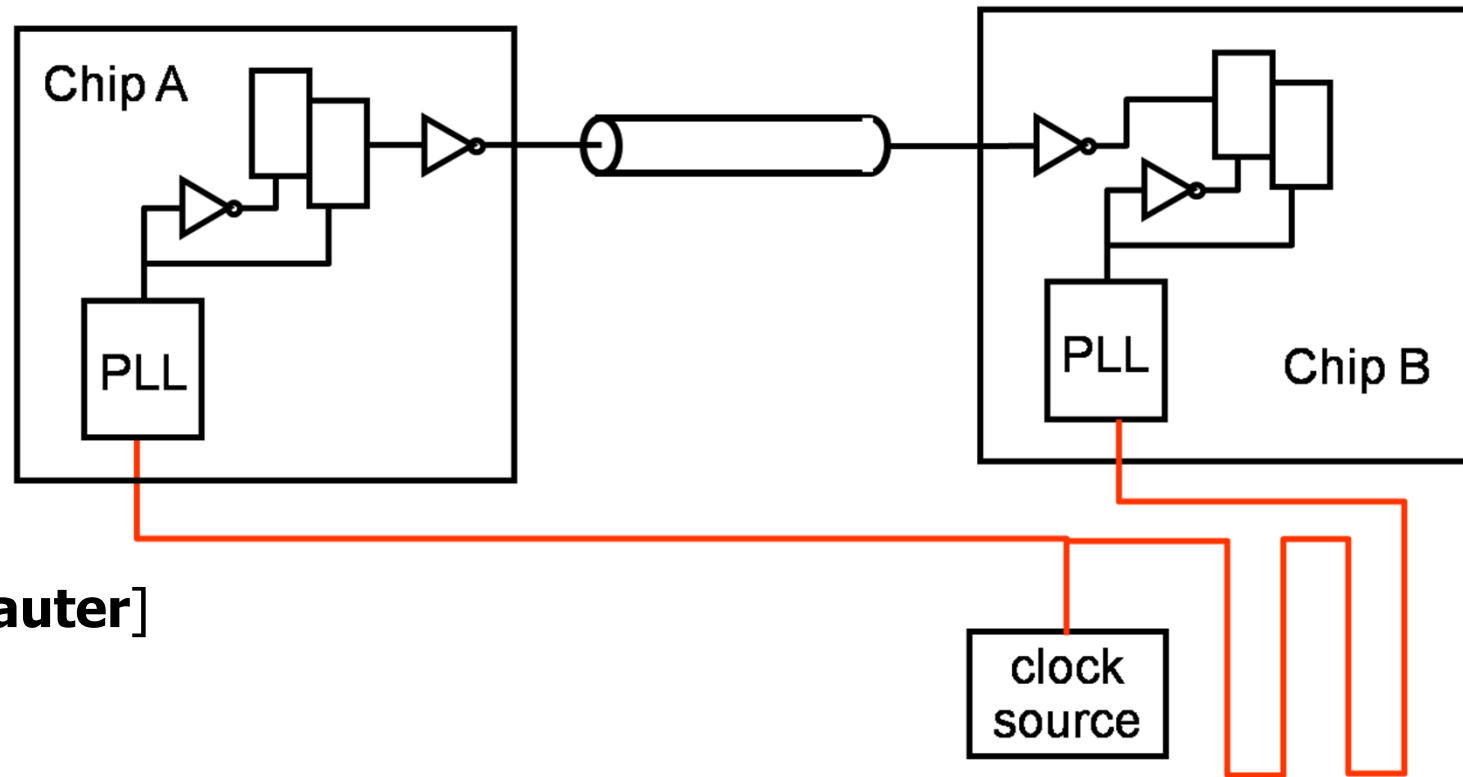- Requires CDR
- Widely used in high-speed links

Asynchronous
- No clocks at all
- Request/acknowledge handshake procedure
- Used in embeddded systems, Unix, Linux

I/O Clocking Architectures

- Three basic I/O architectures
    - Common Clock (Synchronous)
    - Forward Clock (Source Synchronous)
    - Embedded Clock (Clock Recovery)

- These I/O architectures are used for varying applications that require different levels of I/O bandwidth

- A processor may have one or all of these I/O types

- Often the same circuitry can be used to emulate different I/O schemes for design reuse

Common Clock I/O Architecture

[**Krauter**]

- Common in original computer systems
- Synchronous system by design (no active deskew)
- Common bus clock controls chip-to-chip transfers
- Requires equal length routes to chips to minimize clock skew
- Data rates typically limited to ~100Mb/s

8

Common Clock I/O Cycle Time

Cycle time to meet setup time

$$\max(T_{clk-A} + T_{Aclk} + T_{drive} + T_{tof} + T_{receive} + T_{setup}) - \min(T_{Bclk} - T_{clk-B}) < T_{cycle}$$
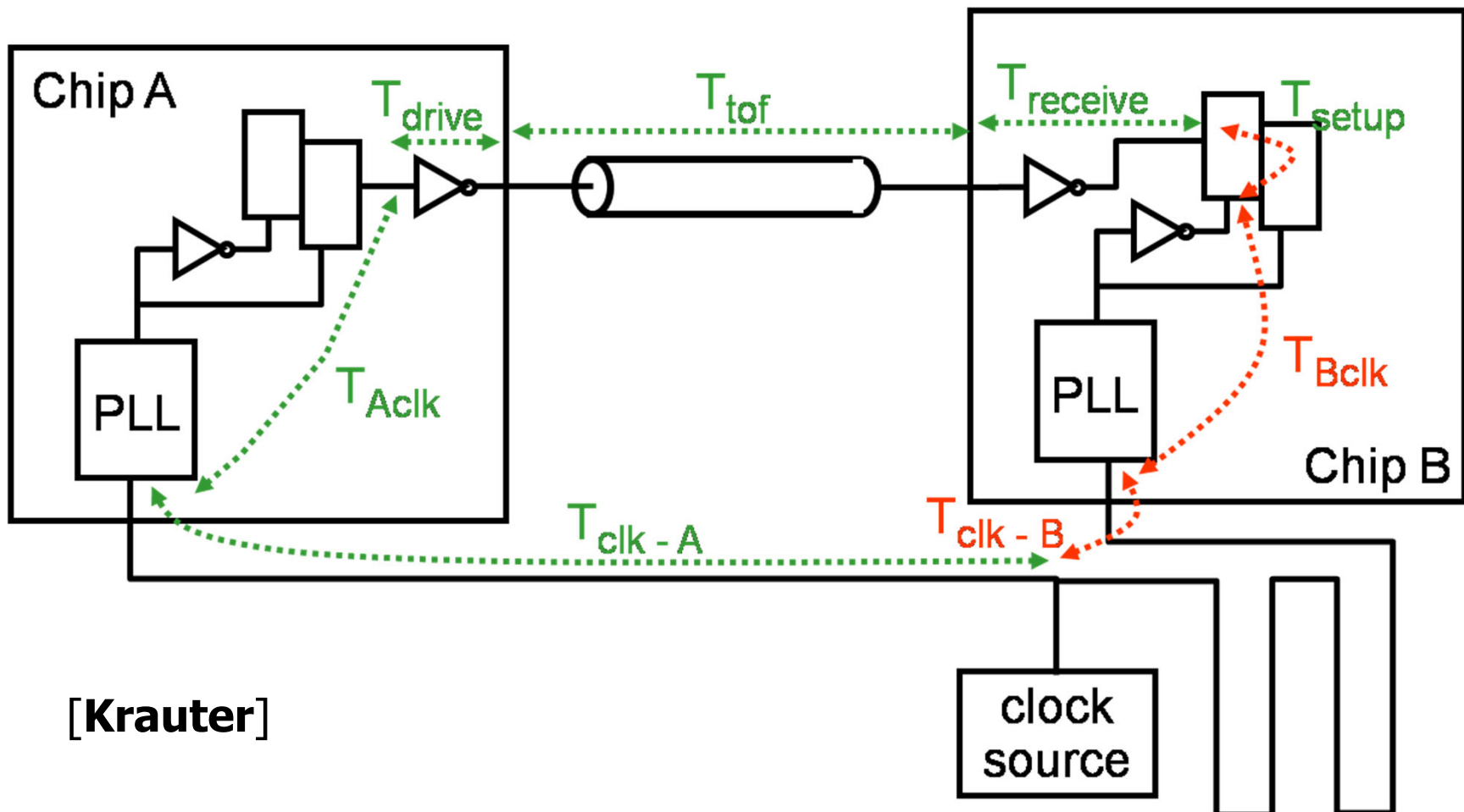
[**Krauter**]

Common Clock I/O Limitations

- Difficult to control clock skew and propagation delay

- Need to have tight control of absolute delay to meet a given cycle time

- Sensitive to delay variations in on-chip circuits and board routes

- Hard to compensate for delay variations due to low correlation between on-chip and off-chip delays

- While commonly used in on-chip communication, offers limited speed in I/O applications

Forward Clock I/O Architecture

Multi-Channel Serial Link System
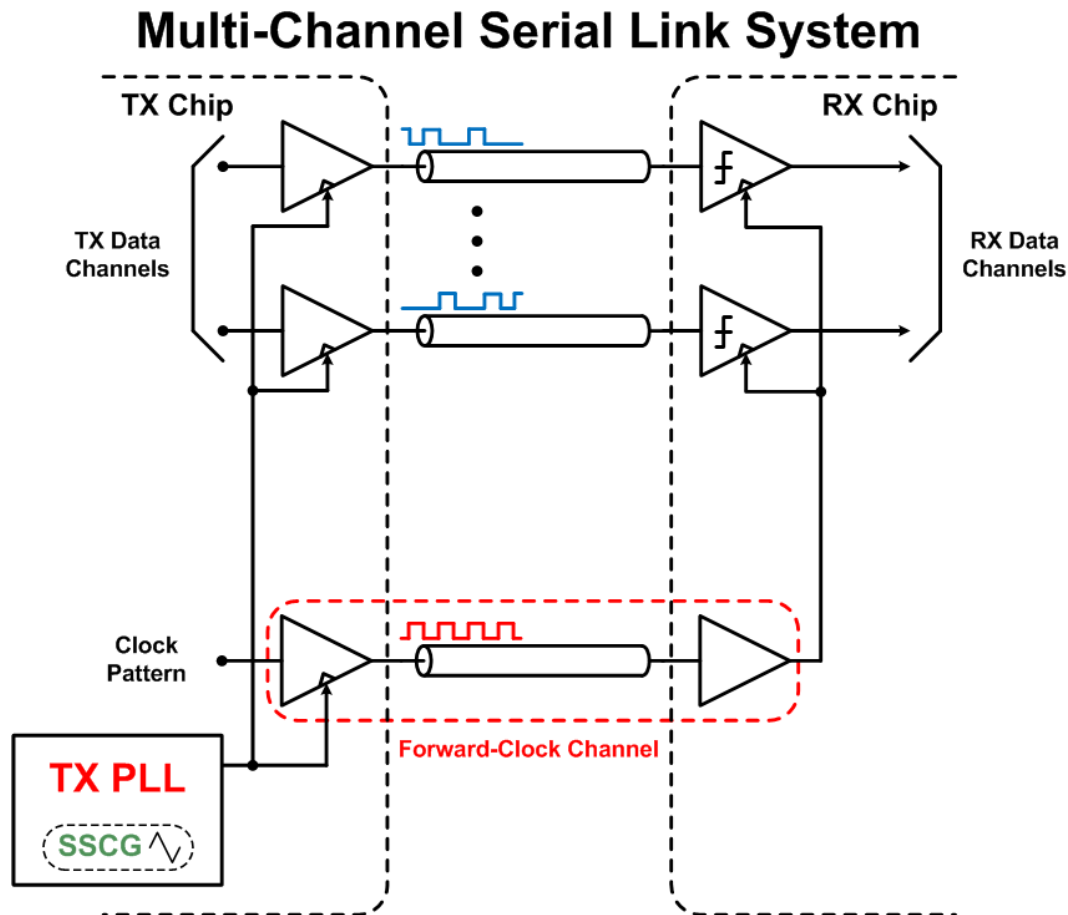
- Common high-speed reference clock is forwarded from TX chip to RX chip
  - Mesochronous system
- Used in processor-memory interfaces and multi-processor communication
  - Intel QPI
  - Hypertransport
- Requires one extra clock channel
- "Coherent" clocking allows low-to-high frequency jitter tracking
- Need good clock receive amplifier as the forwarded clock is attenuated by the channel

Forward Clock I/O Limitations

## Multi-Channel Serial Link System
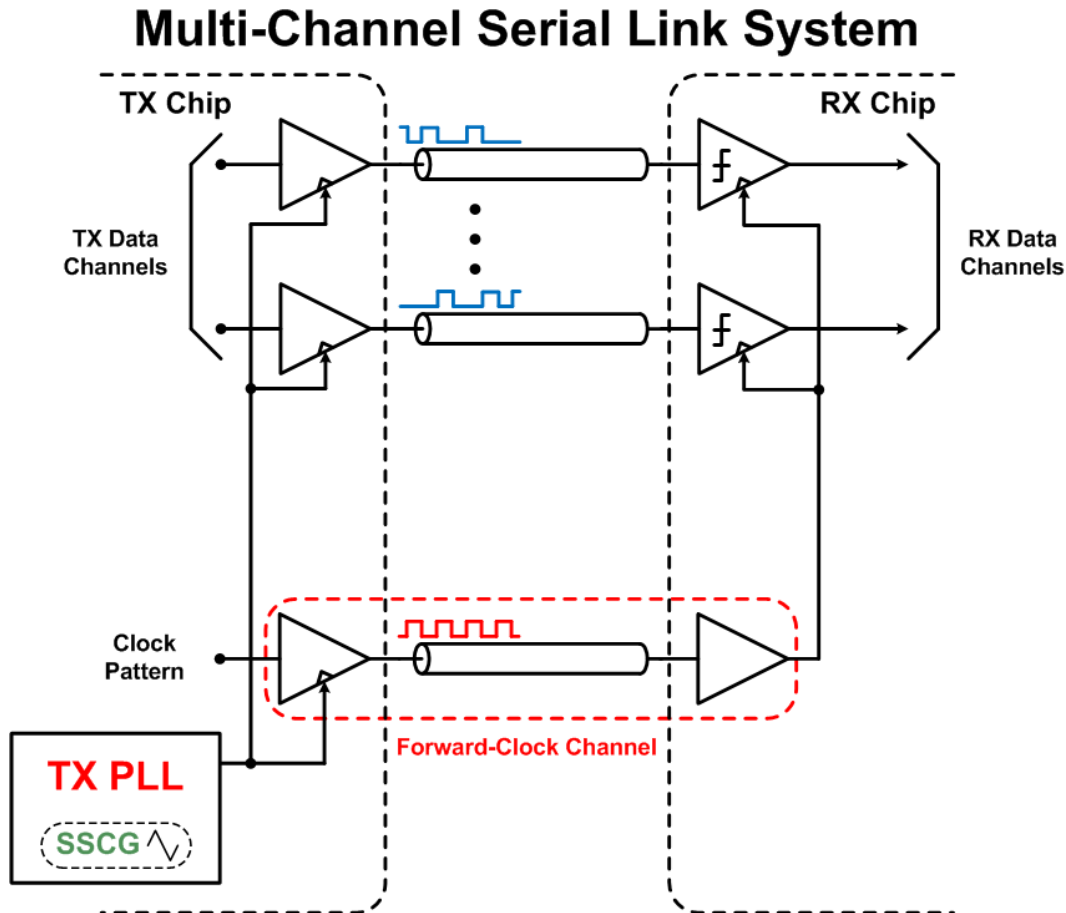
- Clock skew can limited forward clock I/O performance
  - Driver strength and loading mismatches
  - Interconnect length mismatches

- Low pass channel causes jitter amplification

- Duty-Cycle variations of forwarded clock

12

Forward Clock I/O De-Skew


Multi-Channel Serial Link System
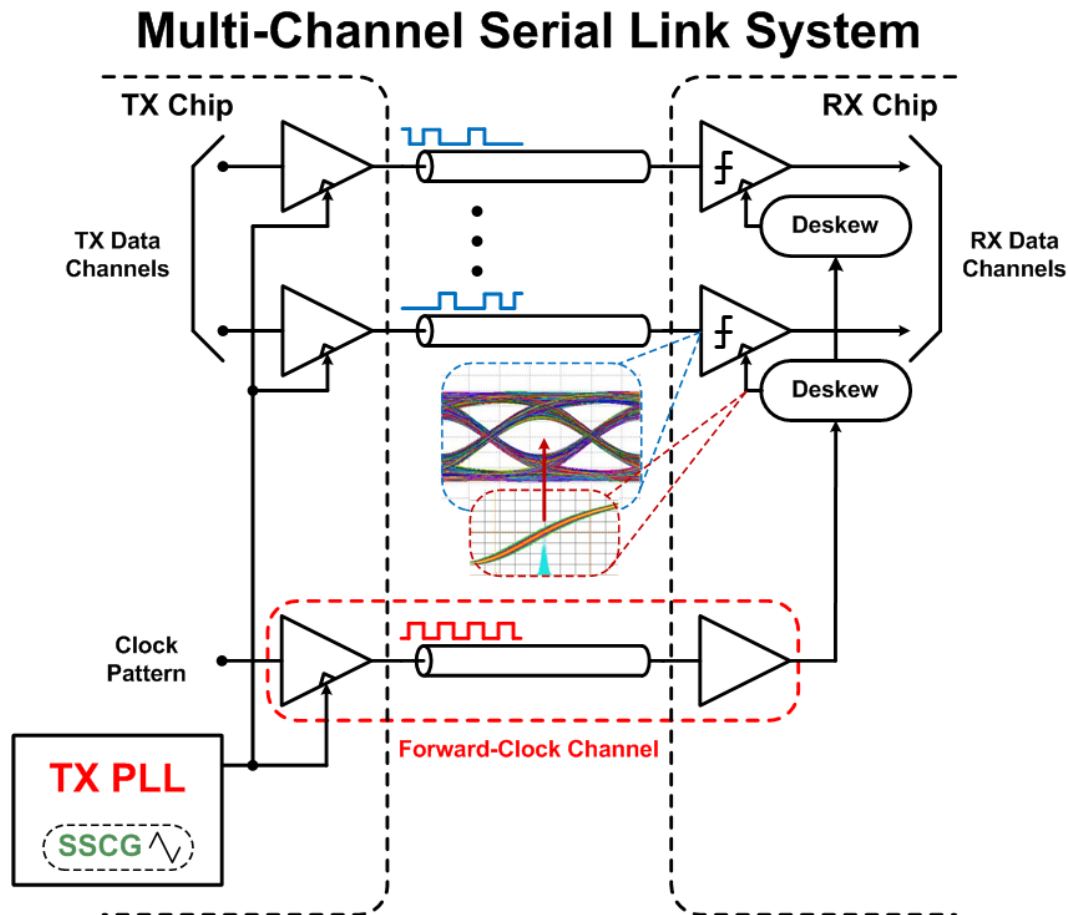
- Per-channel de-skew allows for significant data rate increases

- Sample clock adjusted to center clock on the incoming data eye

- Implementations
  - Delay-Locked Loop and Phase Interpolators
  - Injection-Locked Oscillators

- Phase Acquisition can be
  - BER based – no additional input phase samplers
  - Phase detector based implemented with additional input phase samplers periodically powered on

Forward Clock I/O Circuits
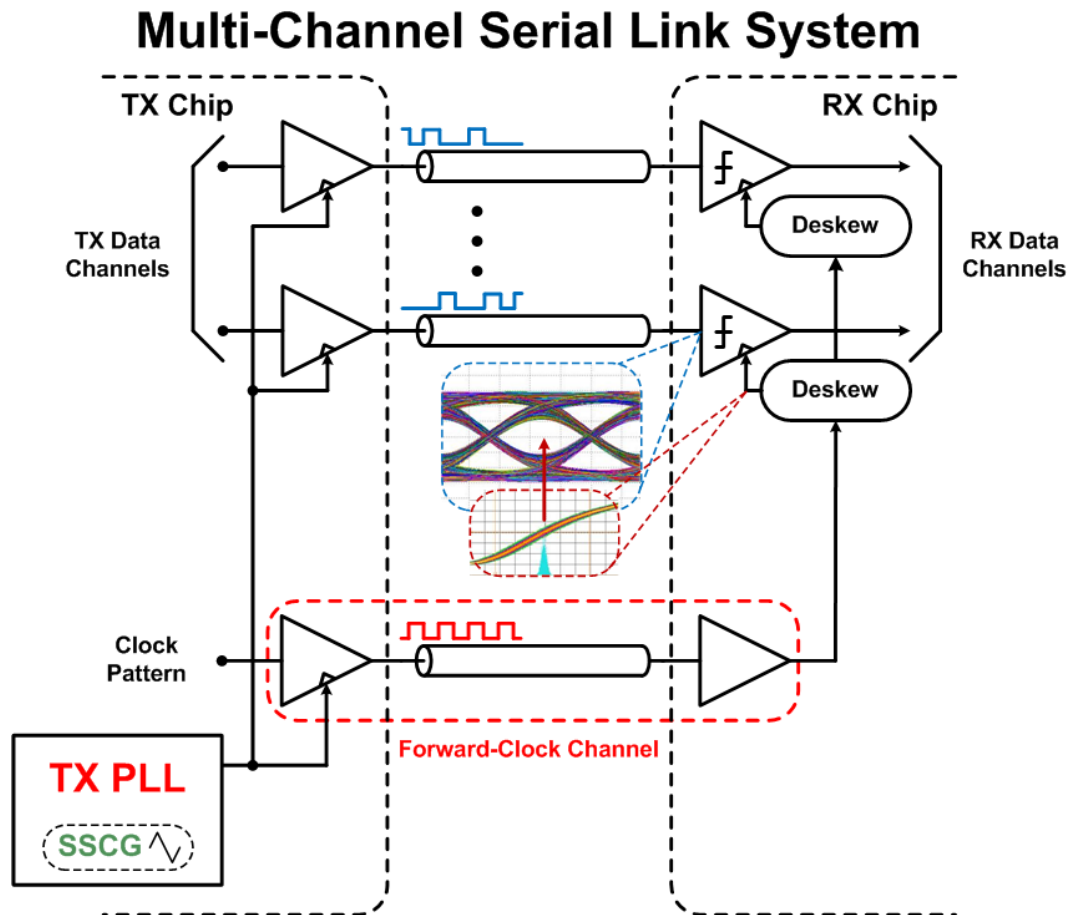

Multi-Channel Serial Link System

- TX PLL

- TX Clock Distribution

- Replica TX Clock Driver

- Channel

- Forward Clock Amplifier

- RX Clock Distribution

- De-Skew Circuit
  - DLL/PI
  - Injection-Locked Oscillator

Embedded Clock I/O Architecture

**Multi-Channel Serial Link System**
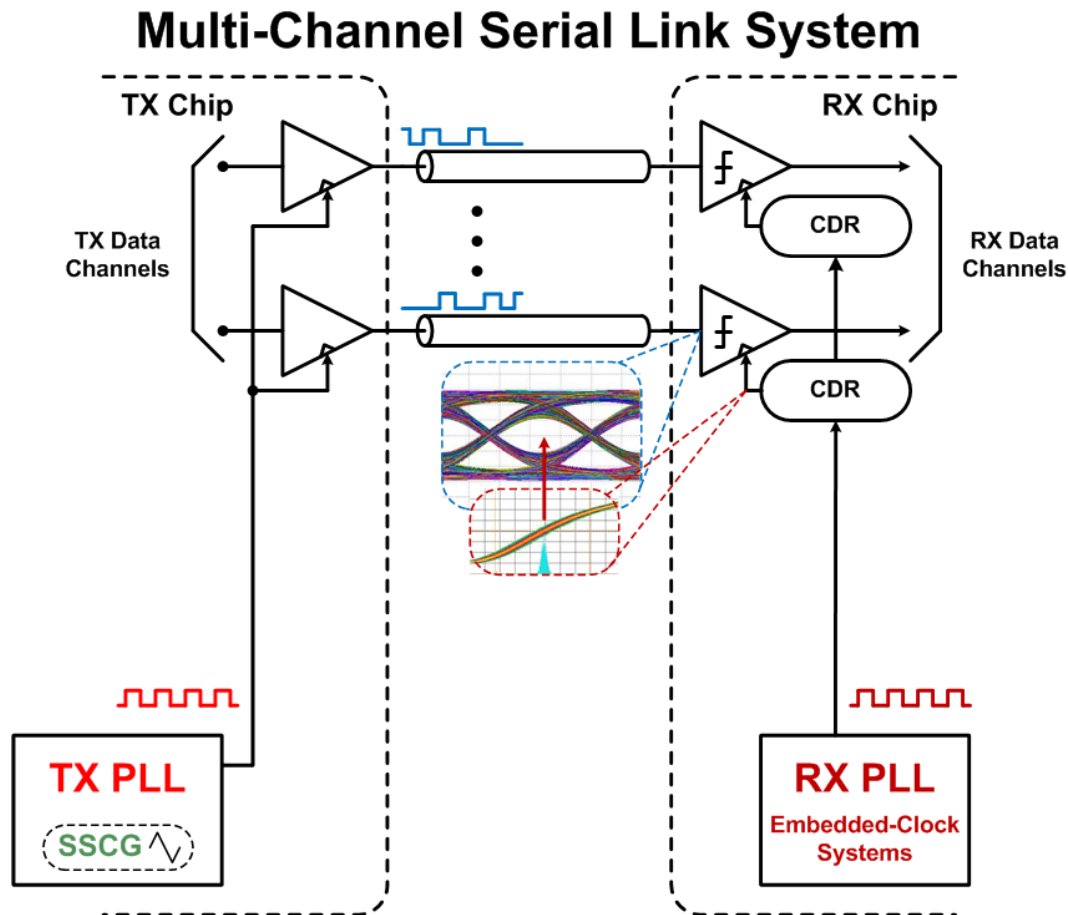
- Can be used in mesochronous or plesiochronous systems

- Clock frequency and optimum phase position are extracted from incoming data stream

- Phase detection continuously running

- CDR Implementations
  - Per-channel PLL-based
  - Dual-loop w/ Global PLL &
    - Local DLL/PI
    - Local Phase-Rotator PLLs

Embedded Clock I/O Limitations


Multi-Channel Serial Link System
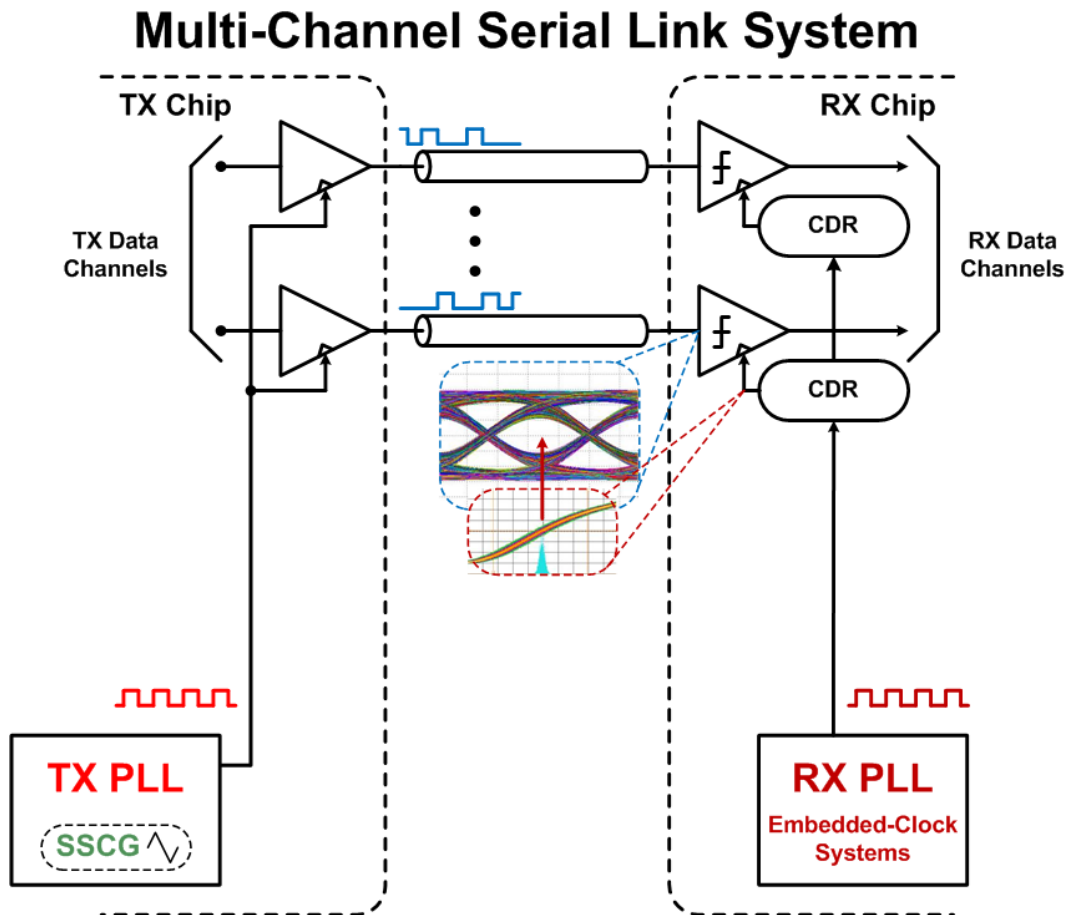
- Jitter tracking limited by CDR bandwidth
  - Technology scaling allows CDRs with higher bandwidths which can achieve higher frequency jitter tracking

- Generally more hardware than forward clock implementations
  - Extra input phase samplers

Embedded Clock I/O Circuits
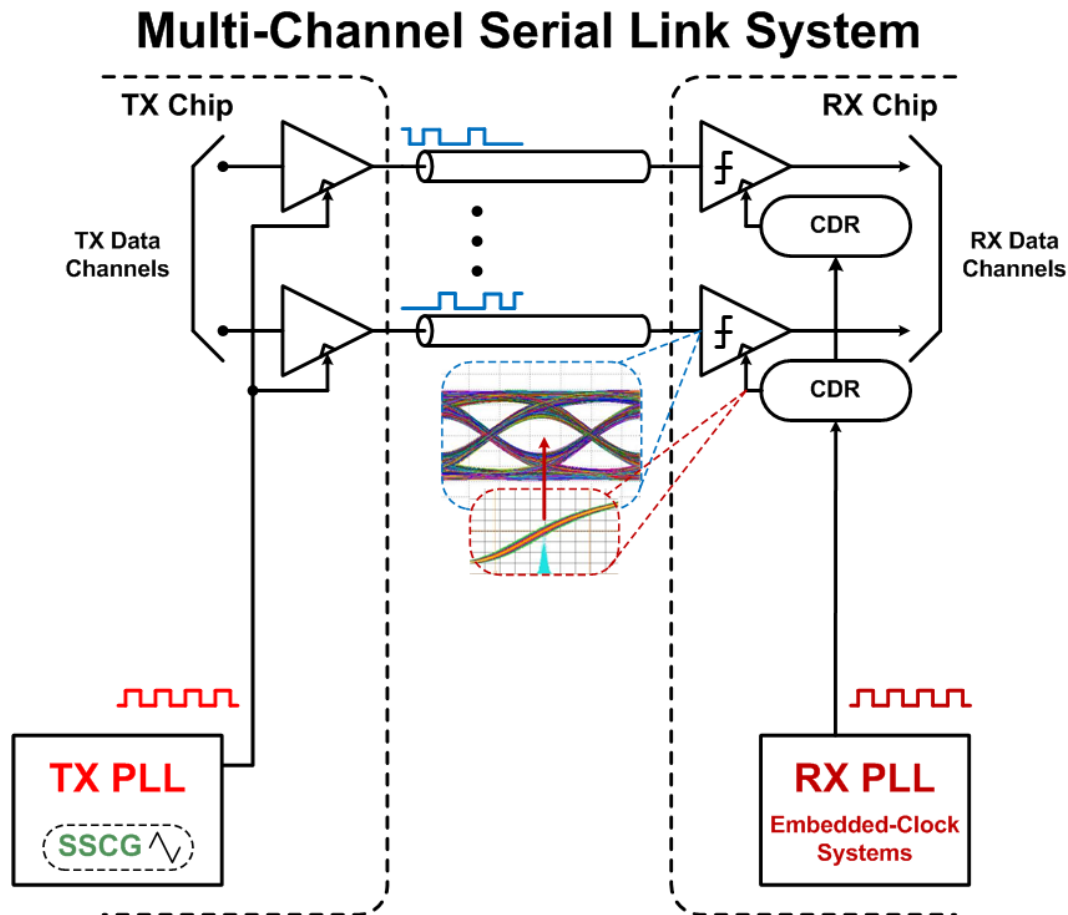
Multi-Channel Serial Link System

- TX PLL

- TX Clock Distribution

- CDR
  - Per-channel PLL-based
  - Dual-loop w/ Global PLL &
    - Local DLL/PI
    - Local Phase-Rotator PLLs
    - Global PLL requires RX clock distribution to individual channels

Xilinx 0.5-32Gb/s Transceiver Clocking

Frac-N LC PLL₁, ₂ **Channels 1-4**
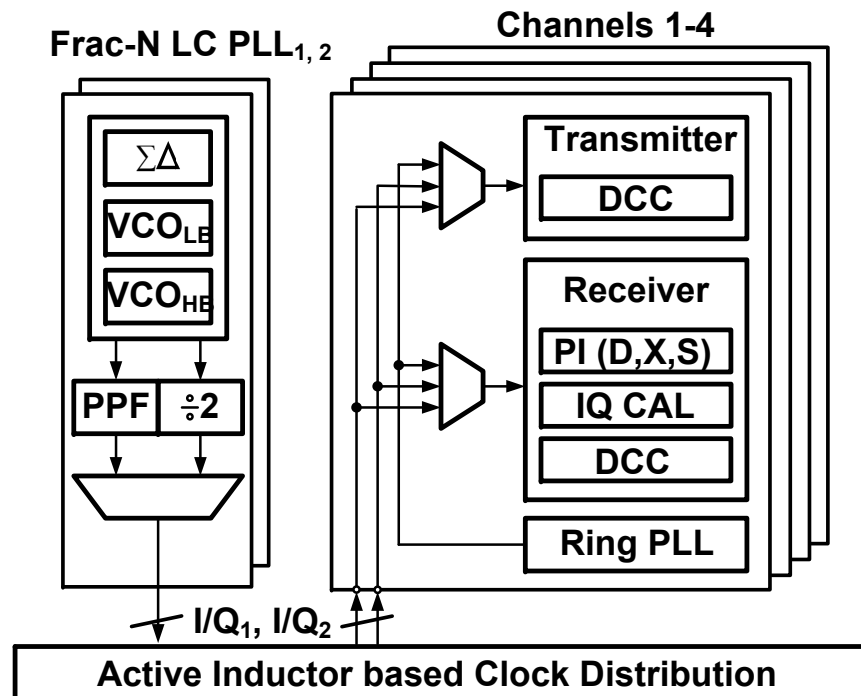
Technology	CMOS 16nm FinFET
Power Supply (V_{avcc}, V_{avtt}, V_{aux})	0.9 V, 1. 2V, 1.8 V
Frequency range	500 Mb/s – 32.75 Gb/s
Transceiver Quad area	2.625 mm × 2.218 mm
LC PLL range	8-16.375 GHz
Ring PLL range	2-6.25 GHz
TX PRBS7 jitter at 32.75Gb/s	TJ: 5.39 ps, RJ: 190 fs
32.75Gb/s RX JTOL @ 30MHz	0.45 UI
@ 100MHz	0.6 UI
Channel loss at 32.75Gb/s	30 dB
Measured BER at 32.75Gb/s	$< 10^{-15}$
Power at 32.75Gb/s with DFE	577mW/ch (17.6pJ/b)

[Upadhyaya VLSI 2016]

- LC-PLL with 2 LC-VCOs used to cover high data rates (8-32Gb/s)

- Ring-PLL used for lower data rates

- CML clock distribution with active inductive loads used for low jitter

PLLs

- PLL modeling

- PLL noise transfer functions

PLL Block Diagram

$$F_{ref}$$

$$F_{out} = N \cdot F_{ref}$$

ref(t) — **PFD** — e(t) — **Loop Filter** — v(t) — **VCO** — out(t)

div(t)

Divider

N

[**Perrott**]
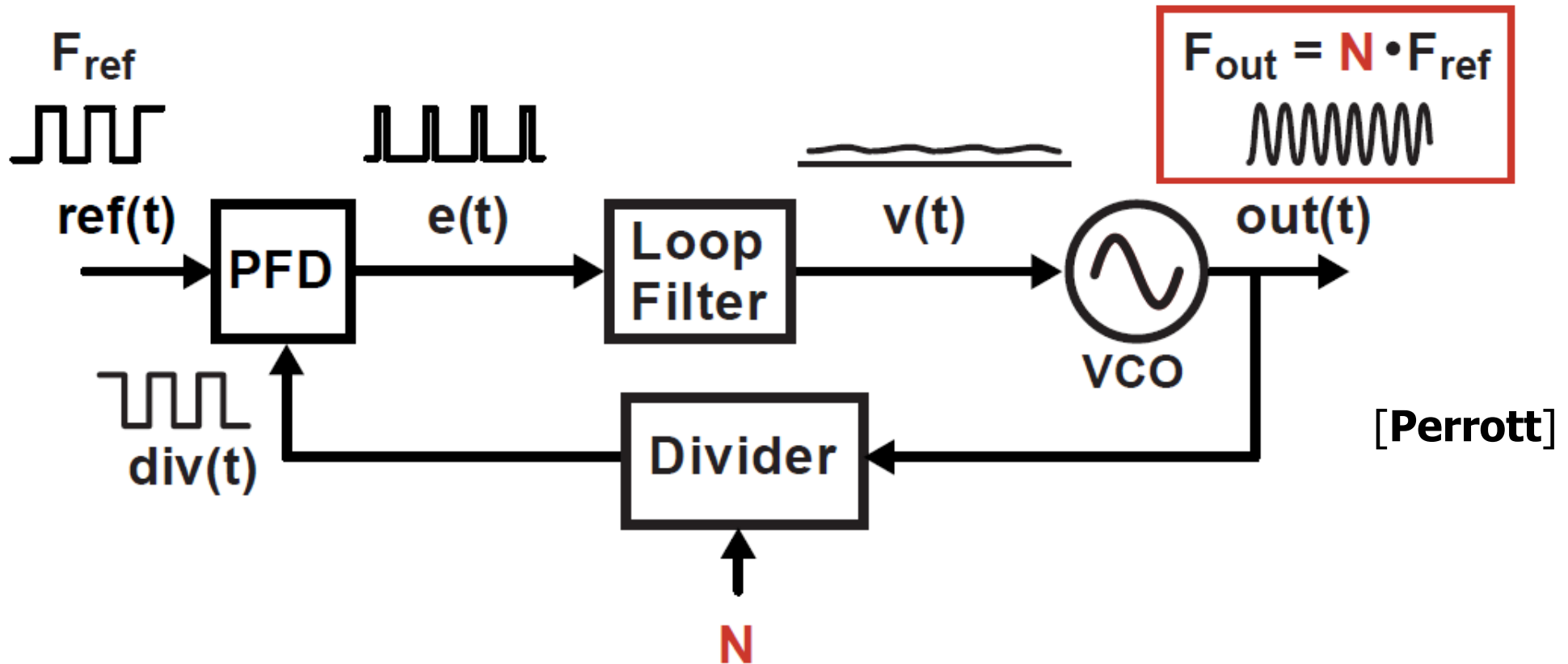
- A phase-locked loop (PLL) is a negative feedback system where an oscillator-generated signal is phase AND frequency locked to a reference signal

PLL Applications

- PLLs applications
  - Frequency synthesis
    - Multiplying a 100MHz reference clock to 10GHz
  - Skew cancellation
    - Phase aligning an internal clock to an I/O clock
  - Clock recovery
    - Extract from incoming data stream the clock frequency and optimum phase of high-speed sampling clocks
  - Modulation/De-modulation
    - Wireless systems
    - Spread-spectrum clocking

Forward Clock I/O Circuits
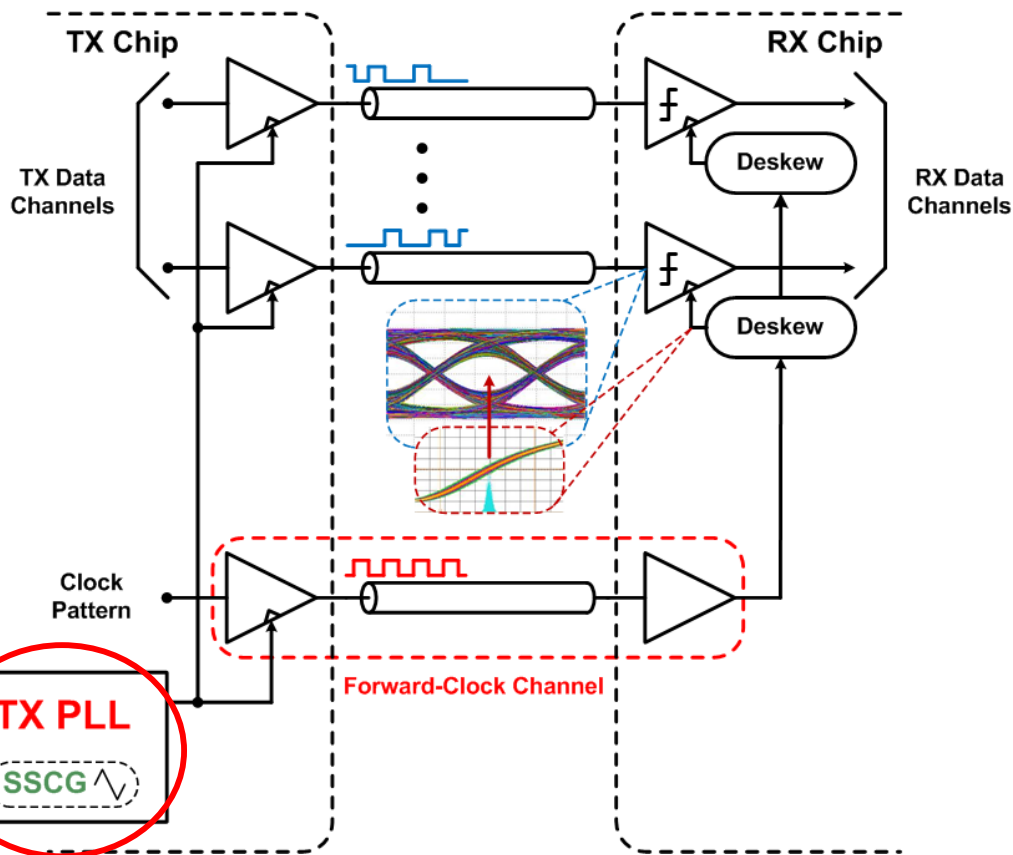
Multi-Channel Serial Link System

- TX PLL

- TX Clock Distribution

- Replica TX Clock Driver

- Channel

- Forward Clock Amplifier

- RX Clock Distribution

- De-Skew Circuit
  - DLL/PI
  - Injection-Locked Oscillator

Embedded Clock I/O Circuits

Multi-Channel Serial Link System
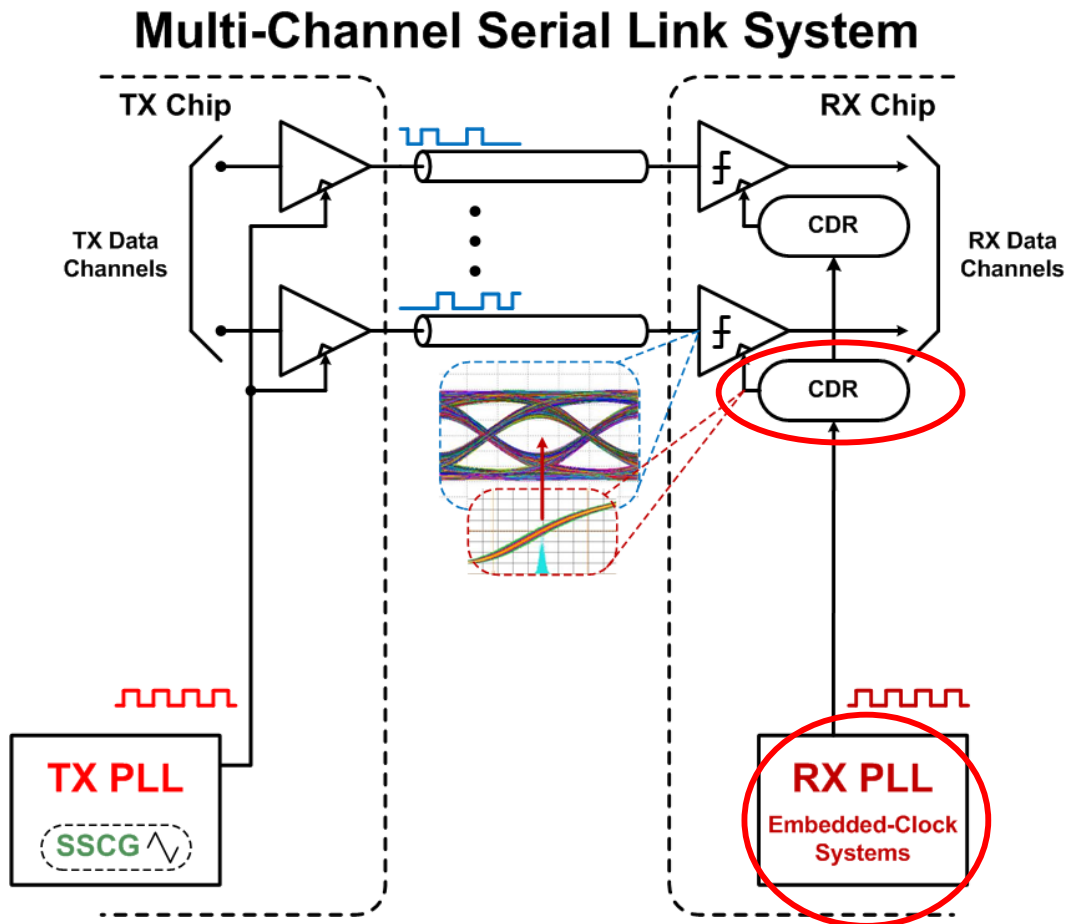
- **TX PLL**

- **TX Clock Distribution**

- **CDR**
  - Per-channel PLL-based
  - Dual-loop w/ Global PLL &
    - Local DLL/PI
    - Local Phase-Rotator PLLs
    - Global PLL requires RX clock distribution to individual channels

PLL Design Challenges

- Board-level reference clock frequencies don't scale often
  - 156MHz is a common frequency
- RX CDR bandwidth is hard to scale with PAM4 signaling and ADC-based front-ends
  - Typically 2-4MHz
- PLL bandwidth must be kept less than 10MHz for stability and to filter reference jitter
- VCO phase noise at low-frequency offsets due to flicker noise must be suppressed

32.75Gbps Transceiver PLL Simulated Jitter Numbers

Receiver Type	PLL PN @1MHz	CDR BW	RJ	RJ in UI
Analog based RX	-92.4dBc/Hz	12.7MHz	160.7fs	5.26mUI
ADC based RX	-92.4dBc/Hz	2MHz	407fs	13.3mUI

[Turker ISSCC 2019]
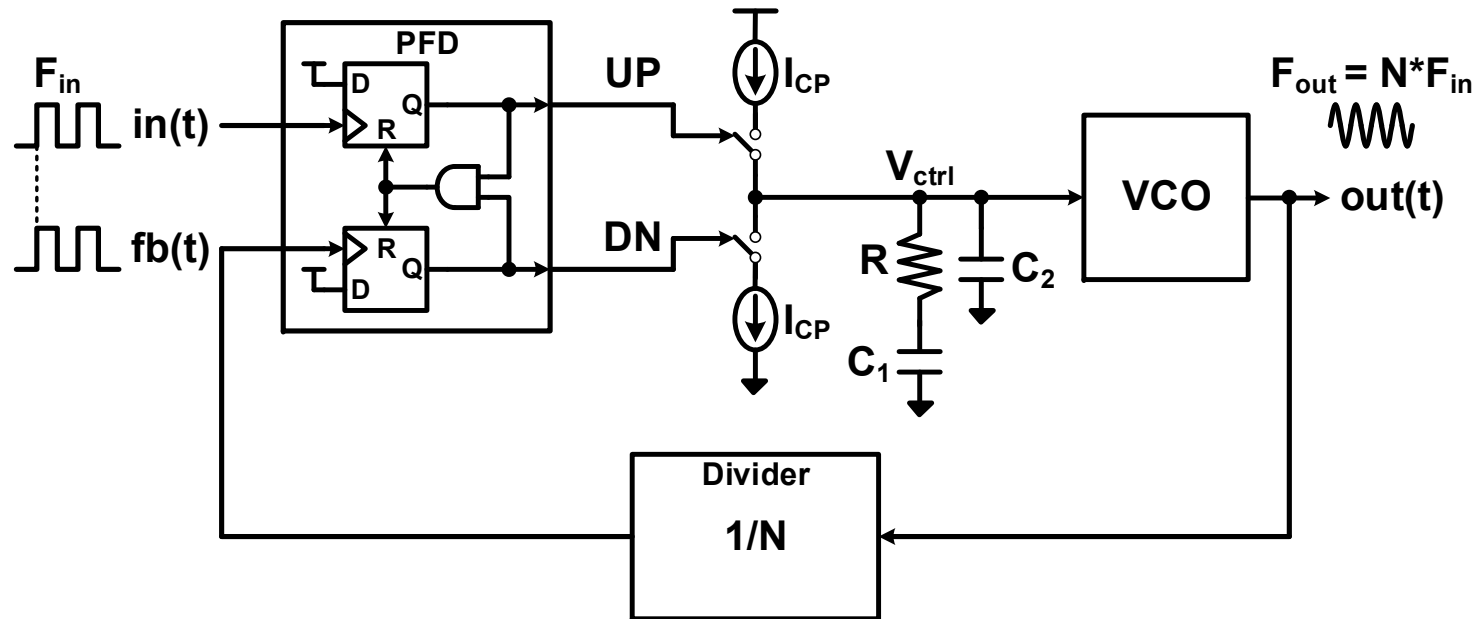
Charge Pump PLL

- Charge pump PLL is a common implementation
- Type-2 (2 integrators) allows for ideally zero phase error between the input and feedback phase
- Requires a stabilizing zero that is realized with the filter resistor
- A secondary capacitor C_2 is often added for additional filtering to reduce reference spurs
- Modeled as a third-order system

Linear PLL Model

Phase Detector

Loop Filter

VCO

ϕ_{in} $+$ Σ $-$ ϕ_e | K_{PD} | $F(s)$ | V_{ctrl} | $\dfrac{K_{VCO}}{s}$ | ϕ_{out}

ϕ_{fb}

$\dfrac{1}{N}$

Divider
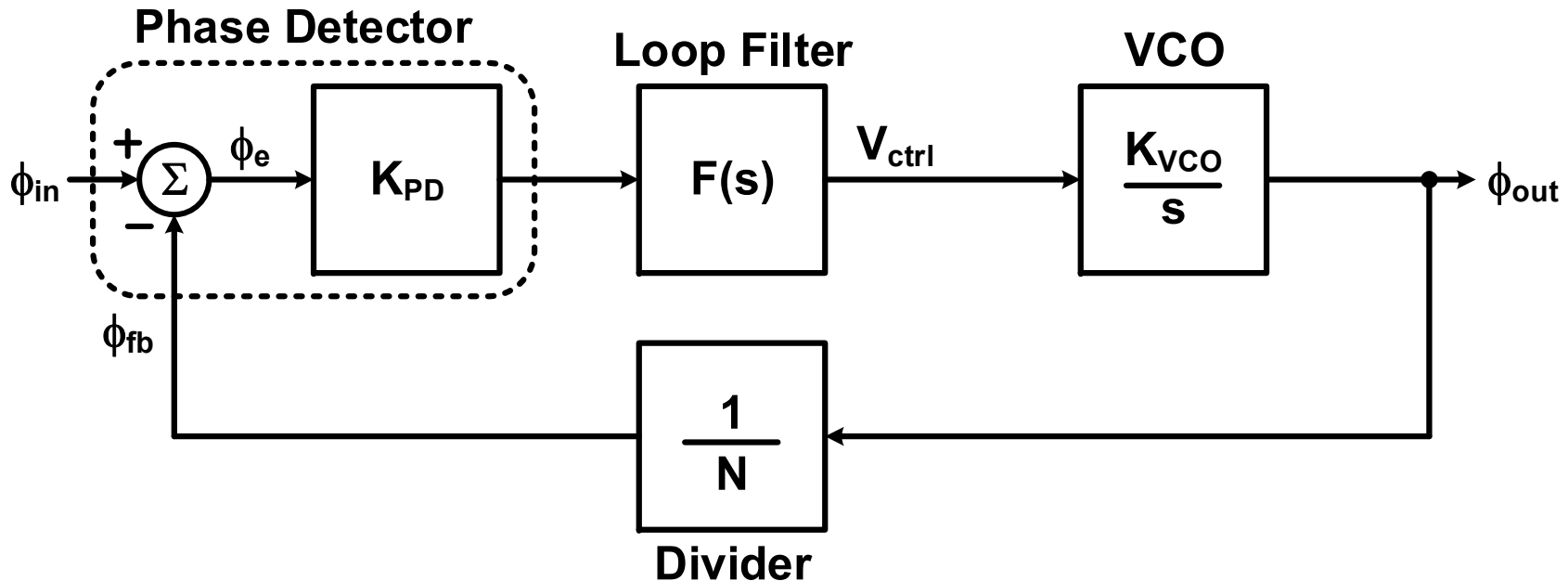
- Phase is the key variable of interest
  - Output phase response to a stimulus injected at a given point in the loop
  - Phase error response is also informative
- Linear "small-signal" analysis is useful for understand PLL dynamics if
  - PLL is locked (or near lock)
  - Input phase deviation amplitude is small enough to maintain operation in lock range

Understanding PLL Frequency Response

Input phase response

$$\frac{\phi_{out}}{\phi_{in}}$$

f

VCO output phase response

$$\frac{\phi_{out}}{\phi_{vco}}$$

f
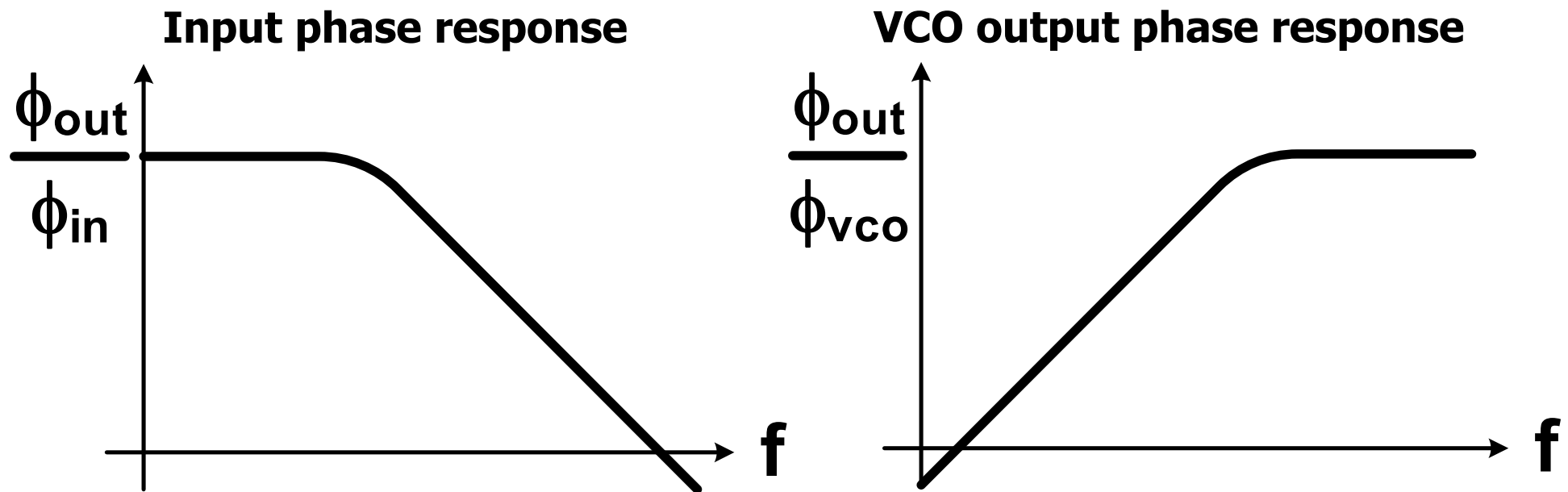
- Frequency domain analysis can tell us how well the PLL tracks the input phase as it changes at a certain frequency

- PLL transfer function is different depending on which point in the loop the output is responding to

Linear PLL Model
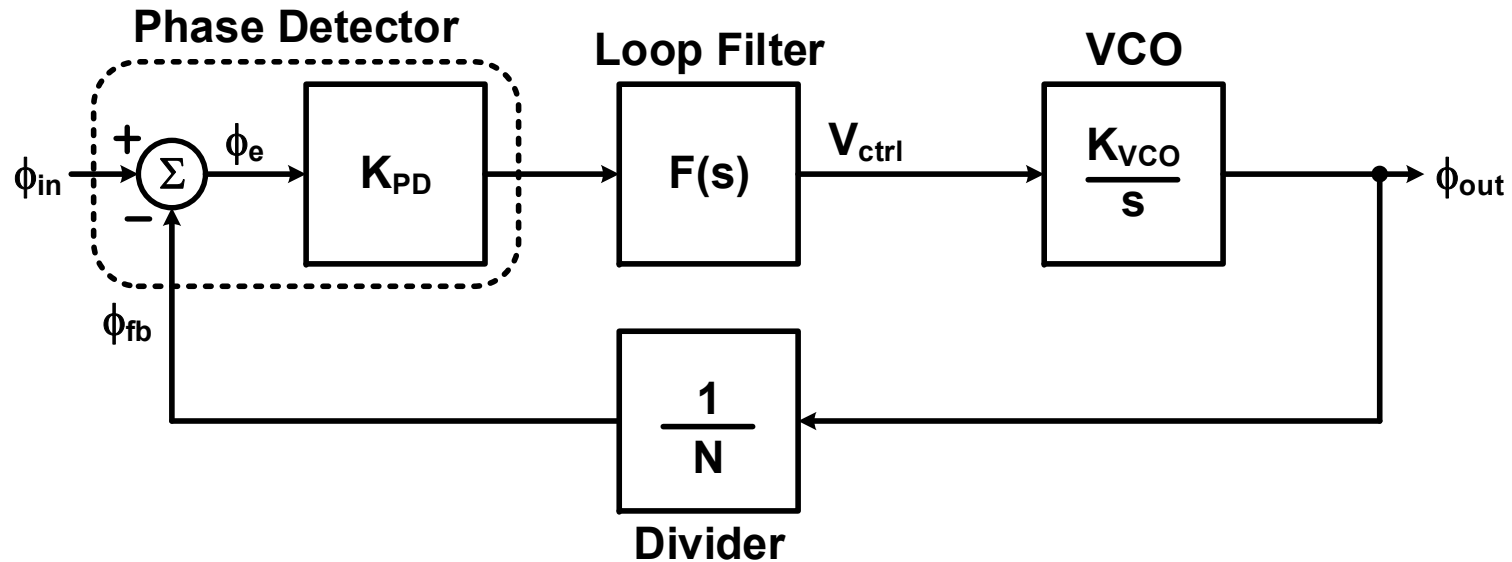
For Charge Pump PLL:

$$K_{PD} = \frac{I_{CP}}{2\pi}$$

$$F(s) = \frac{\left(\frac{1}{C_2}\right)\left(s + \frac{1}{RC_1}\right)}{s\left(s + \frac{C_1 + C_2}{RC_1 C_2}\right)}$$

$$H(s) = \frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{\frac{K_{PD}K_{VCO}}{C_2}\left(s + \frac{1}{RC_1}\right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1 C_2}\right)s^2 + \left(\frac{K_{PD}K_{VCO}}{NC_2}\right)s + \frac{K_{PD}K_{VCO}}{NRC_1 C_2}}$$

14GHz PLL Closed-Loop Transfer Function

Parameter	
Fref	156.25MHz
N	90
Fvco	14GHz
f_u	2MHz
Φ_m	60°
f_{3dB}	3.1MHz
Kvco	2π*1GHz/V
R	4kΩ
C_1	74pF
C_2	5.8pF
I_{cp}	310uA
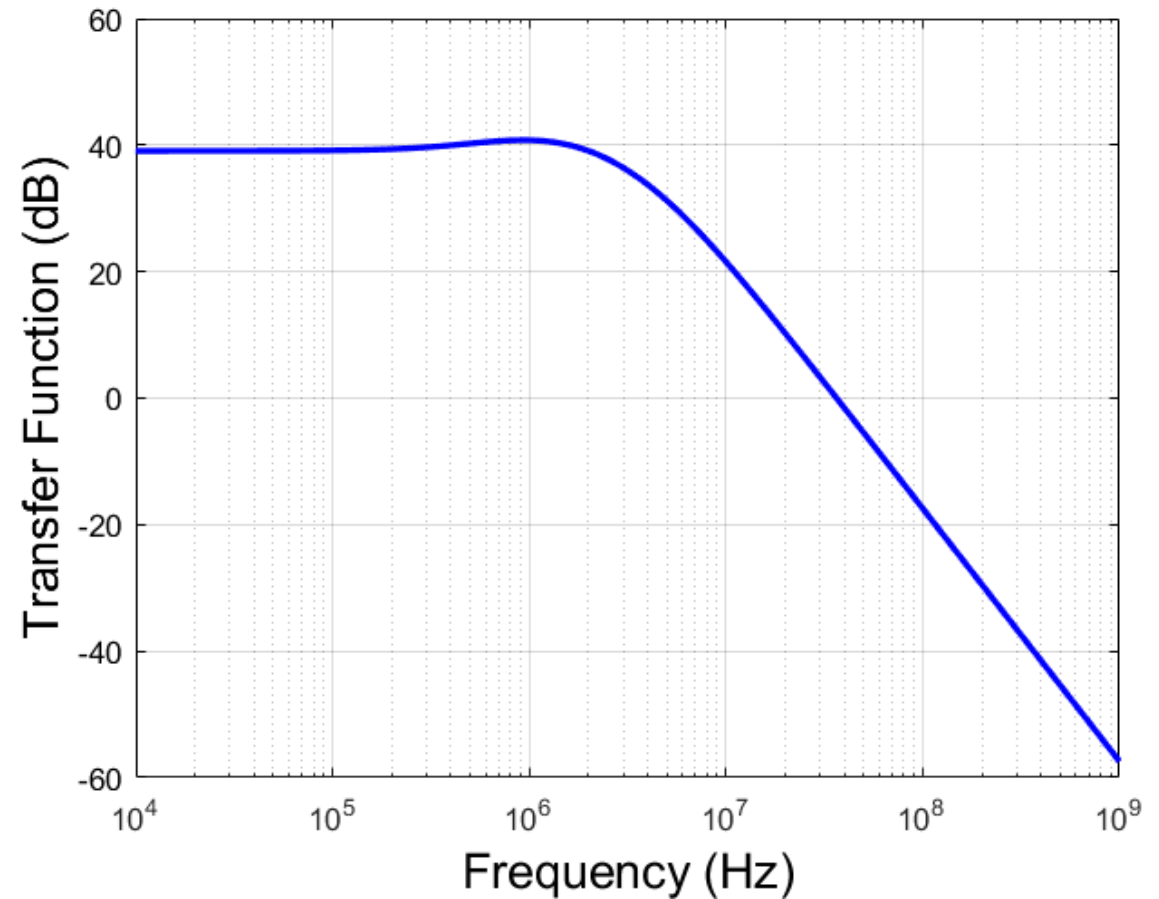
$$H(s) = \frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{\frac{K_{PD}K_{VCO}}{C_2}\left(s + \frac{1}{RC_1}\right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1C_2}\right)s^2 + \left(\frac{K_{PD}K_{VCO}}{NC_2}\right)s + \frac{K_{PD}K_{VCO}}{NRC_1C_2}}$$

Common PLL Noise Sources
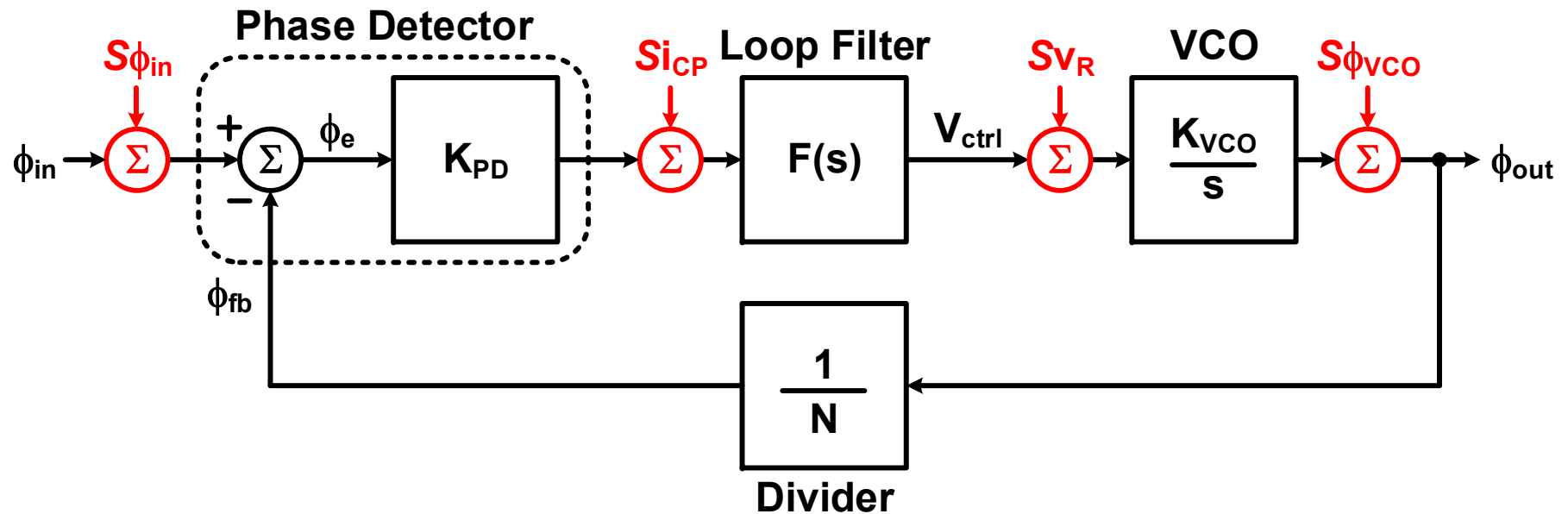
$$S_{\phi_{out}}^{\phi_{in}} = S_{\phi_{in}} |NTF_{IN}(s)|^2$$

$$S_{\phi_{out}}^{i_{CP}} = S_{i_{CP}} |NTF_{CP}(s)|^2$$

$$S_{\phi_{out}}^{v_R} = S_{v_R} |NTF_R(s)|^2$$

$$S_{\phi_{out}}^{\phi_{VCO}} = S_{\phi_{VCO}} |NTF_{VCO}(s)|^2$$

$$S_{\phi_{out}}^{Total} = S_{\phi_{out}}^{\phi_{in}} + S_{\phi_{out}}^{i_{CP}} + S_{\phi_{out}}^{v_R} + S_{\phi_{out}}^{\phi_{VCO}}$$

30

Noise Transfer Functions

$$NTF_{IN}(s) = \frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{(N)LG(s)}{1 + LG(s)}$$

$$NTF_{CP}(s) = \frac{\phi_{out}(s)}{i_{CP}(s)} = \frac{\left(\frac{N}{K_{PD}}\right)LG(s)}{1 + LG(s)}$$

$$NTF_R(s) = \frac{\phi_{out}(s)}{v_R(s)} = \frac{\frac{K_{VCO}}{s}}{1 + LG(s)}$$

$$NTF_{VCO}(s) = \frac{\phi_{out}(s)}{\phi_{VCO}(s)} = \frac{1}{1 + LG(s)}$$
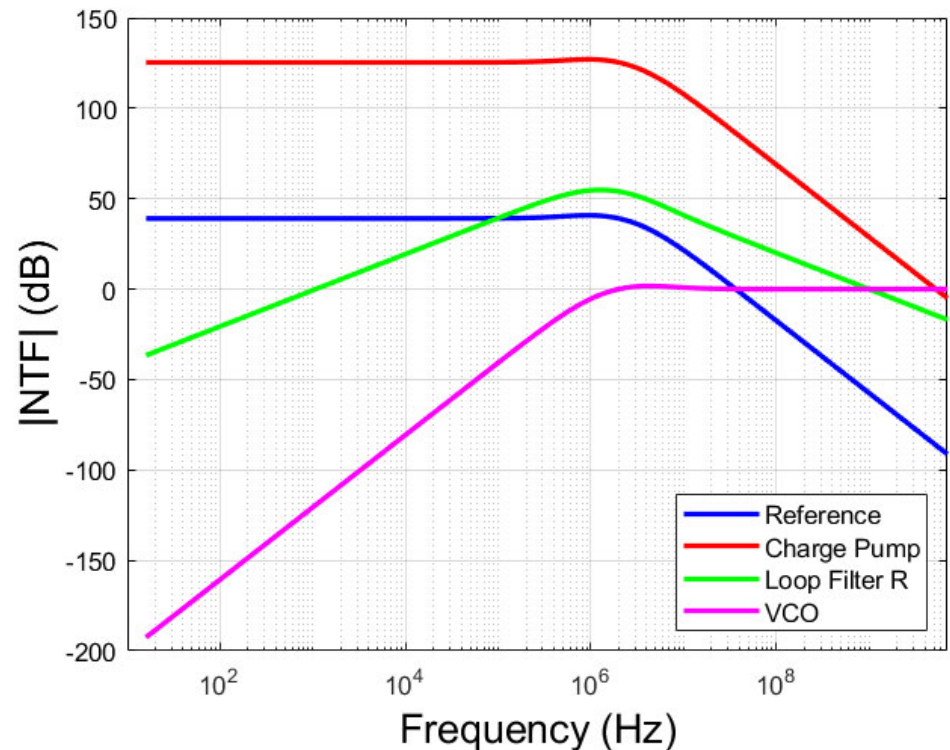
- Input reference and charge pump noise is low-pass filtered
- Loop filter noise (VCO input noise) is band-pass filtered
- VCO output phase noise is high-pass filtered

PLL Phase Noise & Jitter
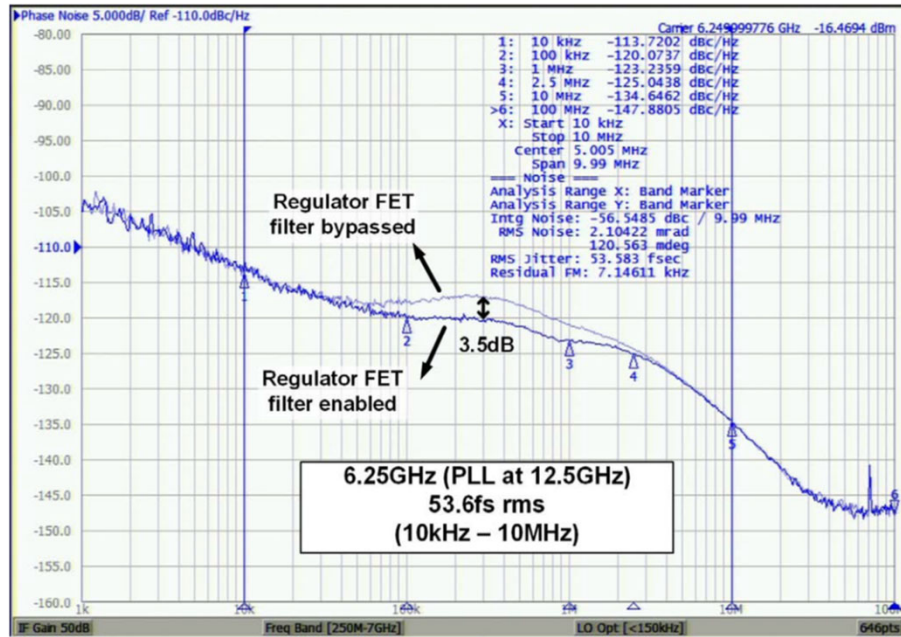
	[3]	[4]	[5]	[6]	This Work
PLL Architecture	Integer N, SSPD based	FracN, SSPD DPLL	FracN, DPLL	Integer N, SPD based	Integer N, CP based
VCO	LC	LC	LC	LC	LC
Technology	180nm	28nm	14nm FinFET	16nm FinFET	16nm FinFET
Reference Freq.(MHz)	55.25	40	26	450	500
Frequency Range (GHz)	2.21	2.7 – 4.3	5.38	9 - 18	7.4 – 14
Measurement Frequency (GHz)	2.21	5.82	2.69	18	6.25
Phase Noise @100kHz (dBc/Hz)	-125 (@200kHz)	-105.5	-113.6	-104.1 (@200kHz)	-120
Phase Noise @1MHz (dBc/Hz)	-125 (from figure)	-115.4	-122.45	-107.3	-123.2
Phase Noise @100kHz (normalized to 1GHz)	- 131.9 (@200kHz)	-120.8	-122.2	- 129.2 (@200kHz)	-135.9
Phase Noise @1MHz (normalized to 1GHz)	- 131.9	-130.7	- 131	- 132.4	-139.1
RMS Jitter (fs)	160 (10k – 100M)	159 (10k – 40M)	137 (10k – 10M)	164 (1k – 100M)	53.6 (10k – 10M)
Reference Spur (dBc)	-56	-78	-87.6	N.A	-75.5 *
Power (mW)	2.5	8.2	13.4	29.2	45
Area (mm²)	0.2	0.3	0.257	0.39	0.35
FOM$_T$ (dB)	N.A	-243.4	N.A	-239.3	-246.8

* including DAC, measured at 1.052GHz DAC output

$$FOM_T = 10\log\left(\left(\frac{\sigma_{rms}}{1s}\right)^2 \times \frac{P}{1mW} \times \frac{1}{TR}\right) \text{ where } TR = \left(\frac{f_{max} - f_{min}}{f_{mid}}\right)$$

- PLL time-domain jitter is obtained by integrating the output phase noise

$$\sigma_{j,Total}^2 = \frac{2}{\omega_0^2} \int_{f_{start}}^{f_{stop}} S_{\phi_{out}}^{Total}(f)\,df$$

- We can model an individual noise source's contribution

$$\sigma_{j,i}^2 = \frac{2}{\omega_0^2} \int_{f_{start}}^{f_{stop}} S_i(f)|NTF_i(f)|^2\,df$$

$$\sigma_{j,Total}^2 = \sum_i \sigma_{j,i}^2$$

$$\text{RMS Jitter } \sigma_j = \sqrt{\sigma_{j,Total}^2}$$

Wireline Transceiver Jitter Modeling
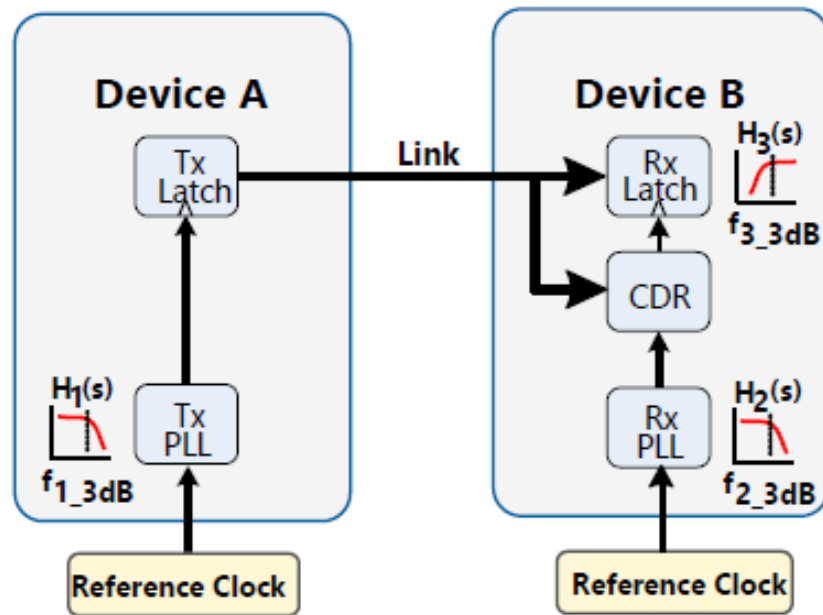
[Richmond SiLabs]
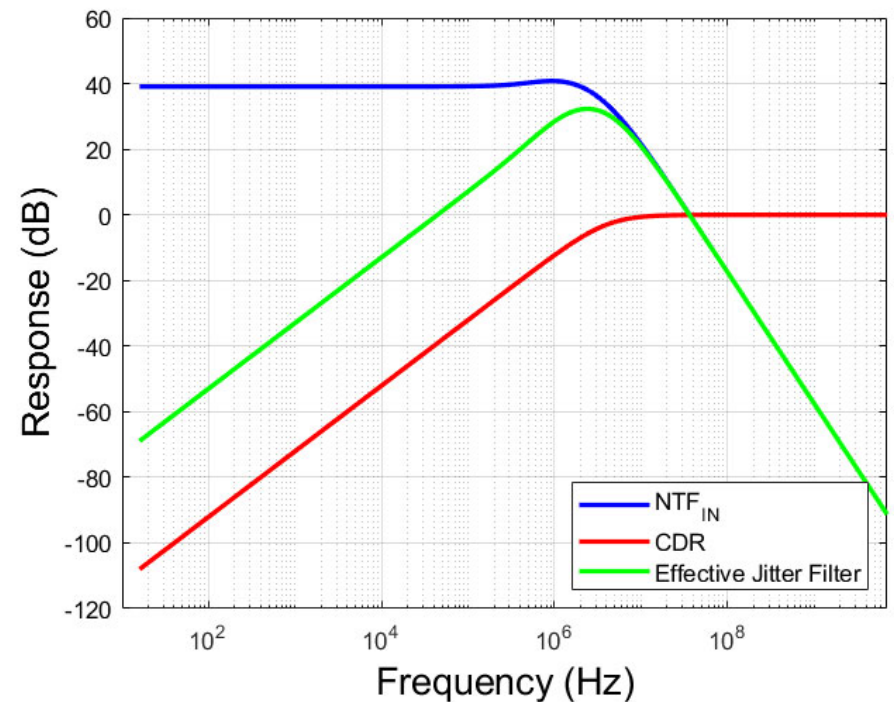
- Relative jitter (dynamic phase error) between the RX CDR-generated sampling clock and input data sets the system timing margin
- This CDR high-pass response provides additional filtering
- Modeled as a 4MHz 1st-order response (IEEE 802.3 & OIF-CEI)

$$\sigma^2_{jSYS,i} = \frac{2}{\omega_0^2} \int_0^{\frac{f_0}{2}} S_i(f)|NTF_i(f)|^2 |CDR(f)|^2 df$$

33

Input Reference Noise

Phase Noise at 156.26MHz

Silicon Labs Ultra Low Jitter Crystal Oscillator
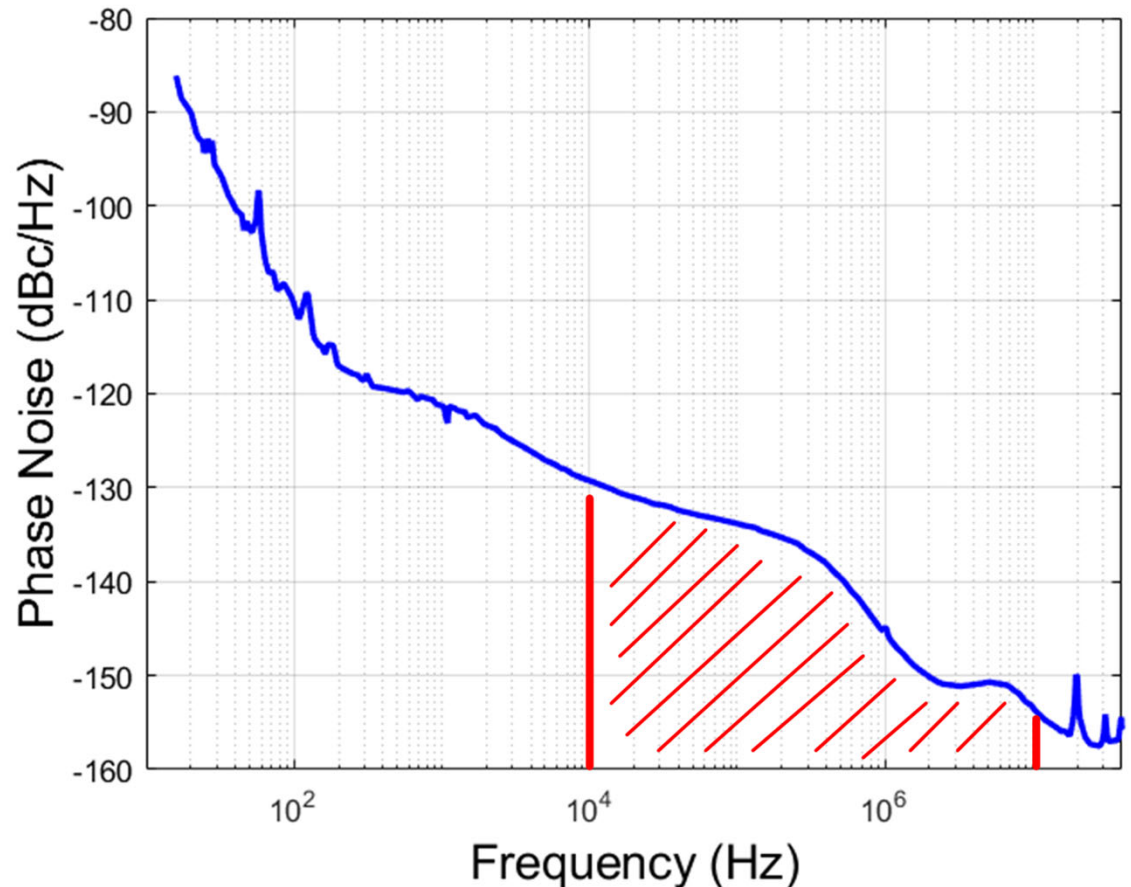
- Reference jitter $\sigma_{j,in}$ = 226fs$_{rms}$ (10kHz − 10MHz)

Input Reference Noise

$$NTF_{IN}(s) = \frac{\frac{K_{PD}K_{VCO}}{C_2}\left(s + \frac{1}{RC_1}\right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1C_2}\right)s^2 + \left(\frac{K_{PD}K_{VCO}}{NC_2}\right)s + \frac{K_{PD}K_{VCO}}{NRC_1C_2}}$$
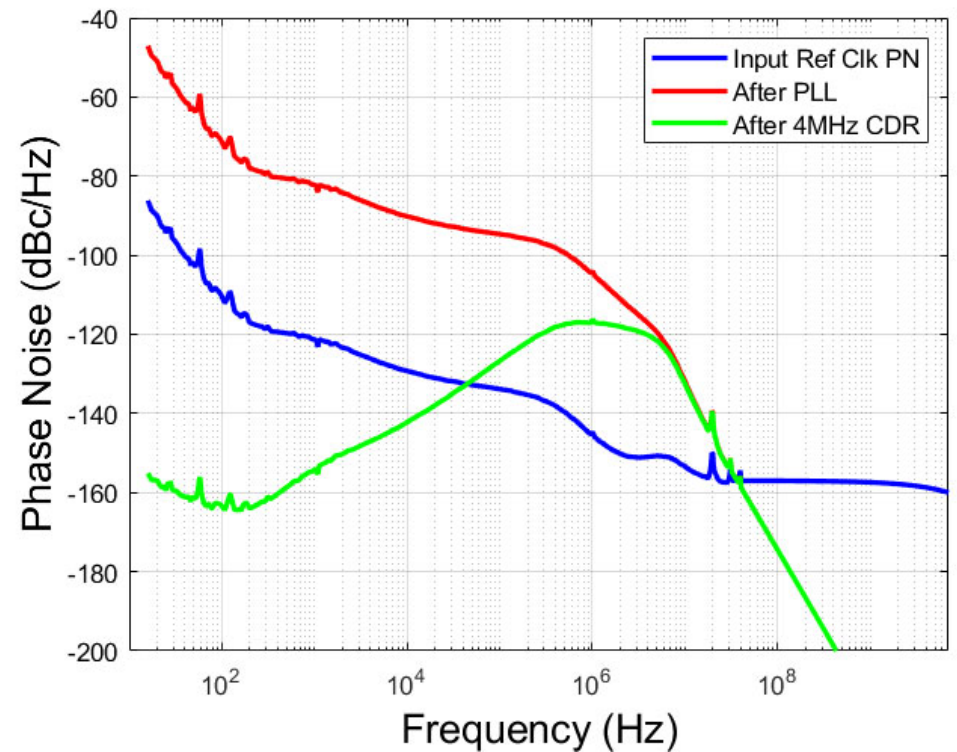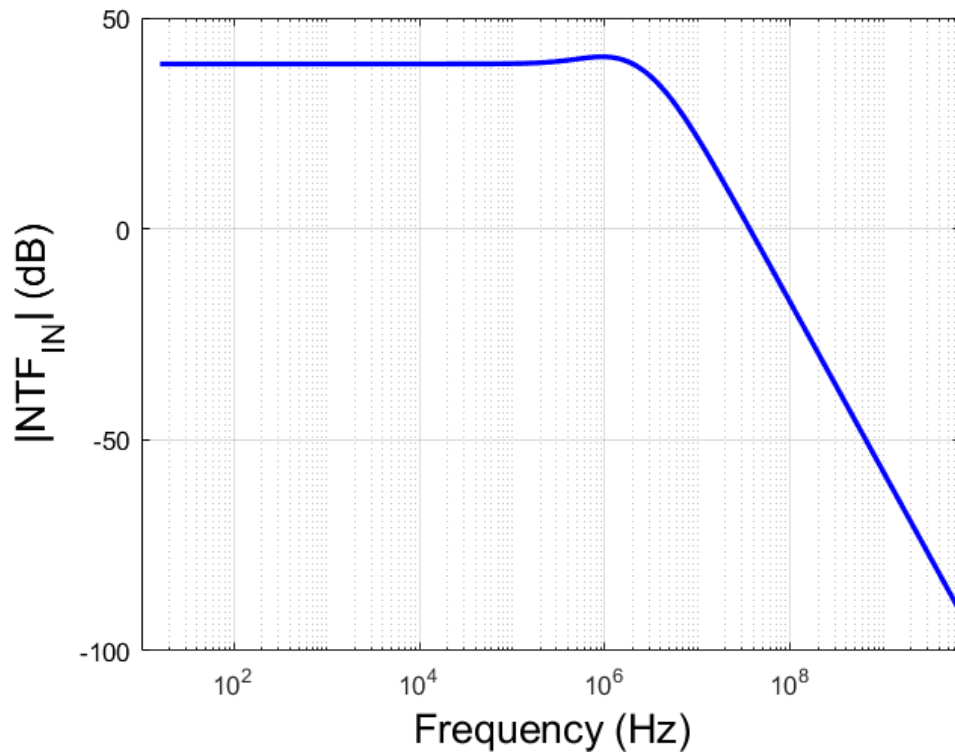
- After PLL: $\sigma_{j,in}$ = 217fs$_{rms}$ (10kHz − 10MHz)
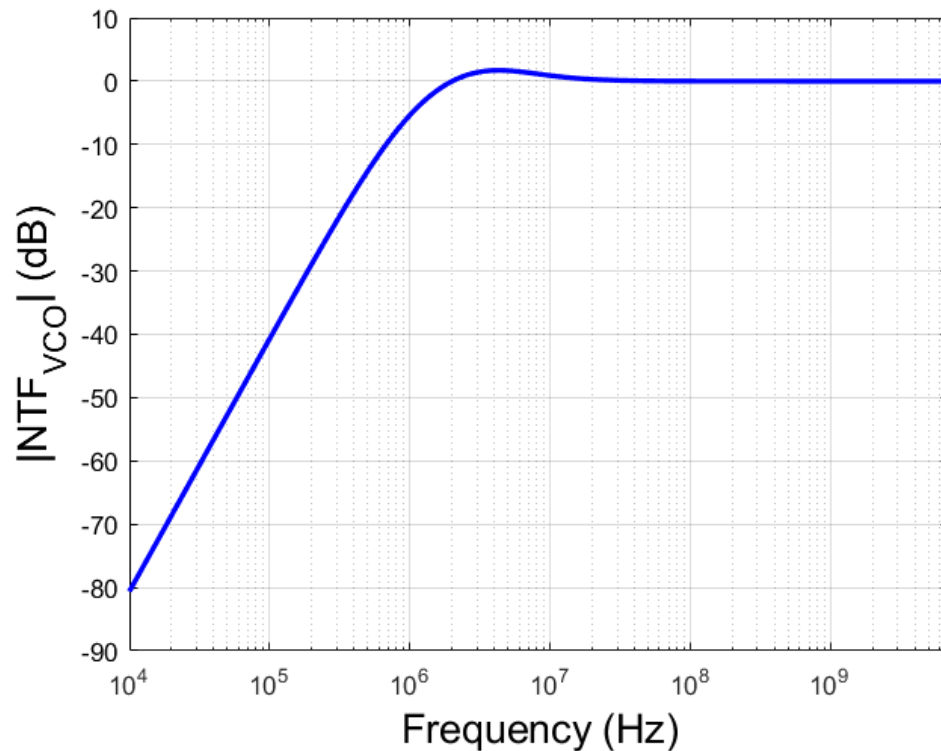- Including CDR: $\sigma_{j,in}$ = 45fs$_{rms}$ (100Hz − 7GHz)

Charge Pump Noise

[Lacaita 2007]

$\tau = T_{rst}$

$$\frac{\langle i_{CP}^2 \rangle}{\Delta f} \quad * \quad \frac{\tau^2}{T_{ref}^2}$$
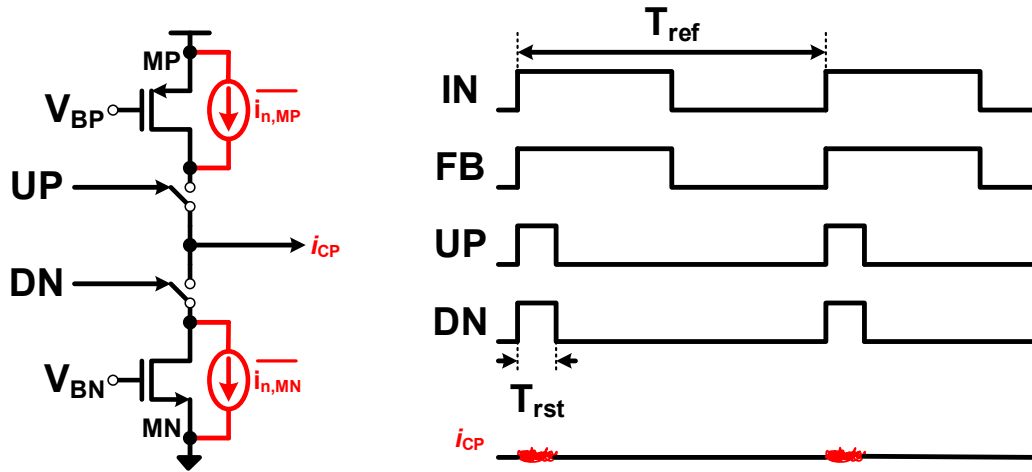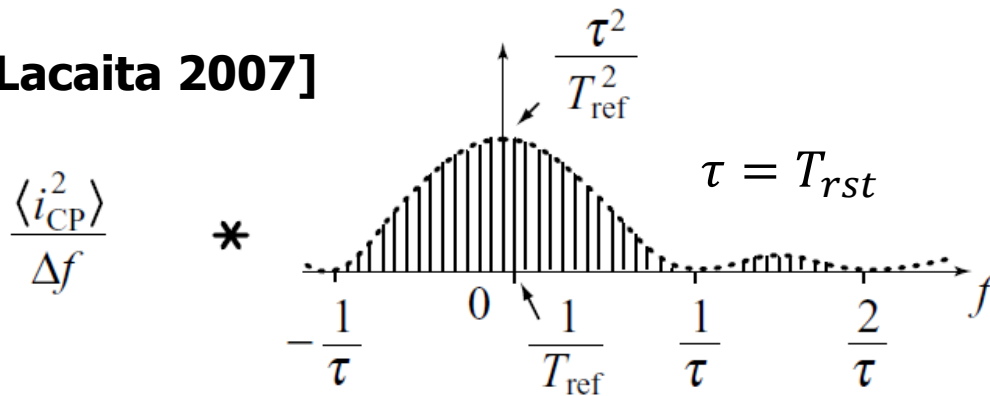
$$S_{i_{CP}} \approx \frac{T_{rst}}{T_{ref}}\left(S_{i_{n,MP,W}} + S_{i_{n,MN,W}}\right) + \left(\frac{T_{rst}}{T_{ref}}\right)^2 \left(S_{i_{n,MP,^1/_f}} + S_{i_{n,MN,^1/_f}}\right)$$
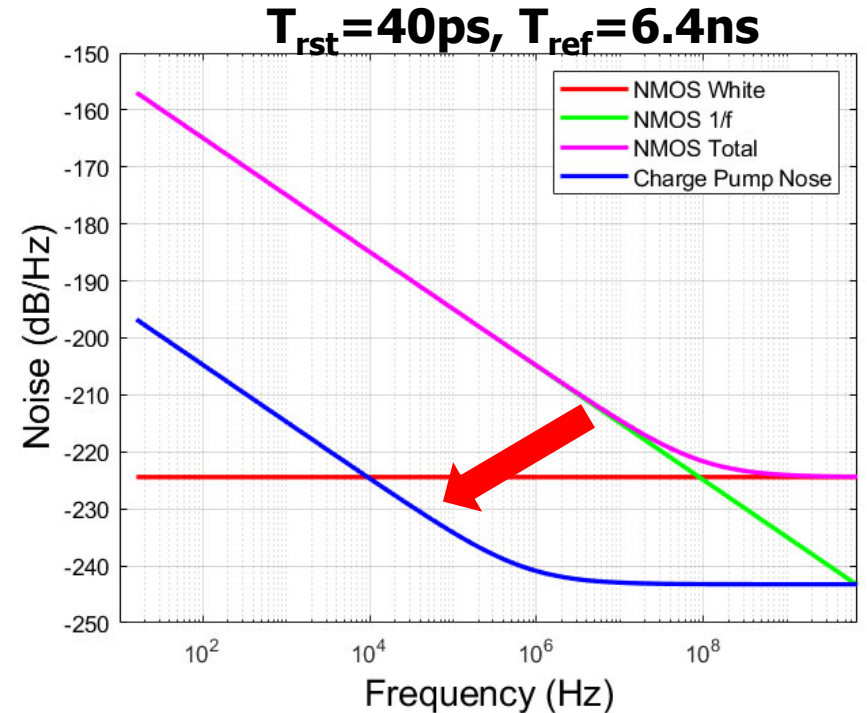
- Charge pump noise current is injected into the loop filter during the PFD reset time
- Transistor noise PSD convolved with pulse frequency spectrum
- White noise scaled by (T_{rst}/T_{ref}) and 1/f noise scaled by $(T_{rst}/T_{ref})^2$

36

Charge Pump Noise

$$NTF_{CP}(s) = \frac{\frac{K_{VCO}}{C_2}\left(s + \frac{1}{RC_1}\right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1C_2}\right)s^2 + \left(\frac{K_{PD}K_{VCO}}{NC_2}\right)s + \frac{K_{PD}K_{VCO}}{NRC_1C_2}}$$
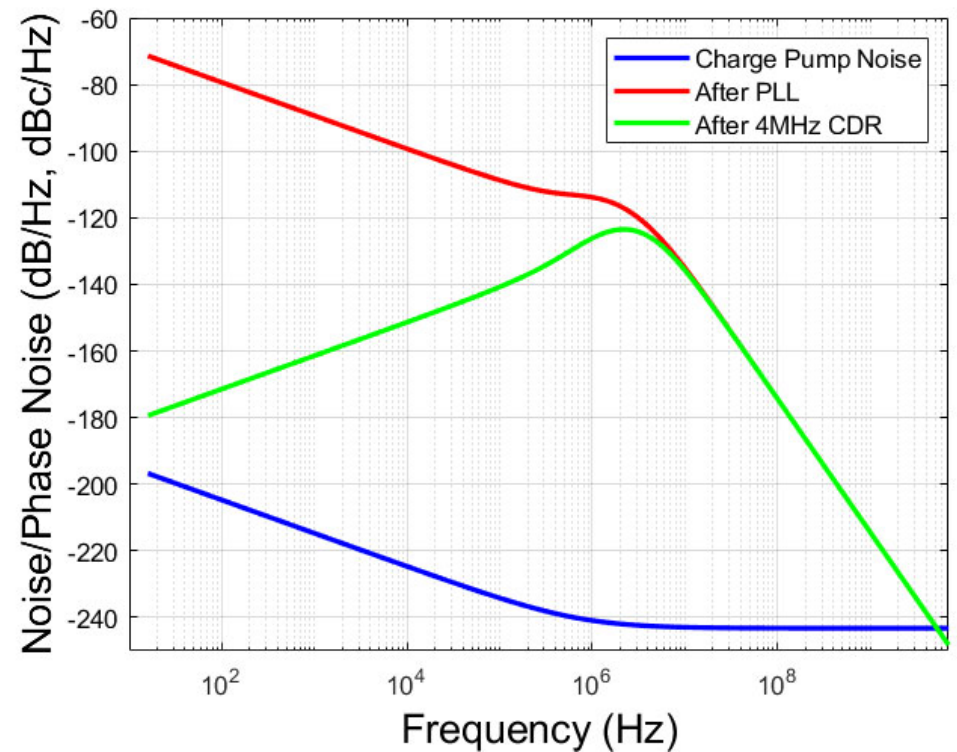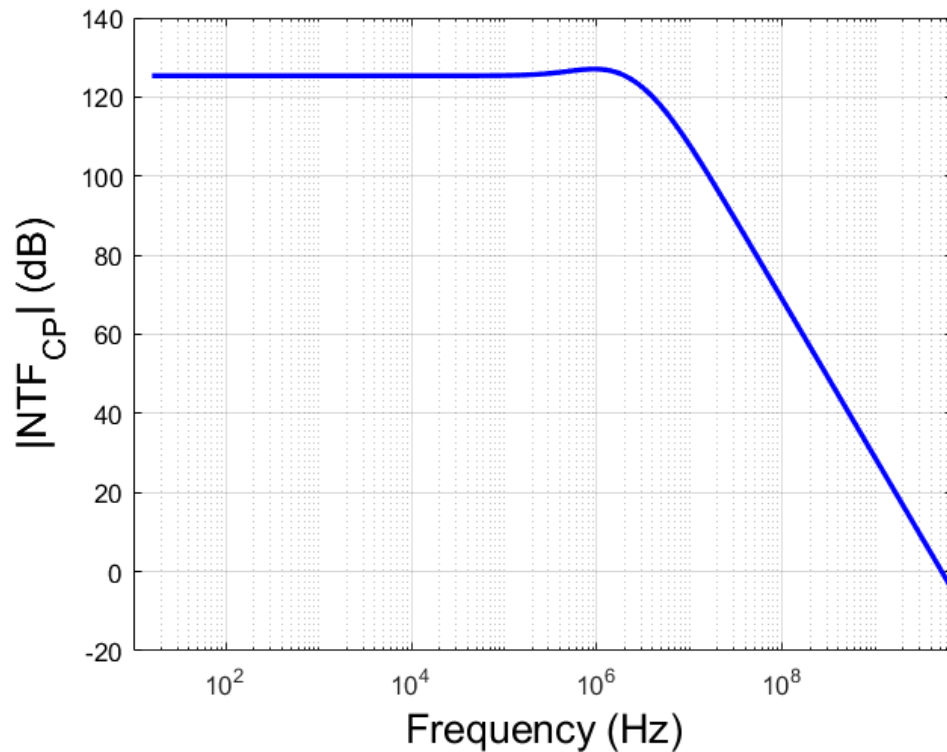
- After PLL: $\sigma_{j,CP} = 61\text{fs}_{rms}$ (10kHz $-$ 10MHz)
- Including CDR: $\sigma_{j,CP} = 22\text{fs}_{rms}$ (100Hz $-$ 7GHz)

Loop Filter R Noise

w/ 4kΩ Resistor

$$S_{v_R} = 4kTR = -162\, dB/Hz$$
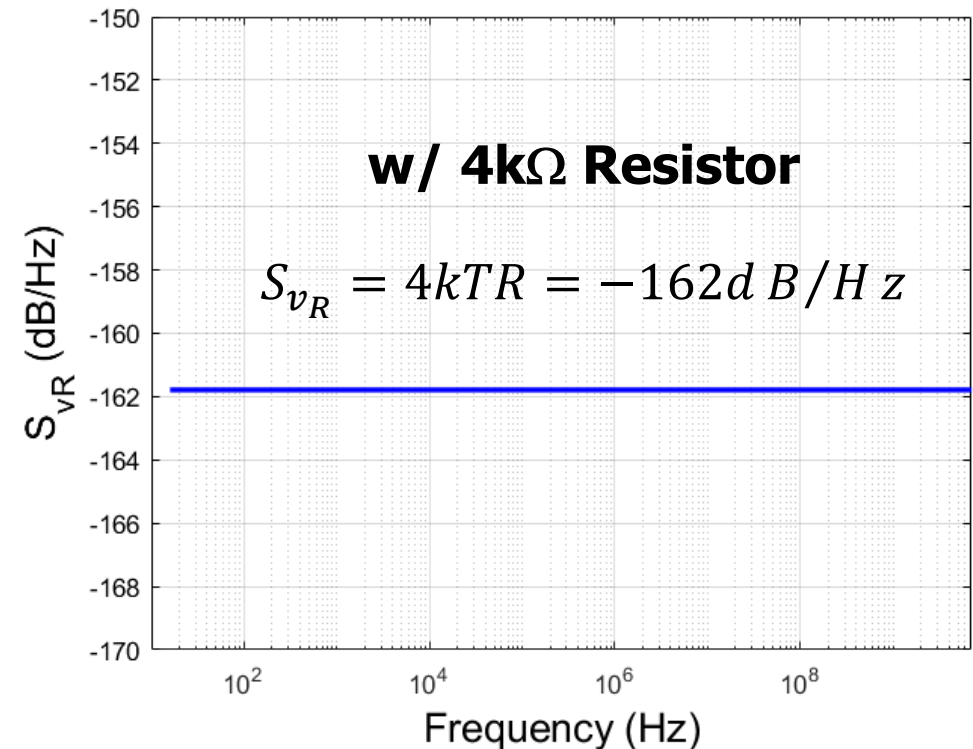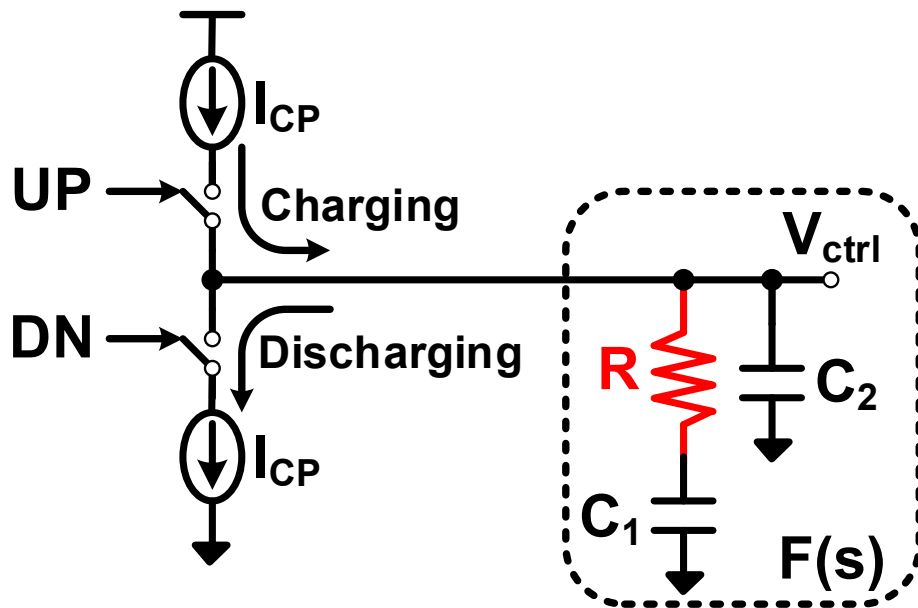
- Trade-off between resistor noise, loop filter capacitor size, and charge pump noise
  - Smaller resistor results in larger capacitors (higher area) and larger charge pump current (higher S_{iCP})

Loop Filter R Noise

$$NTF_R(s) = \frac{K_{VCO}s\left(s + \frac{C_1 + C_2}{RC_1C_2}\right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1C_2}\right)s^2 + \left(\frac{K_{PD}K_{VCO}}{NC_2}\right)s + \frac{K_{PD}K_{VCO}}{NRC_1C_2}}$$
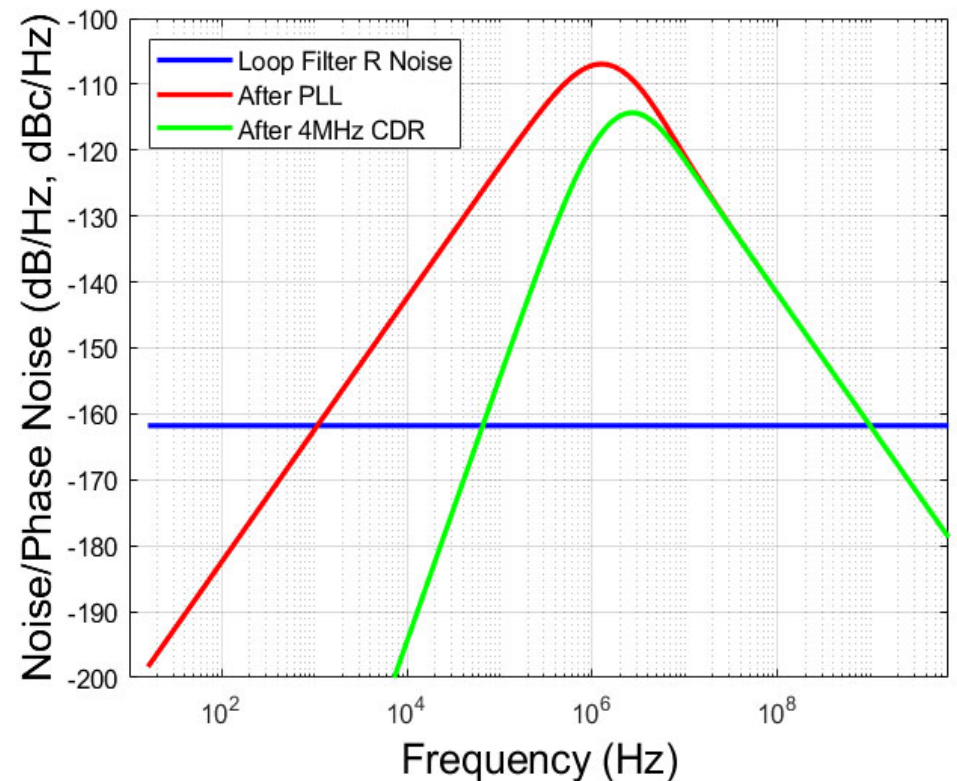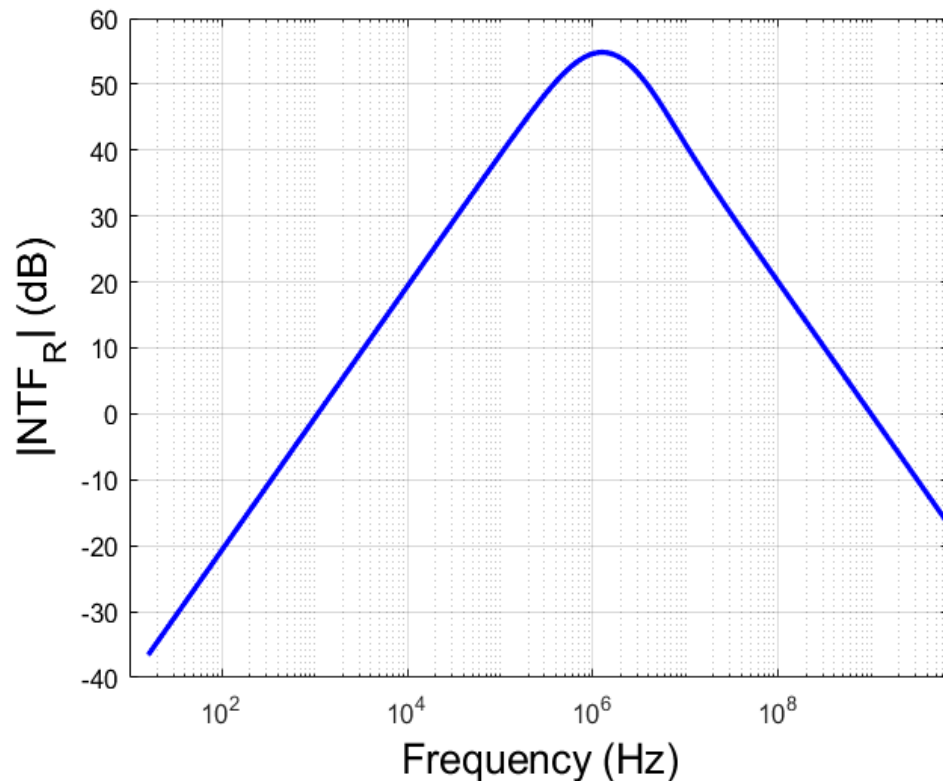
- After PLL: $\sigma_{j,R} = 128\text{fs}_{rms}$ (10kHz $-$ 10MHz)
- Including CDR: $\sigma_{j,R} = 81\text{fs}_{rms}$ (100Hz $-$ 7GHz)

VCO Noise

**LC-Oscillator
w/ Differential Tank & Noise Sources**
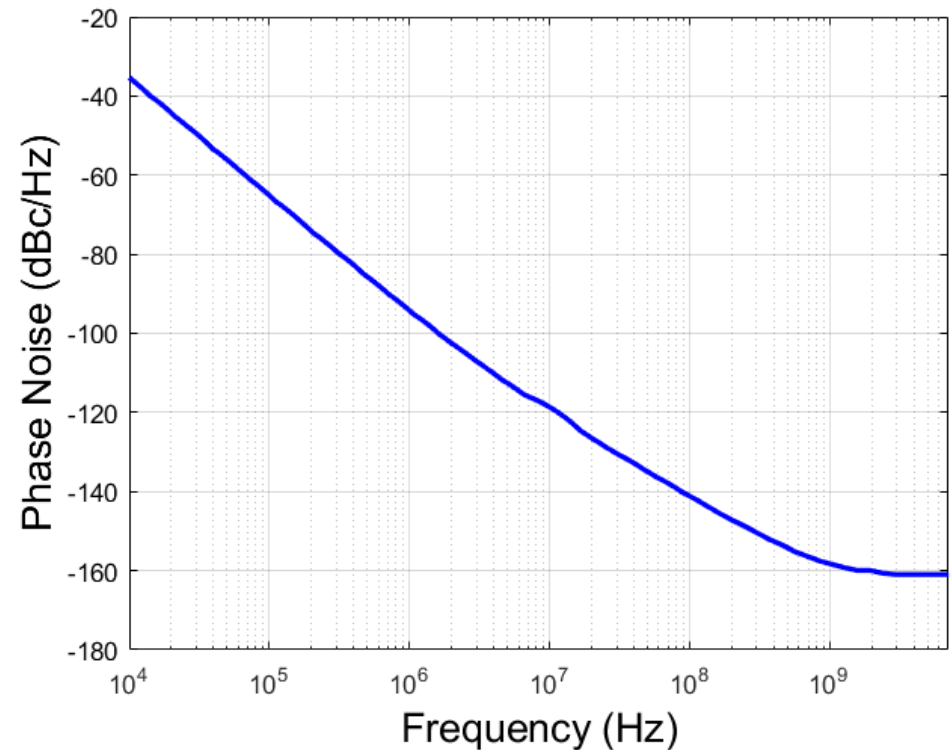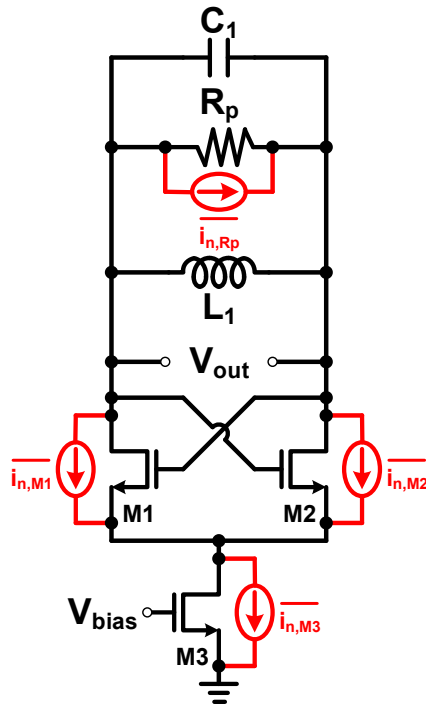
- ## LC-VCO phase noise sources
  - Finite tank quality factor
  - Cross-coupled pair
  - Tail current source

40

VCO Noise

$$NTF_{VCO}(s) = \frac{s^2\left(s + \frac{C_1 + C_2}{RC_1C_2}\right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1C_2}\right)s^2 + \left(\frac{K_{PD}K_{VCO}}{NC_2}\right)s + \frac{K_{PD}K_{VCO}}{NRC_1C_2}}$$
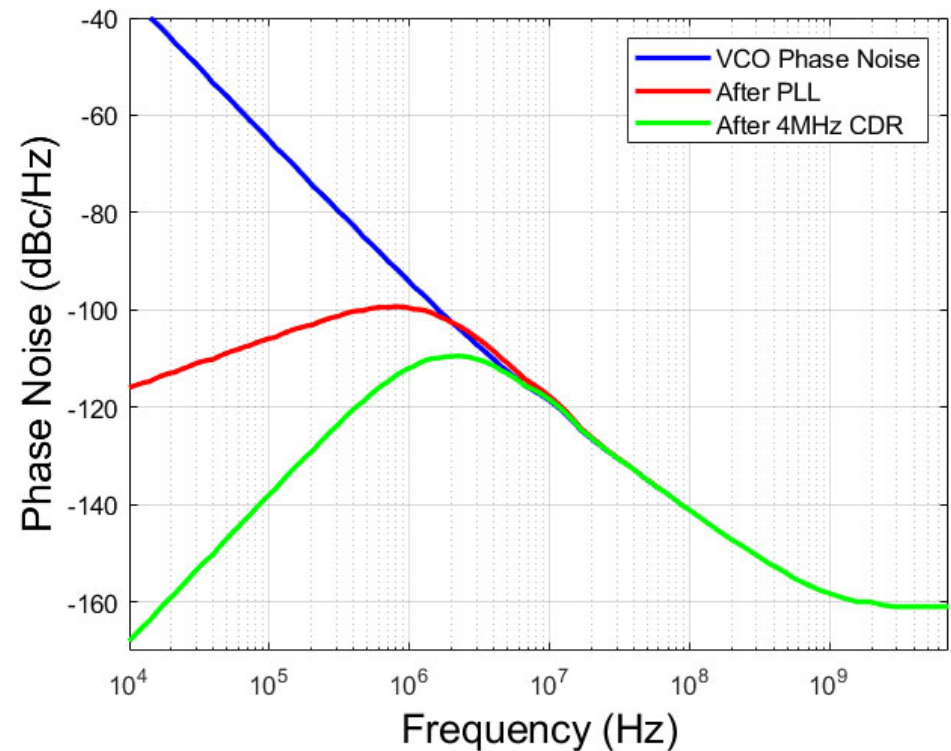
- After PLL: $\sigma_{j,VCO} = 257\text{fs}_{rms}$ (10kHz − 10MHz)
- Including CDR: $\sigma_{j,R} = 125\text{fs}_{rms}$ (100Hz − 7GHz)

Total Noise
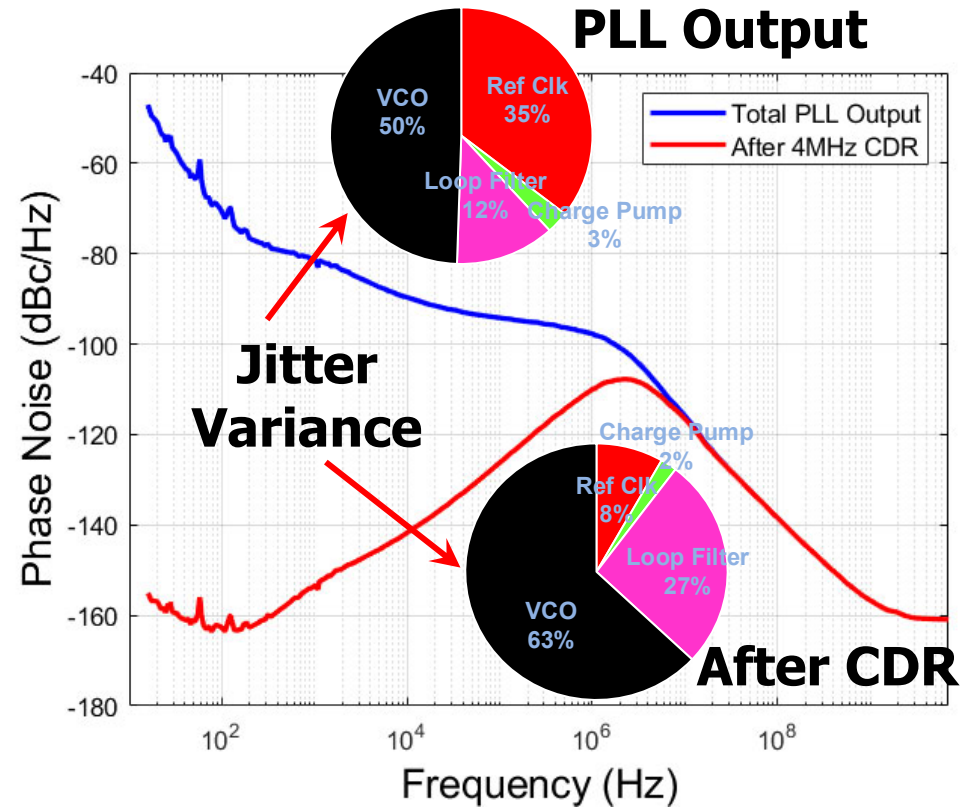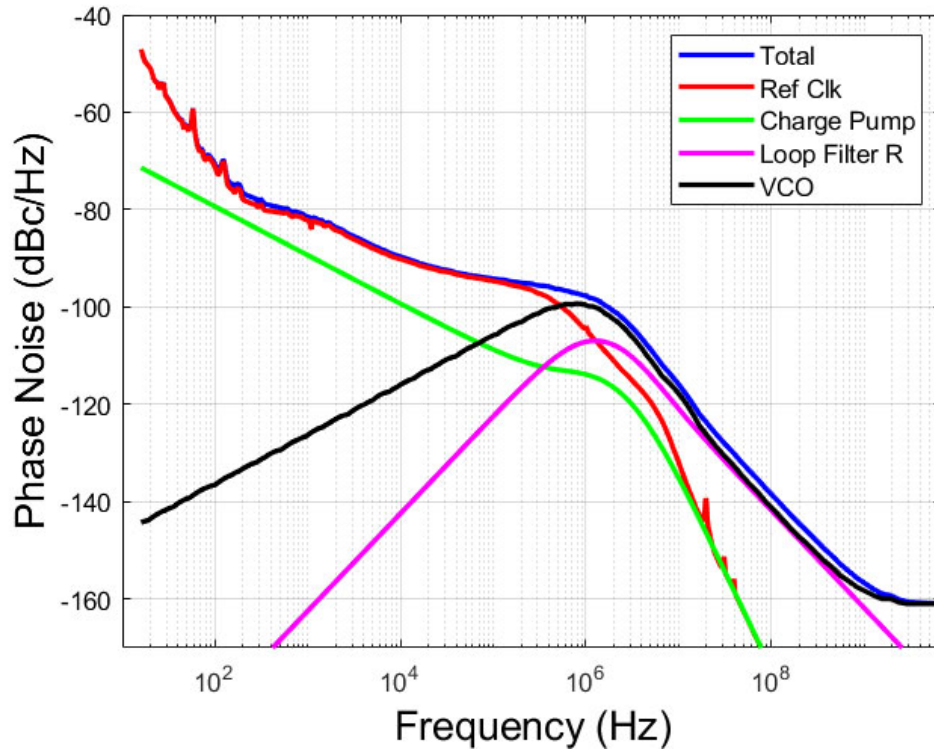
- After PLL: $\sigma_{j,Total} = 365\text{fs}_{rms}$ (10kHz – 10MHz)
  - Reference clock noise dominates at low frequency
  - VCO dominates near loop bandwidth and higher
- Including CDR: $\sigma_{j,Total} = 157\text{fs}_{rms}$ (100Hz – 7GHz)
  - Now VCO noise clearly dominates total
  - Loop resistor noise is a larger percentage

42

PLL Noise Transfer Function Take-Away Points

- The way a PLL shapes phase noise depends on where the noise is introduced in the loop

- Optimizing the loop bandwidth for one noise source may enhance other noise sources

- Generally, the PLL low-pass shapes input phase noise, band-pass shapes VCO input voltage noise, and high-pass shapes VCO/clock buffer output phase noise

Oscillator Noise

Jitter

V(t)

Φ(t)

4π
3π
2π
π
0

ω(t)
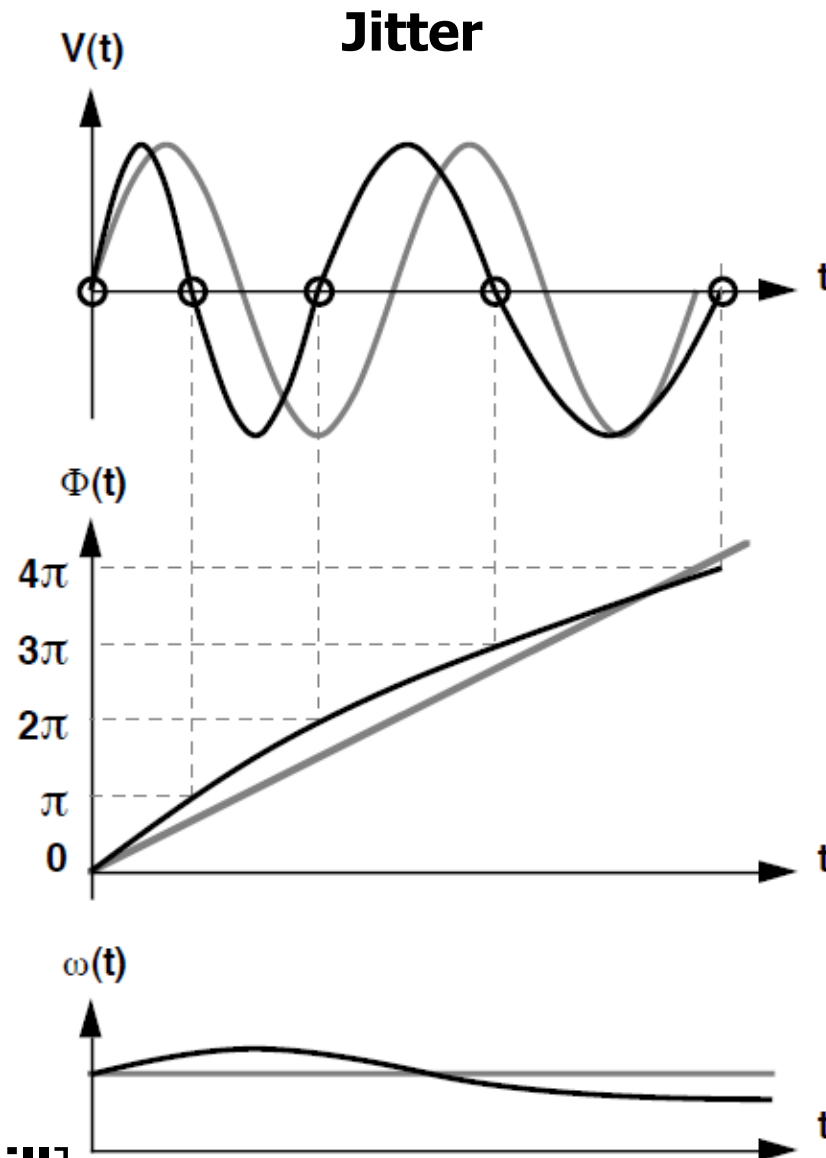
PHASE NOISE

[**McNeill**]
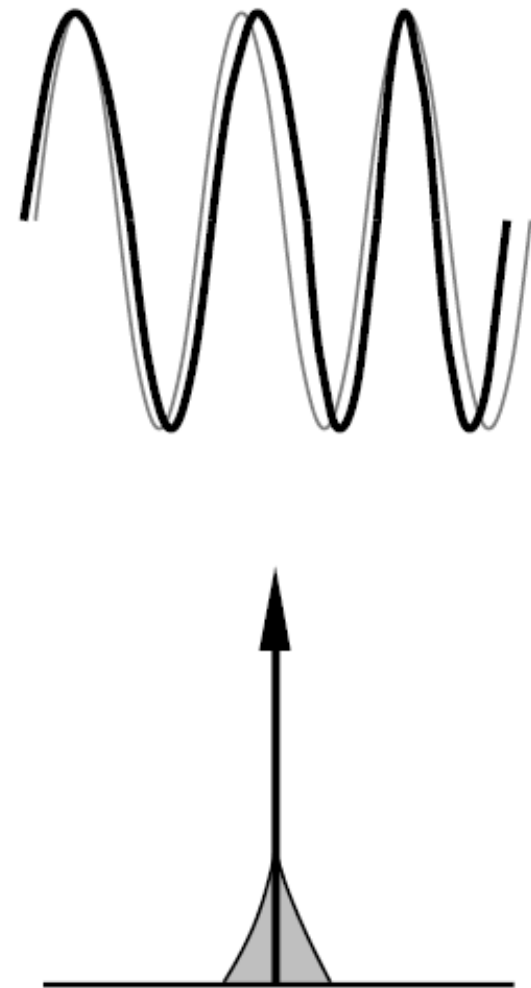
Oscillator Phase Noise Model
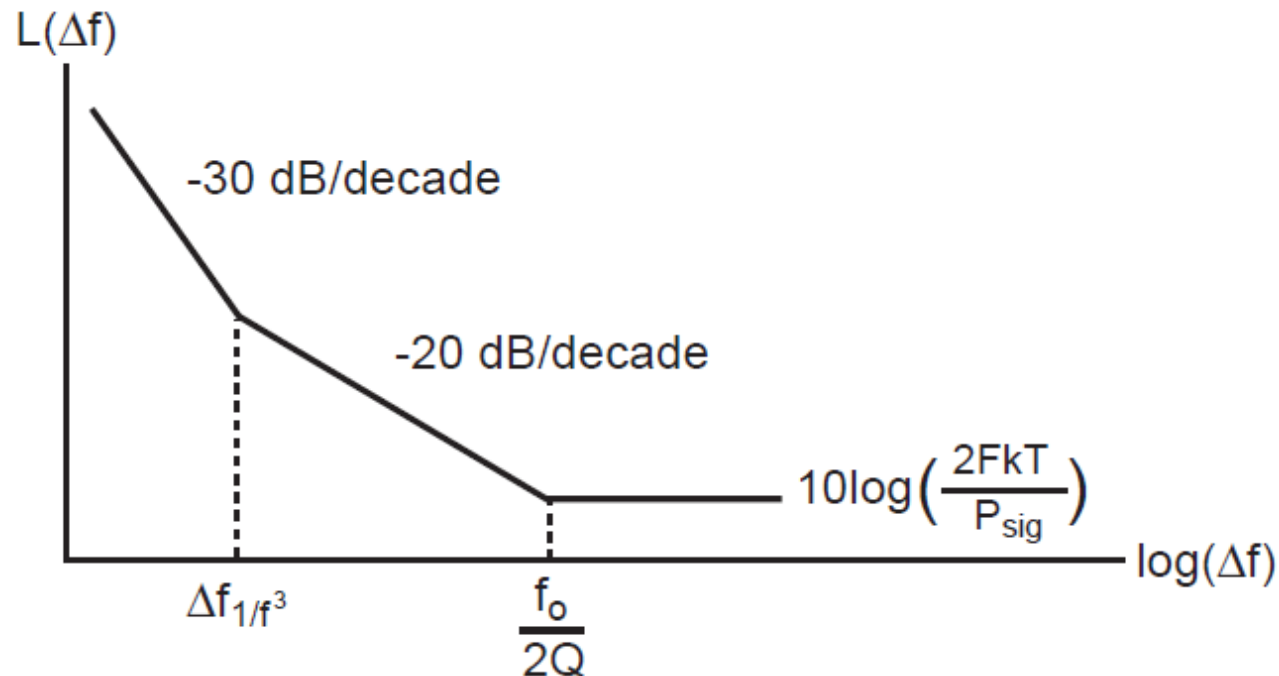
[**Perrott**]

$$L(f) = 10\log\left(\frac{\textbf{Noise Spectral Density}}{\textbf{Carrier Power}}\right) \ (\textbf{dBc/Hz})$$

Leeson's Model:
$$L(\Delta f) = 10\log\left(\frac{2FkT}{P_{sig}}\left(1 + \left(\frac{1}{2Q}\frac{f_o}{\Delta f}\right)^2\right)\left(1 + \frac{\Delta f_{1/f^3}}{|\Delta f|}\right)\right)$$

- For improved model see Hajimiri papers

Open-Loop VCO Jitter

[**McNeill**]

TRIGGER   Average delay = NT_o
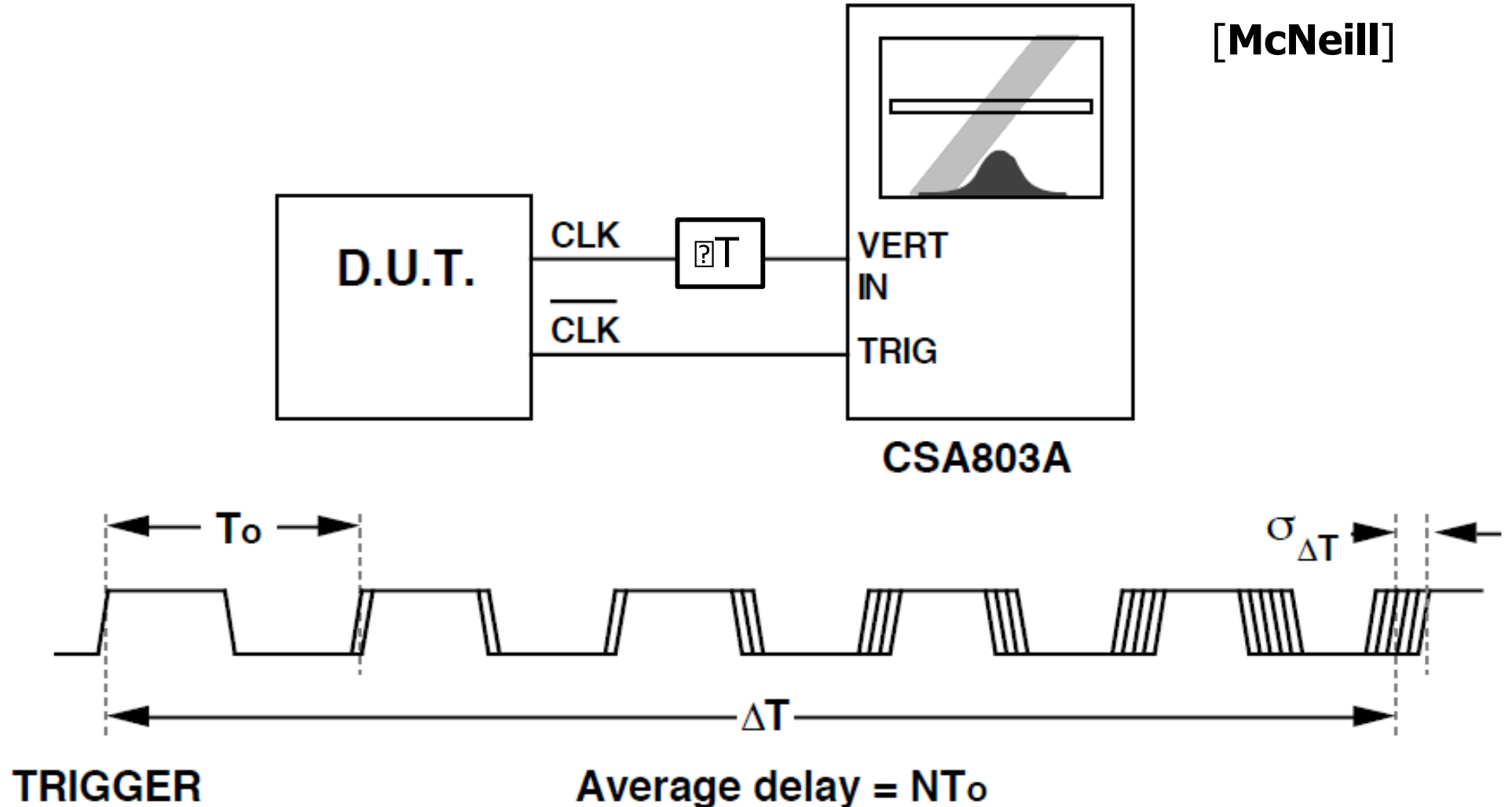
- Measure distribution of clock threshold crossings
- Plot σ as a function of delay ΔT

Open-Loop VCO Jitter
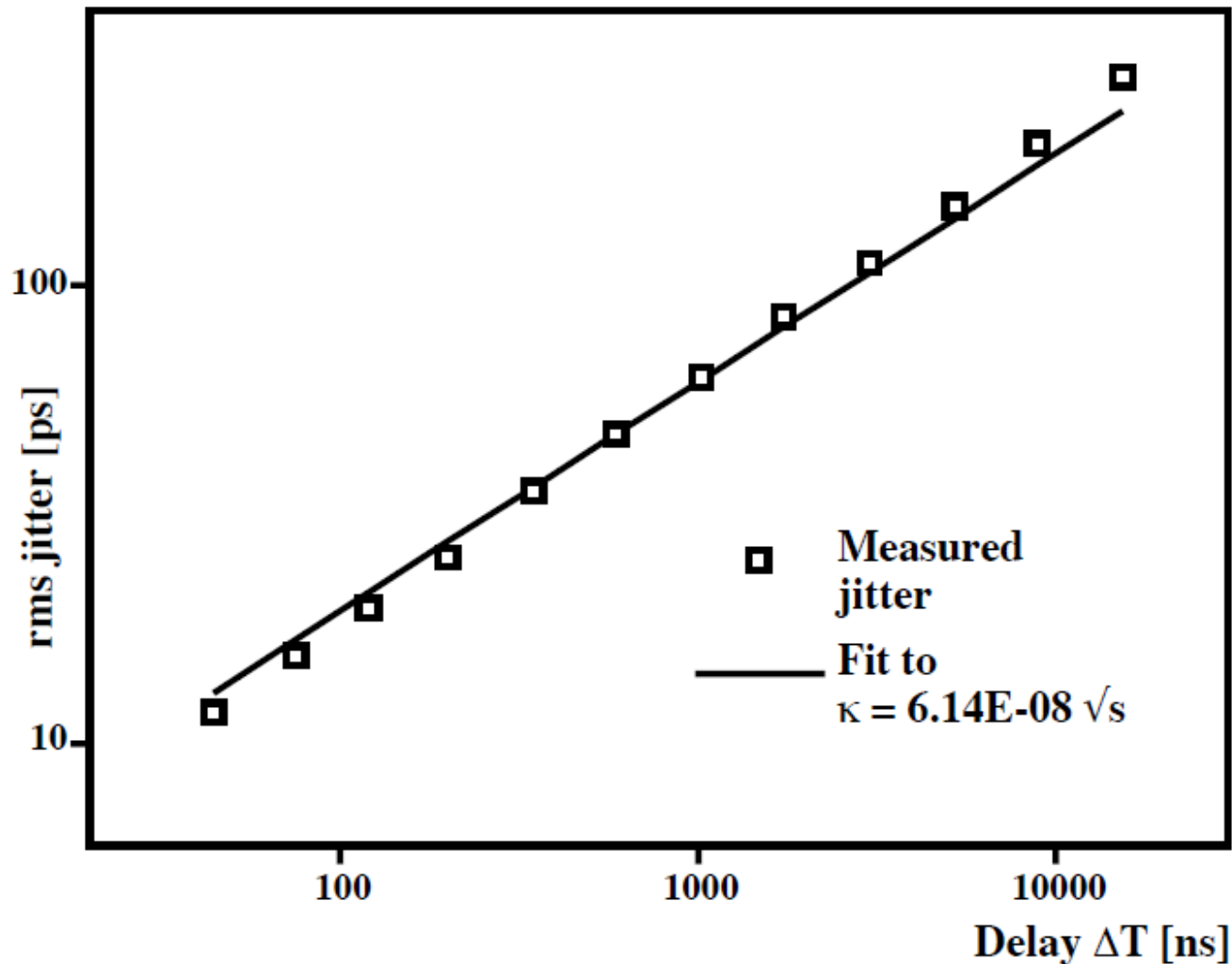
[**McNeill**]

$$\sigma_{\Delta T(OL)}(\Delta T) \approx \kappa \sqrt{\Delta T}$$

- Jitter σ is proportional to sqrt(ΔT)
- κ is VCO time domain figure of merit

VCO in Closed-Loop PLL Jitter
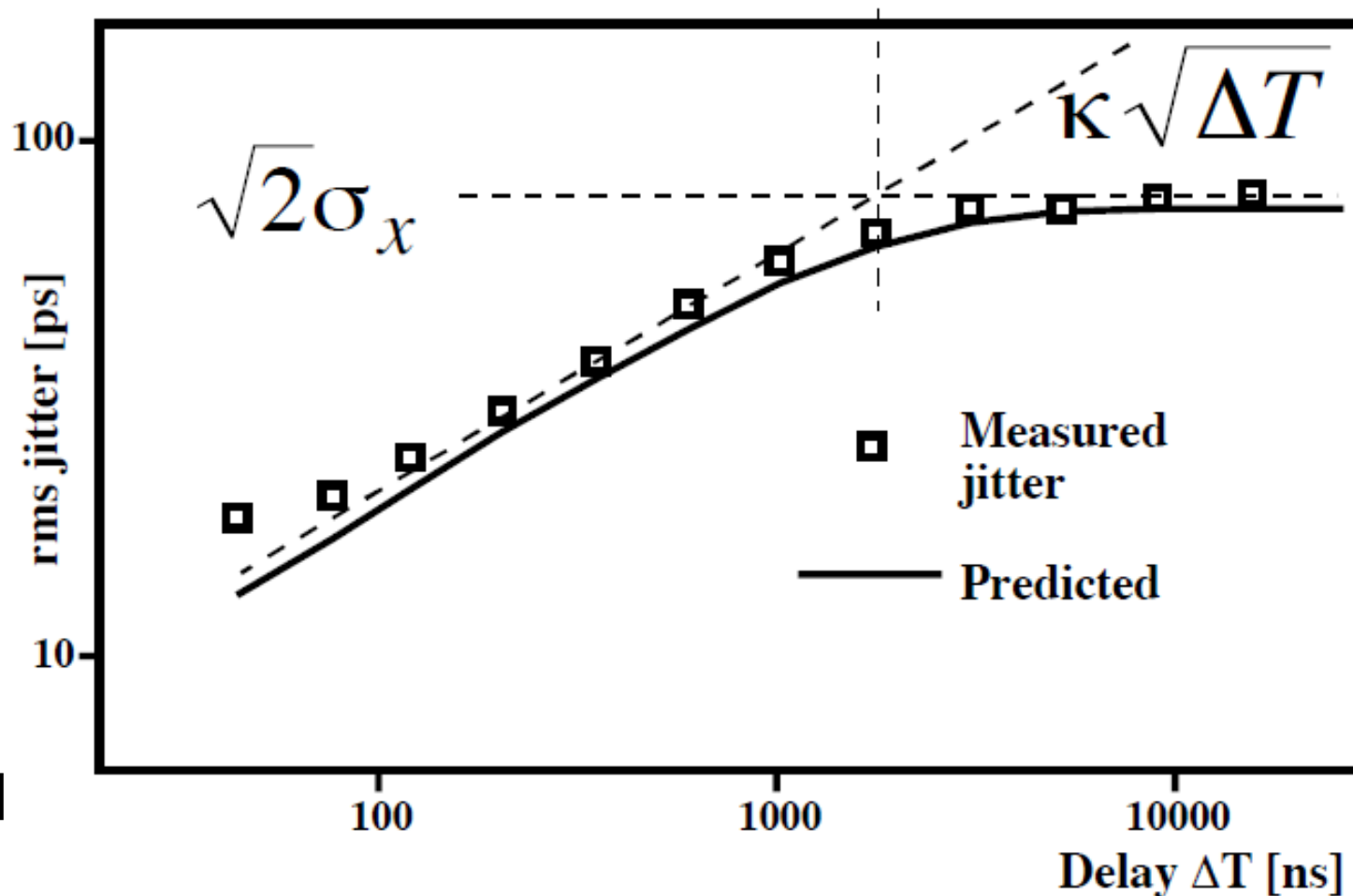
[**McNeill**]

- PLL limits σ for delays longer than loop bandwidth τ_L

$$\tau_L = 1/2\pi f_L$$

Ref Clk-Referenced vs Self-Referenced

[**McNeill**]

CDR Example
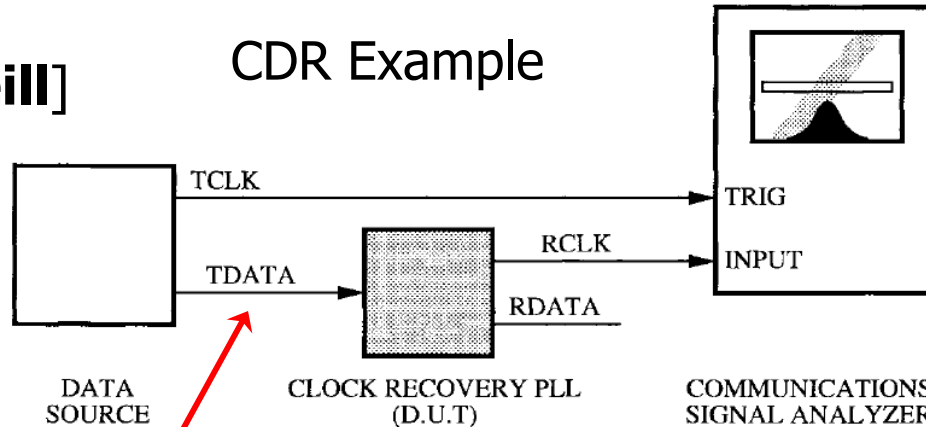
Ref Clock for
Frequency Synthesis PLL
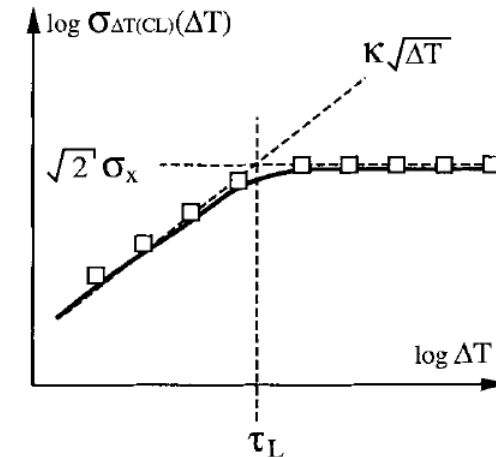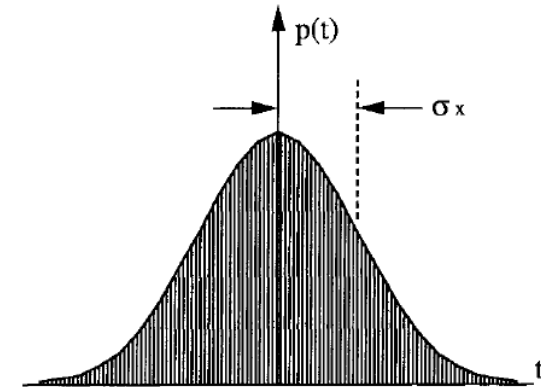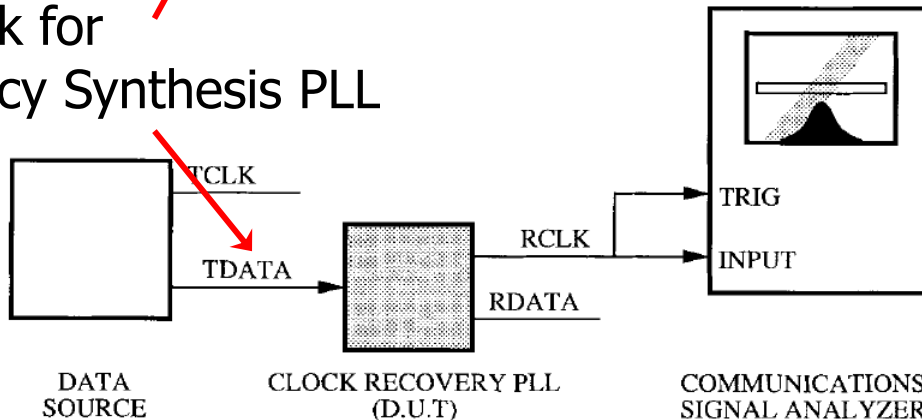
- Generally, we care about the jitter w.r.t. the ref. clock (σ_x)
- However, may be easier to measure w.r.t. delayed version of output clk
  - Due to noise on both edges, this will be increased by a sqrt(2) factor relative to the reference clock-referred jitter

49

Converting Phase Noise to Jitter
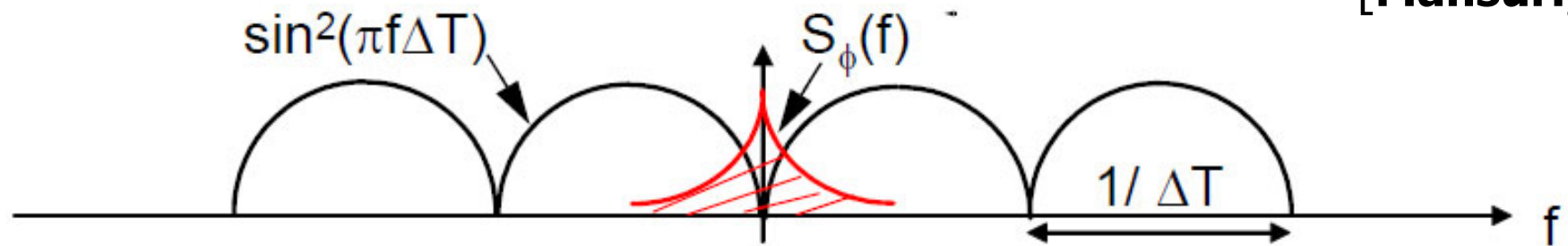
- RMS jitter for ΔT accumulation $\quad \sigma_{\Delta T}^2 = \dfrac{8}{\omega_o^2} \displaystyle\int_0^\infty S_\phi(f) sin^2(\pi f \Delta T) df$

- As ΔT goes to ∞ $\quad \sigma_T^2 = \dfrac{2}{\omega_o^2} R_\phi(0) = \dfrac{2}{\omega_o^2} \displaystyle\int_0^\infty S_\phi(f) df$

- Actual integration range depends on application bandwidth
    - f_{min} set by assumed CDR tracking bandwidth
    - f_{max} set by Nyquist frequency ($f_0/2$)

- Most exact approach $\quad \sigma_T^2 = \dfrac{2}{\omega_o^2} \displaystyle\int_0^{f_0/2} S_\phi(f) \left| H_{sys}(f) \right|^2 df$

where $\left| H_{sys}(f) \right|^2$ is the system jitter transfer function

50

Time Domain Model

- Time domain models captures the discrete-time operation of the PLL architectures
  - Interaction between charge pump and loop filter
  - Cycle slipping behavior

- Allows modeling of non-linear control systems
  - Dynamic loop bandwidth control
  - Automatic frequency band selection

- Potential implementation tools
  - Matlab Simulink
  - CppSim
  - Cadence

Simulink Model

PLL FREQUENCY SYNTHESIZER MODEL

PFD

Loop Filter

52
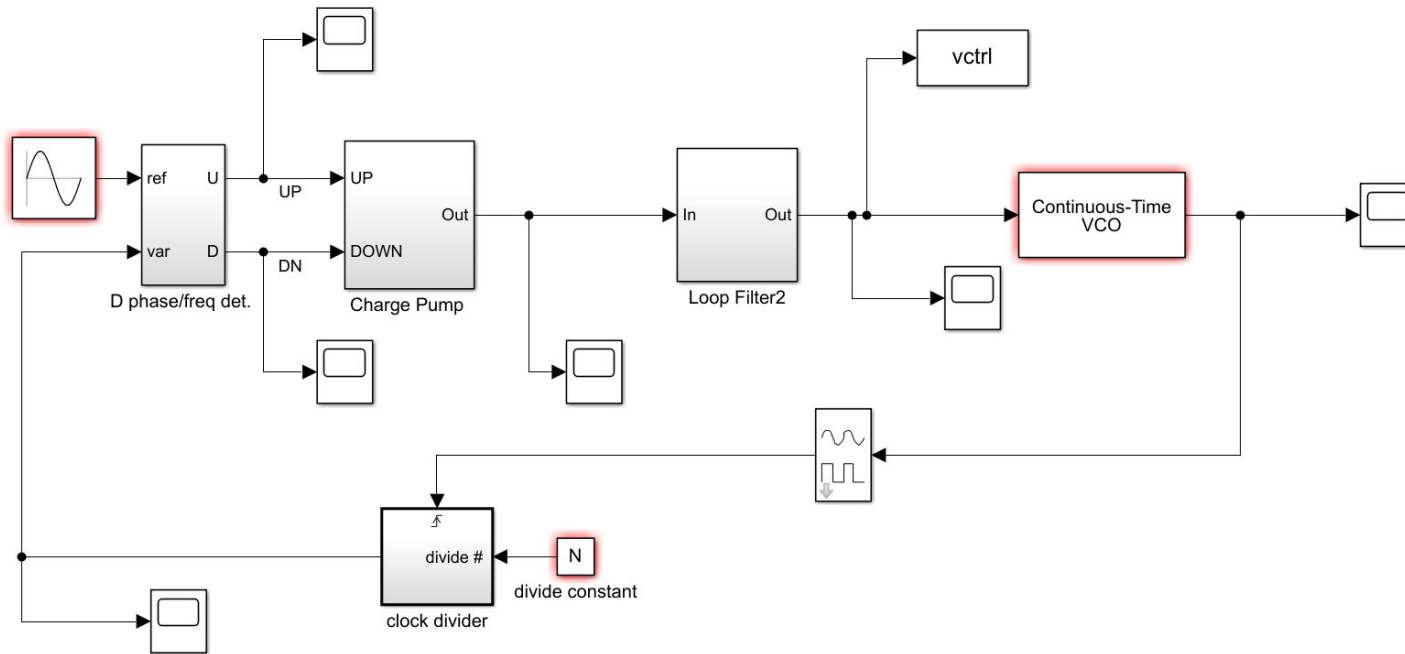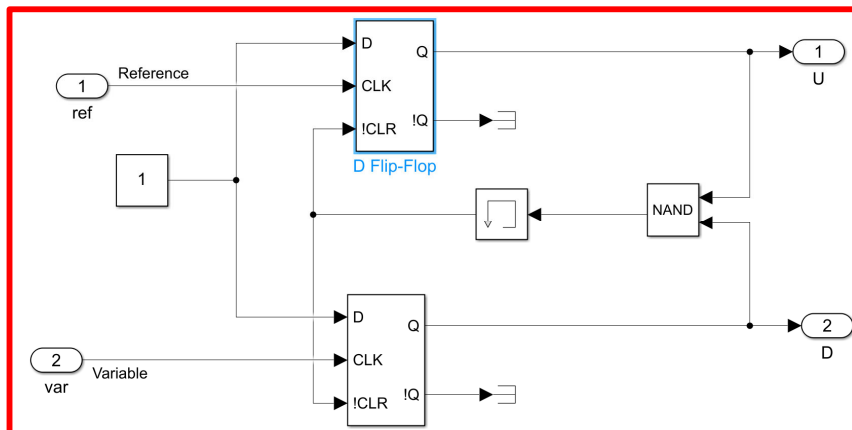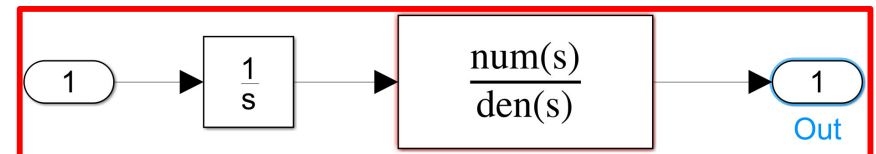
Frequency Step w/ Simulink Model

- VCO control voltage response to input frequency step

$K_{VCO}=2\pi*1GHz/V$ (LC Osc)

$K_{VCO}=2\pi*10GHz/V$ (Ring Osc)
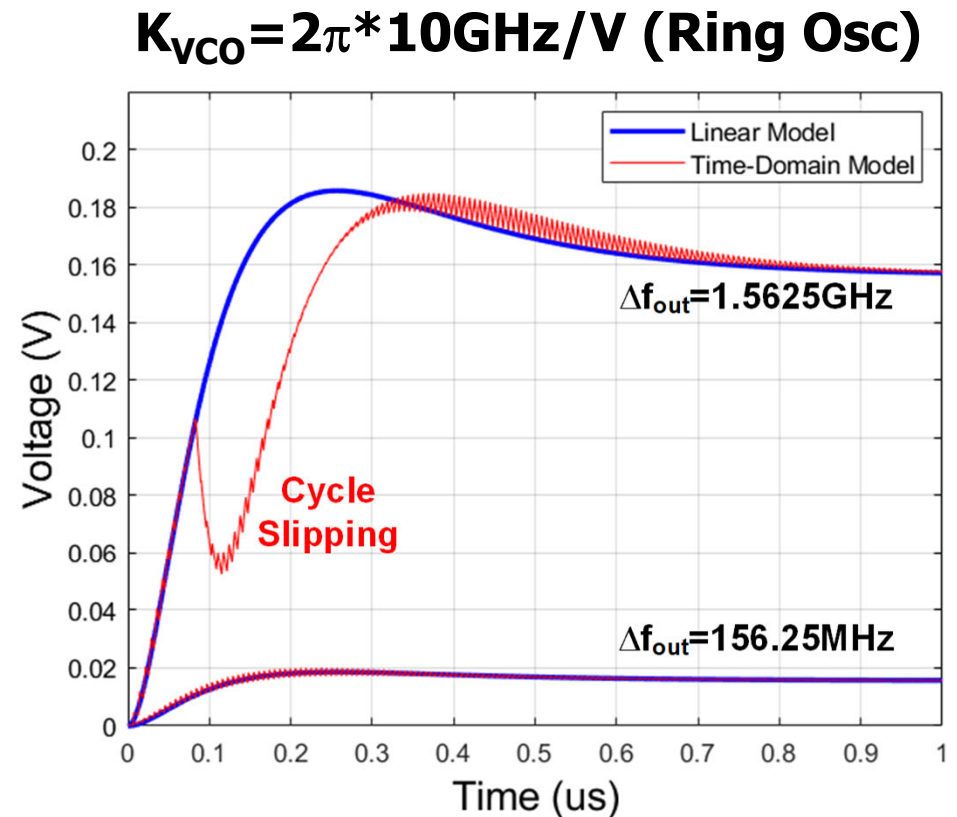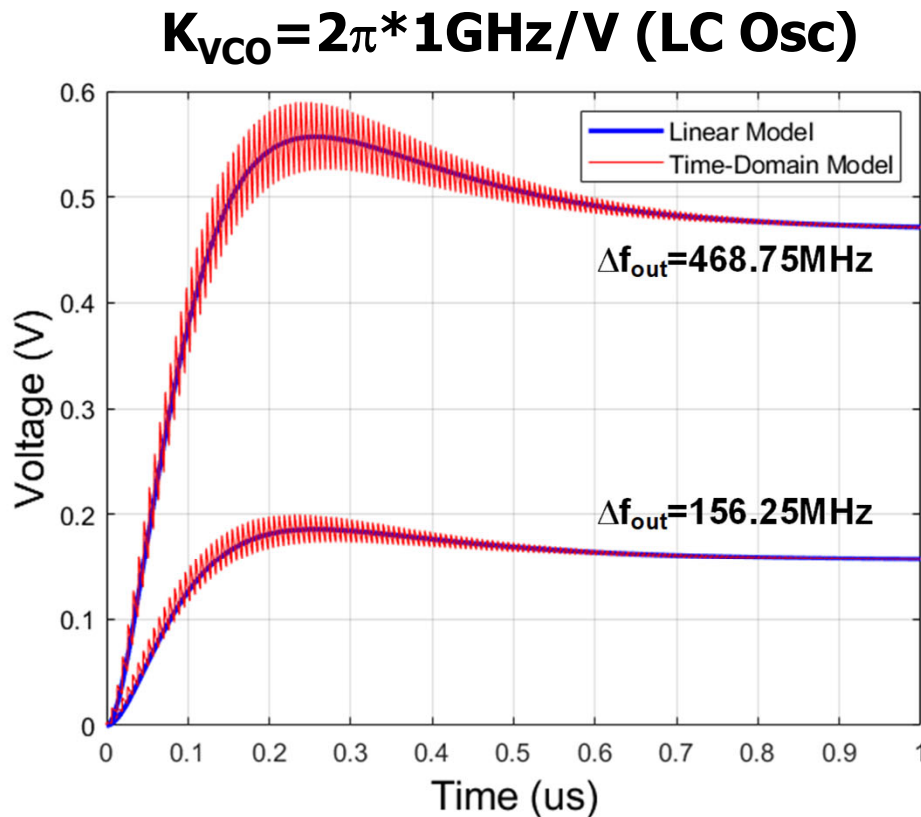
- Voltage spikes due to charge pump current driving loop filter resistor
- Cycle slipping occurs during lock acquisition due to large initial frequency difference

CppSim Model

[Perrott/Meninger]
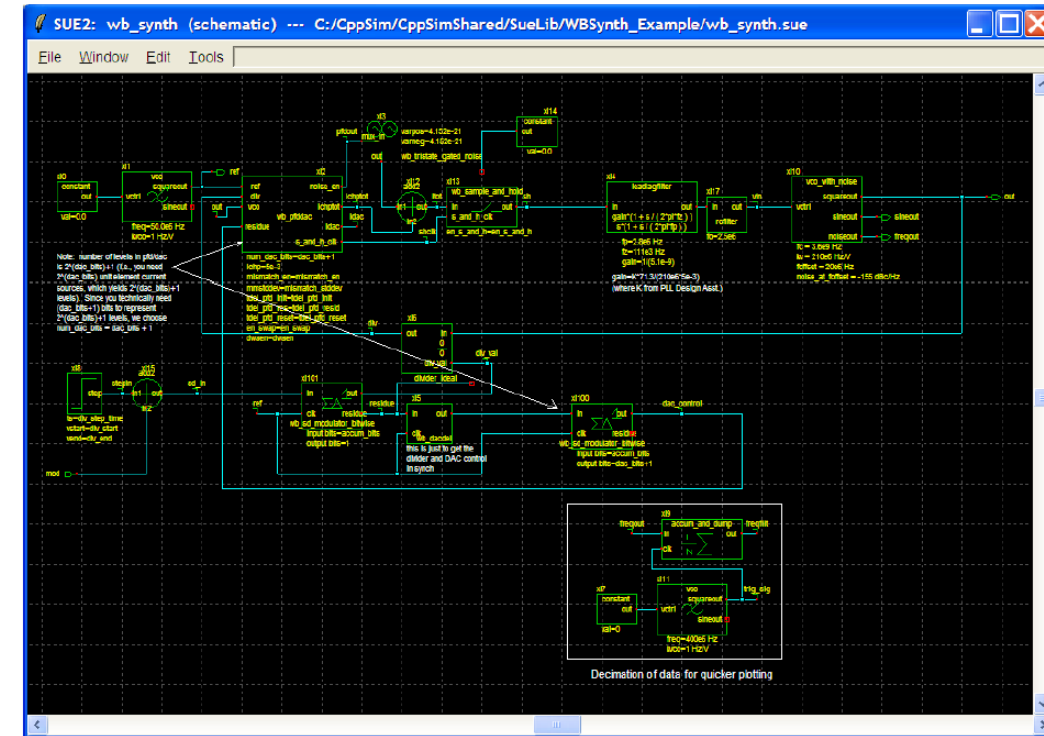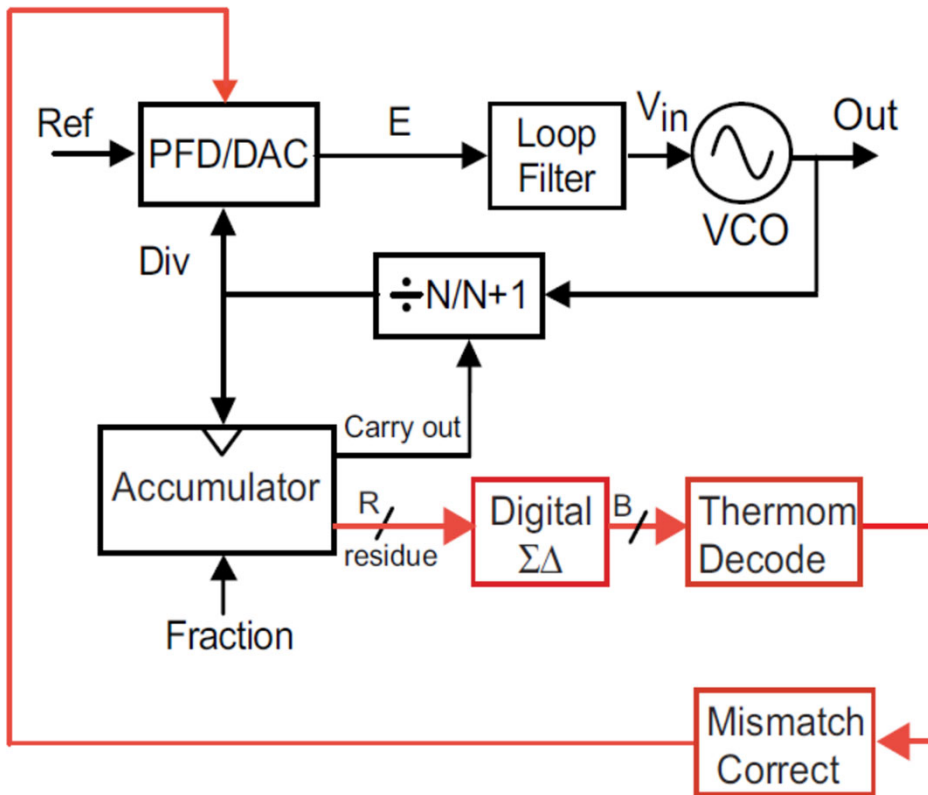
- https://cppsim.com/
- C++ based allows for rapid simulation of advanced architectures
- Many useful building blocks included

54
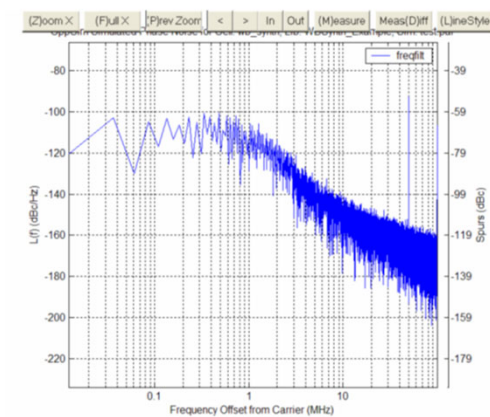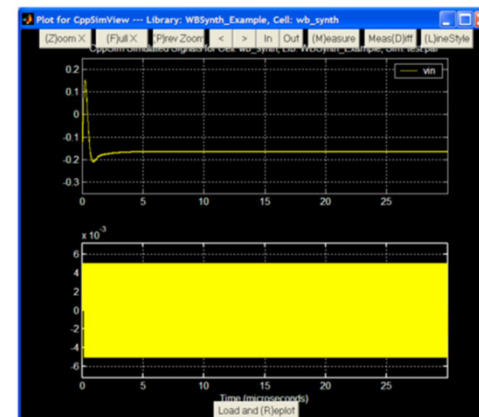
Cadence Verilog-A Model
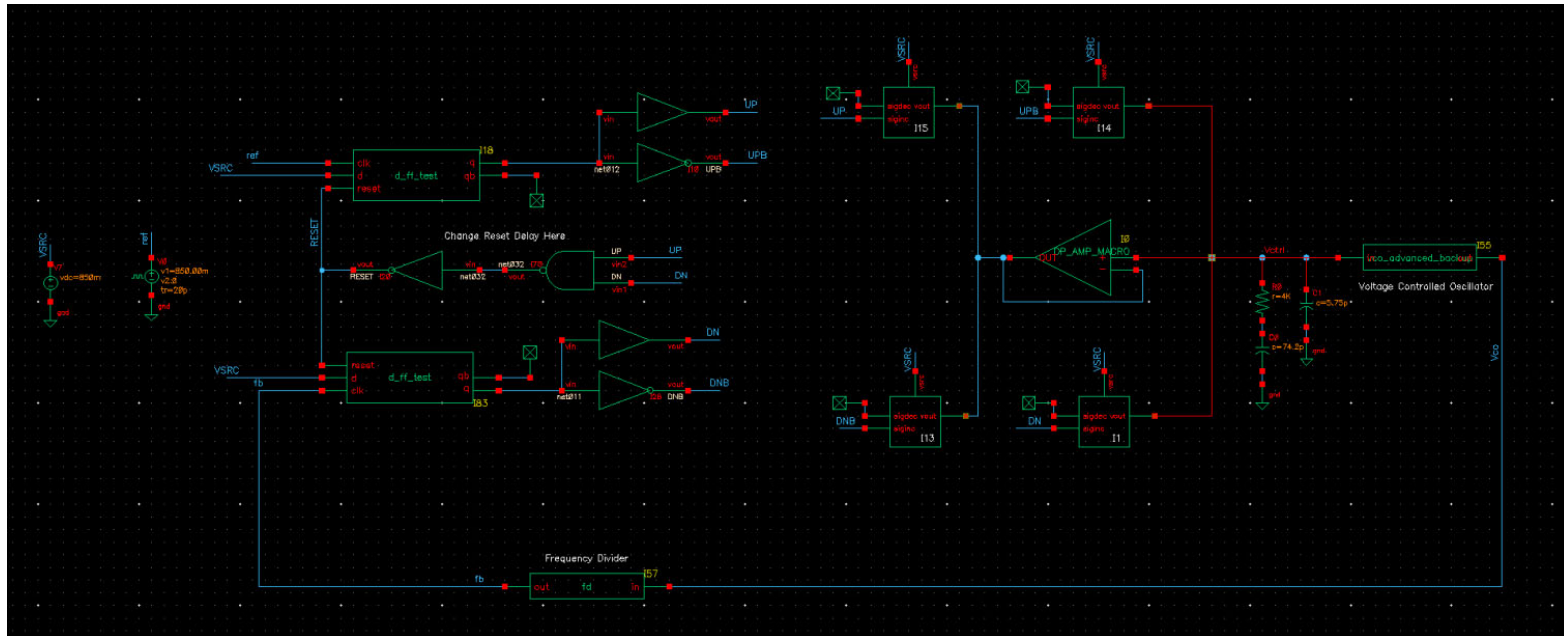
VCO (Square Wave)
Verilog-A Code Snippet

```
module vco_advanced_backup(in, out);
input in;
output out;
voltage in, out;
parameter real Vamp = 0.425;
parameter Fmax = 14.3125G;
parameter Fmin = 13.5625G;
//... (lines omitted)
real phase;
real ideal_phase;
real dPhase ;
//... (lines omitted)
analog begin
if(V(in)<Vmin) inst_freq = Fmin;
else if(V(in) > Vmax) inst_freq = Fmax;
else inst_freq = ((V(in)-Vmin)*(Fmax-Fmin)/(Vmax-Vmin)) + Fmin ;
ideal_phase = 2*`PI*idtmod(inst_freq, 0.0, 1.0, -0.5);
phase = ideal_phase + dPhase;
//... (lines omitted)
n = (phase >= -`PI/2)&&(phase < `PI/2);
end
V(out) <+ transition(n?Vamp:0,0,tran_time);
end
endmodule
```


$\Delta f_{out} = 500\,\text{MHz}$

55
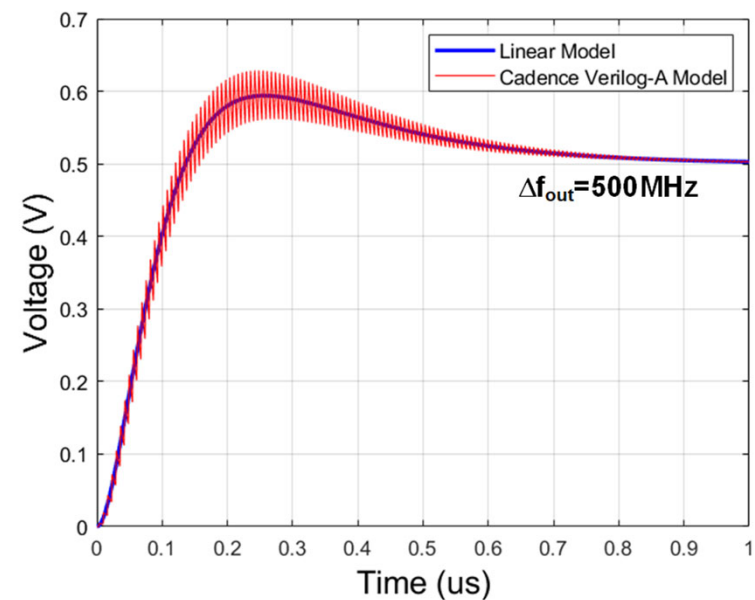
Next Time

- CDRs

- The following slides provide more details on PLL circuits. This 620 material may useful for the project, but won't be covered in detail on Exam 2.

PLL Loop Gain
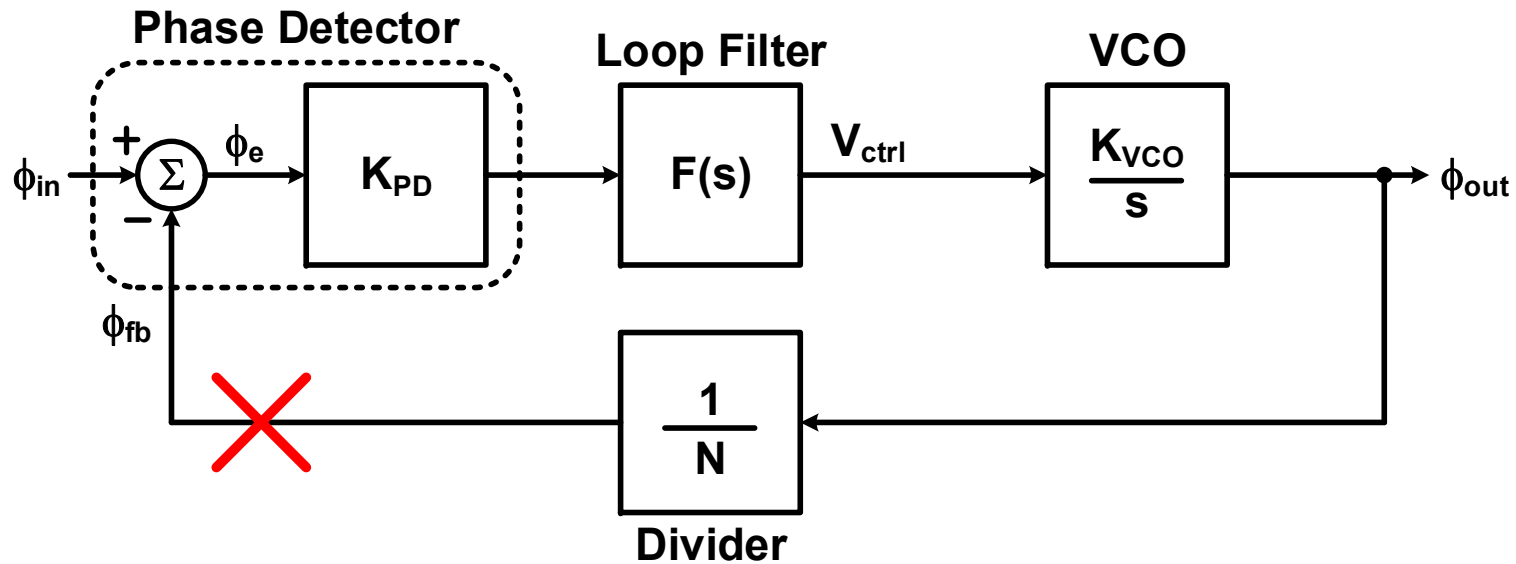
$$LG(s) = \frac{K_{PD}F(s)K_{VCO}}{Ns} = \frac{K_{PD}K_{VCO}\left(s + \frac{1}{R_1 C_1}\right)}{NC_2 s^2 \left(s + \frac{C_1 + C_2}{R_1 C_1 C_2}\right)}$$

$$\omega_z = \frac{1}{R_1 C_1}, \qquad \omega_{p1} = \omega_{p2} = 0, \qquad \omega_{p3} = \frac{C_1 + C_2}{R_1 C_1 C_2}$$

Loop Gain Response

$$LG(s) = \frac{K_{PD}K_{VCO}(s + \omega_z)}{NC_2 s^2(s + \omega_{p3})}$$
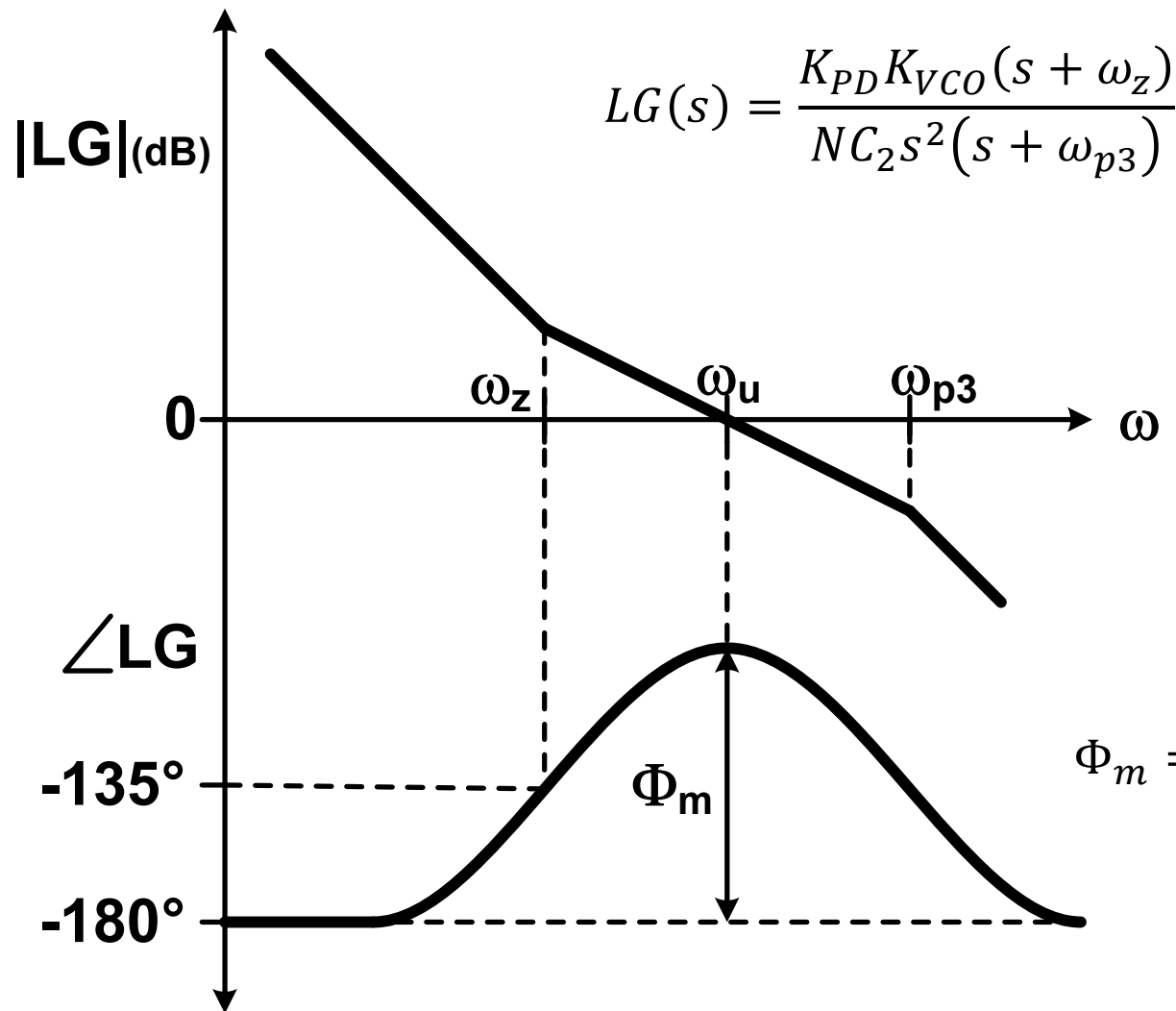
$$\omega_{p1} = \omega_{p2} = 0$$

$$\omega_z = \frac{1}{R_1 C_1}$$

$$\omega_{p3} = \frac{C_1 + C_2}{R_1 C_1 C_2}$$

$$\Phi_m = \tan^{-1}\left(\frac{\omega_u}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_u}{\omega_{p3}}\right)$$

Design Procedure for Max Φ_m

$$LG(s) = \frac{K_{PD}K_{VCO}(s + \omega_z)}{NC_2 s^2 (s + \omega_{p3})}$$
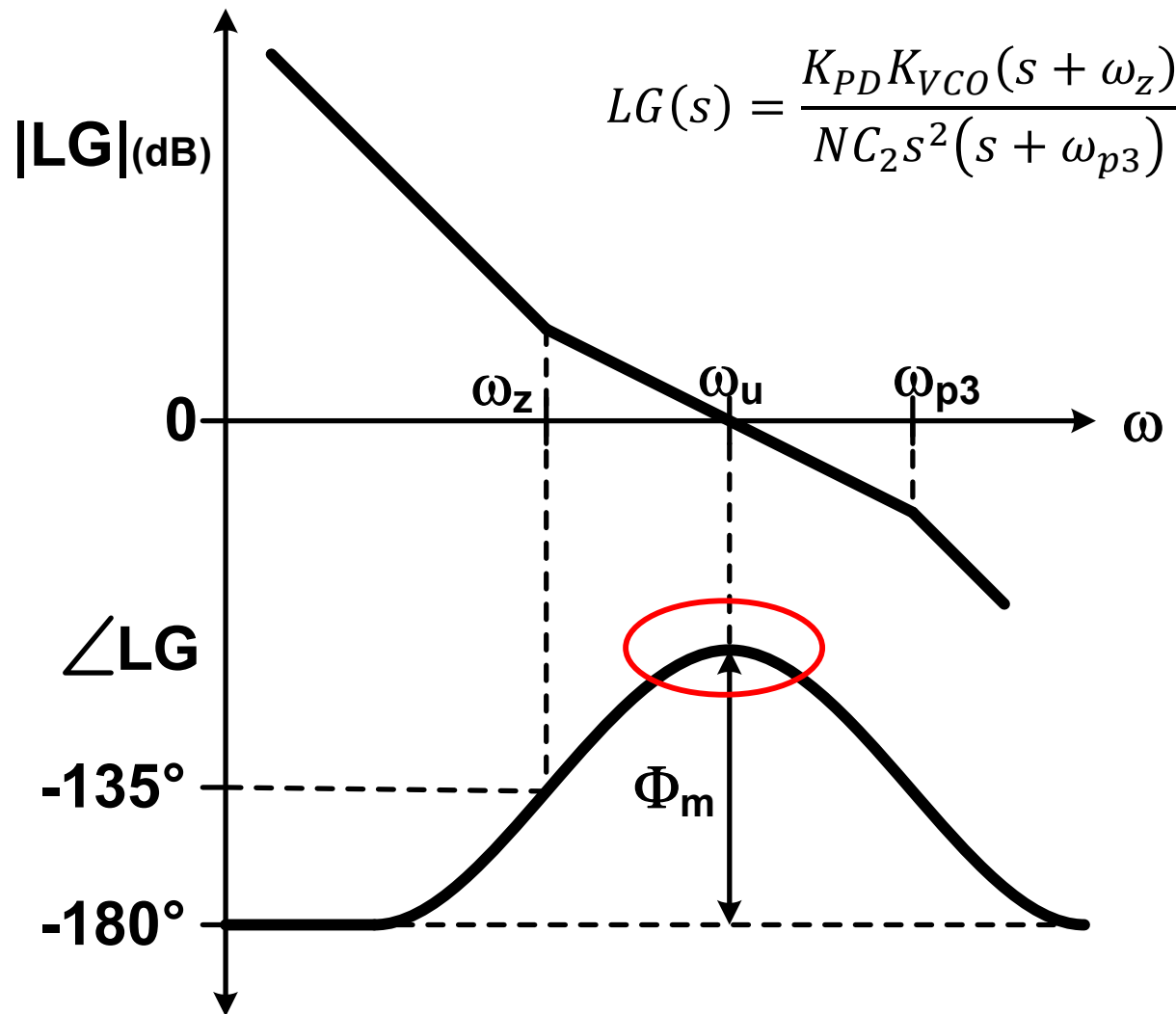
PLL Specs

Parameter	
Fref	156.25MHz
N	90
Fvco	14GHz
f_u	**2MHz**
Φ_m	**60°**
Kvco	2π*1GHz/V
R	??
C_1	??
C_2	??
I_{cp}	??

- Design procedure maximizes phase margin for a given f_u and Φ_m specification [Hanumolu TCAS1 2004]

Design Procedure for Max Φ_m

1. Set loop filter capacitor ratio based on Φ_m

$$K_C = \frac{C_1}{C_2} = 2\left(tan^2(\Phi_m) + tan(\Phi_m)\sqrt{tan^2(\Phi_m) + 1}\right)$$

$$\Phi_m = 60° \rightarrow K_C = 12.9$$

2. Set loop filter values based on ω_u & with R set for low noise

$$\omega_z = \frac{\omega_u}{\sqrt{1 + K_C}}$$

$$C_1 = \frac{1}{\omega_z R}, \quad C_2 = \frac{C_1}{K_C}$$

$$\omega_u = 2\pi * 2MHz \rightarrow \omega_z = 2\pi * 536kHz$$

$$\text{Set } R = 4k\Omega \rightarrow C_1 = 74pF \quad \& \quad C_2 = 5.8pF$$

3. Set I_{cp} to achieve required loop gain

$$I_{cp} = \frac{NC_2\omega_u^2}{K_{VCO}}\sqrt{\frac{\omega_{p3}^2 + \omega_u^2}{\omega_z^2 + \omega_u^2}}$$

$$\omega_{p3} = 2\pi * 7.45MHz \rightarrow I_{cp} = 310\mu A$$

Simulated Responses

$$LG(s) = \frac{K_{PD}K_{VCO}(s + \omega_z)}{NC_2 s^2 (s + \omega_{p3})}$$
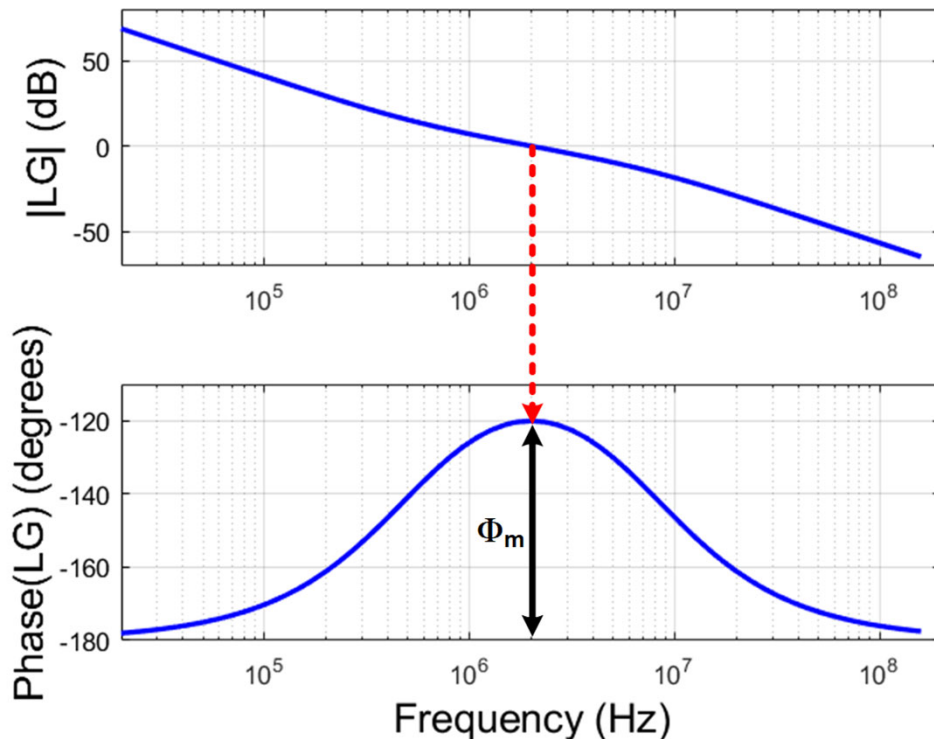
$$\frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{\frac{K_{PD}K_{VCO}}{C_2}\left(s + \frac{1}{RC_1}\right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1 C_2}\right)s^2 + \left(\frac{K_{PD}K_{VCO}}{NC_2}\right)s + \frac{K_{PD}K_{VCO}}{NRC_1 C_2}}$$
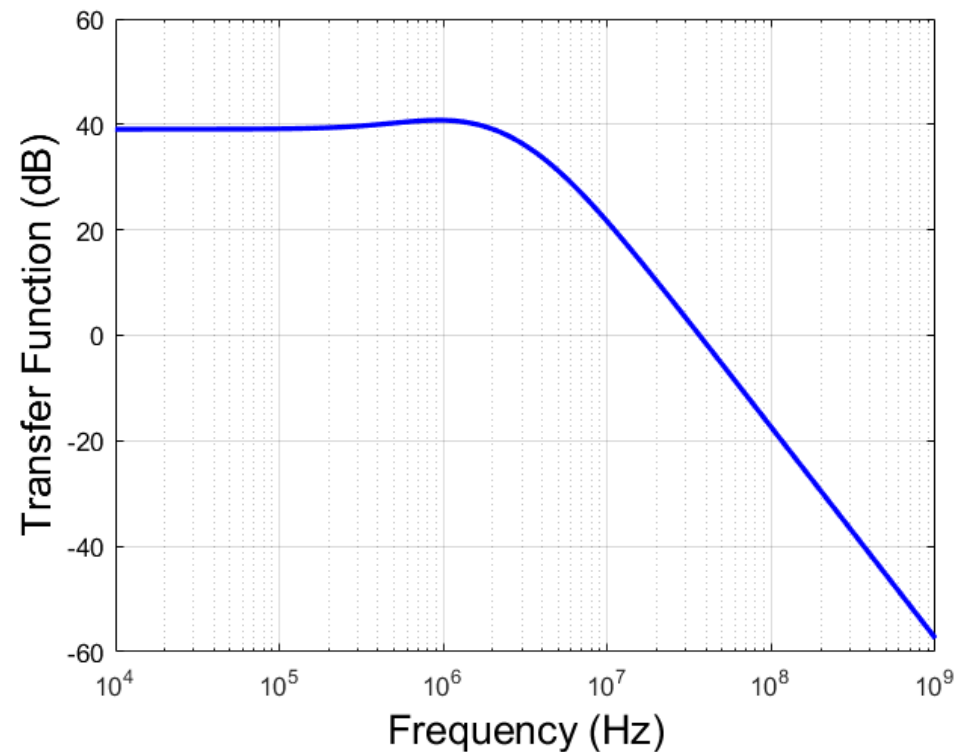
- Design achieves f_u=2MHz and Φ_m=60°
- Closed loop response has f_{3dB}=3.1MHz

61

Charge-Pump PLL Circuits

- **Phase Detector**

- Charge-Pump

- Loop Filter

- VCO

- Divider
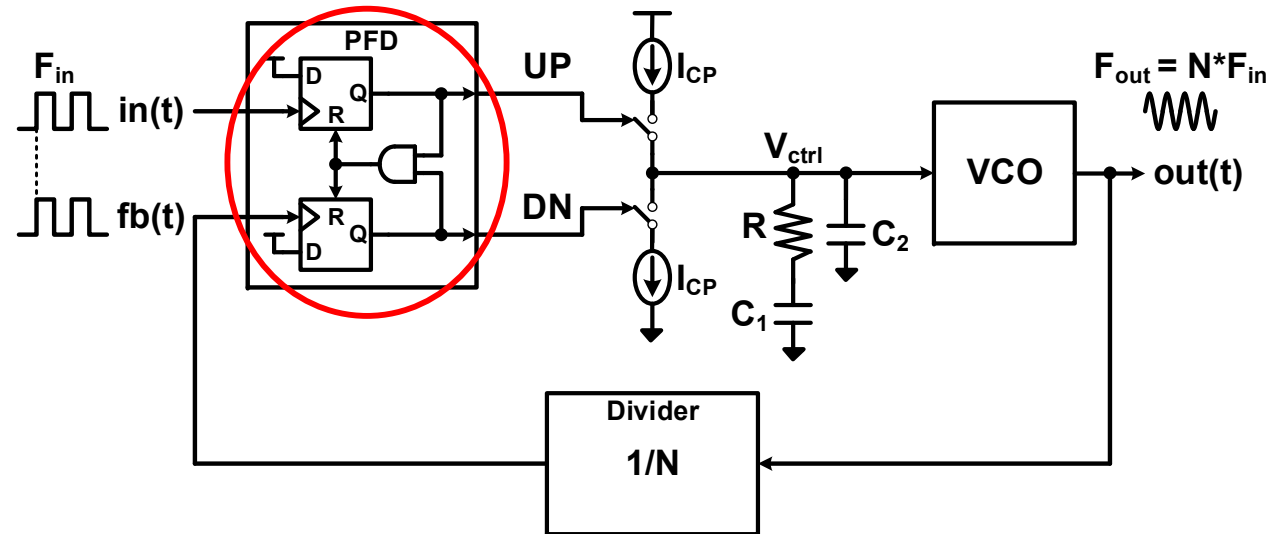
Phase Detector
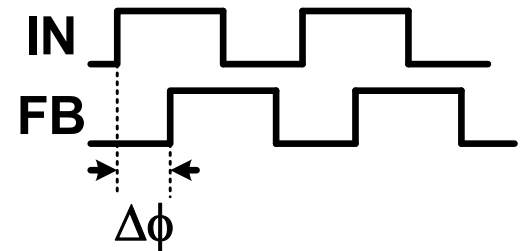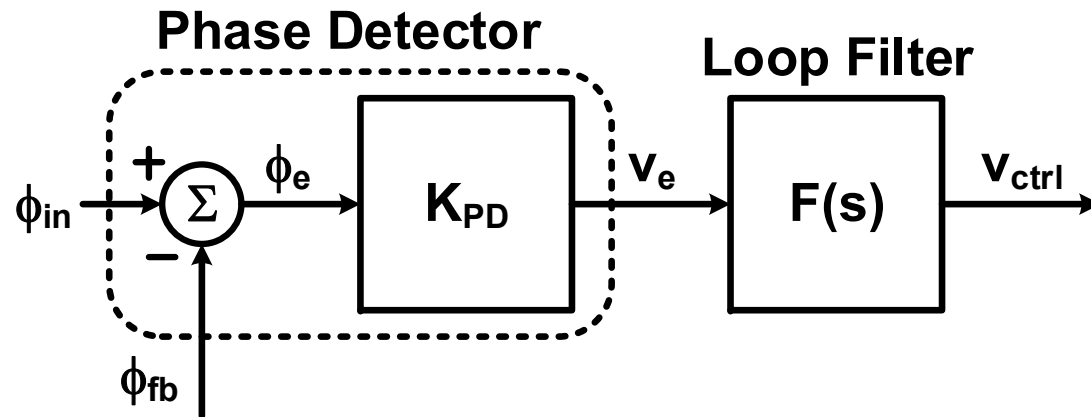
avg$\{v_e(t)\} = K_{PD}\Delta\phi$

- Detects phase difference between feedback clock and reference clock
- The loop filter will filter the phase detector output, thus to characterize phase detector gain, extract average output voltage
- The K_{PD} factor can change depending on the specific phase detector circuit
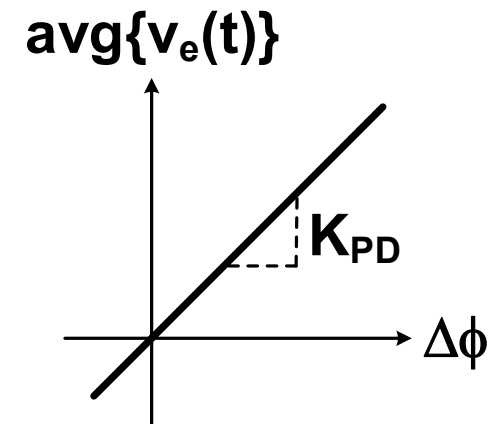
K_{PD} units are V/rad when used with a dimension-less filter

K_{PD} units are rad^{-1} (averaged) or A/rad when combined with the charge-pump

when used with a impedance filter

Analog Multiplier Phase Detector

$A_1 \cos \omega_1 t$

$A_2 \cos(\omega_2 t + \Delta\phi)$

$$\frac{\alpha A_1 A_2}{2} \cos[(\omega_1 + \omega_2)t + \Delta\phi] + \frac{\alpha A_1 A_2}{2} \cos[(\omega_1 - \omega_2)t - \Delta\phi]$$

α is mixer gain
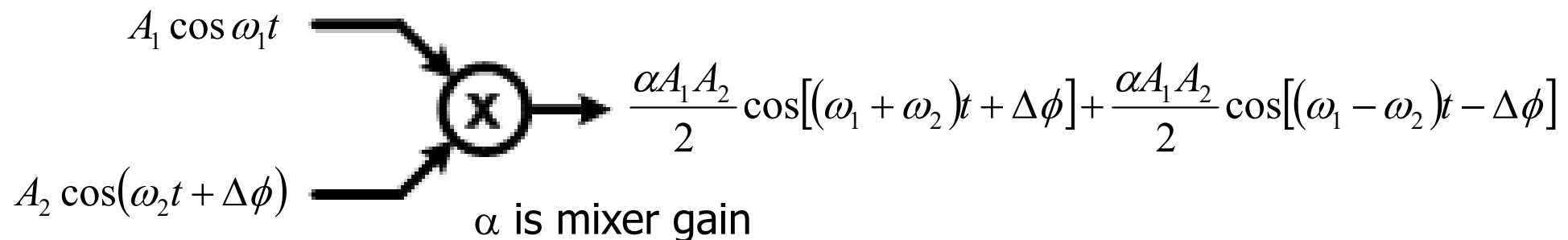
- If $\omega_1 = \omega_2$ and filtering out high-frequency term

$$\overline{y(t)} = \frac{\alpha A_1 A_2}{2} \cos \Delta\phi$$

- Near $\Delta\phi$ lock region of $\pi/2$: $\overline{y(t)} \approx \frac{\alpha A_1 A_2}{2}\left(\frac{\pi}{2} - \Delta\phi\right)$

$$K_{PD} = -\frac{\alpha A_1 A_2}{2}$$
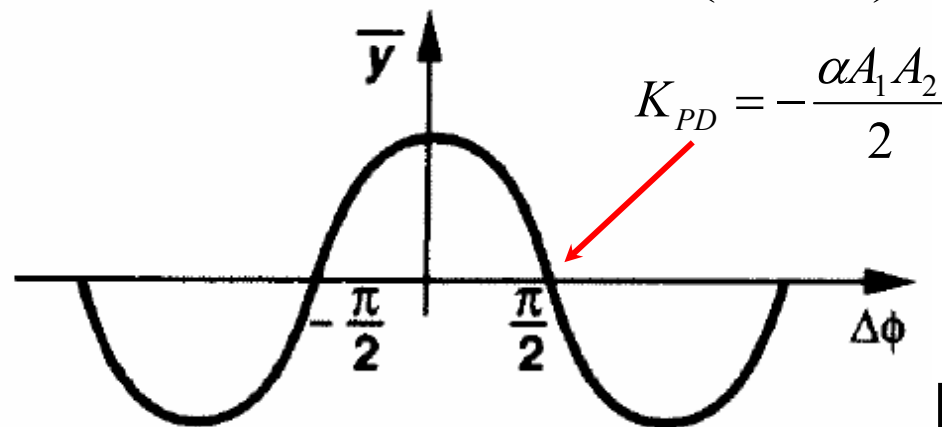
[**Razavi**]

XOR Phase Detector
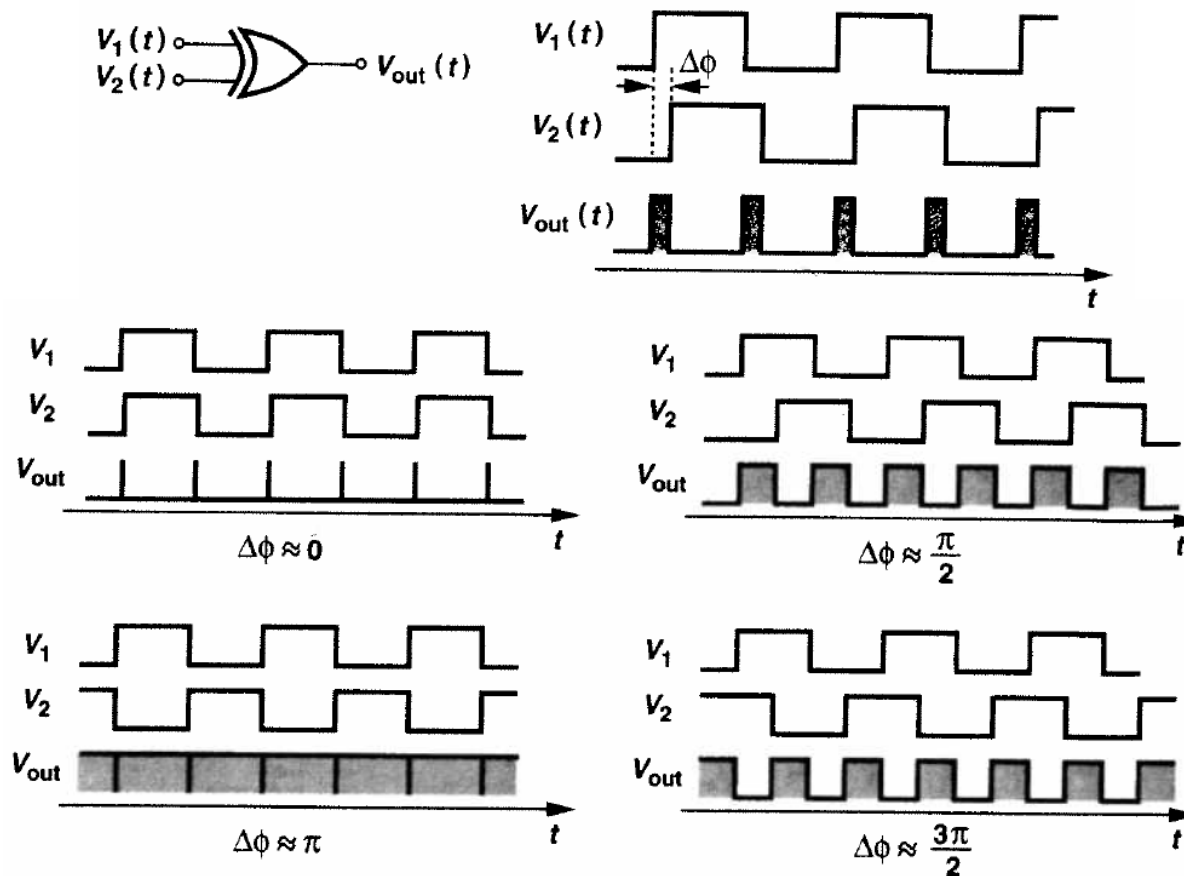
[**Razavi**]

- Assuming logic 1="+1" and 0="-1", the XOR PD will lock when the average output is 0
  - Generally, $\pi/2$ is a stable lock point and $-\pi/2$ is a metastable point
- Sensitive to clock duty cycle

XOR Phase Detector

$$-\pi < \Phi_{ref} - \Phi_{div} < 0$$

T/2

ref(t)

div(t)

e(t)

W

$$W = -\left(\frac{\Phi_{ref} - \Phi_{div}}{\pi}\right)T/2$$

$$0 < \Phi_{ref} - \Phi_{div} < \pi$$

T/2

ref(t)

div(t)

e(t)

W

$$W = \left(\frac{\Phi_{ref} - \Phi_{div}}{\pi}\right)T/2$$
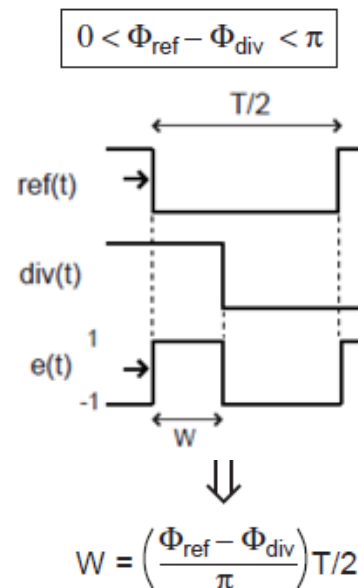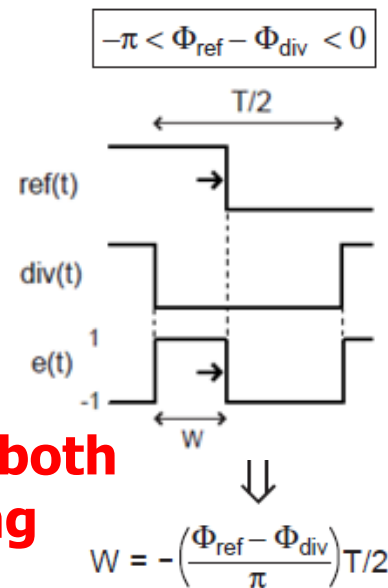
Width is same for both leading and lagging phase difference!

[**Perrott**]

avg{e(t)}

gain = -2/π

gain = 2/π

1

$$-\pi \quad -\pi/2 \quad 0 \quad \pi/2 \quad \pi$$

$$\Phi_{ref} - \Phi_{div}$$

-1

phase detector
range = π
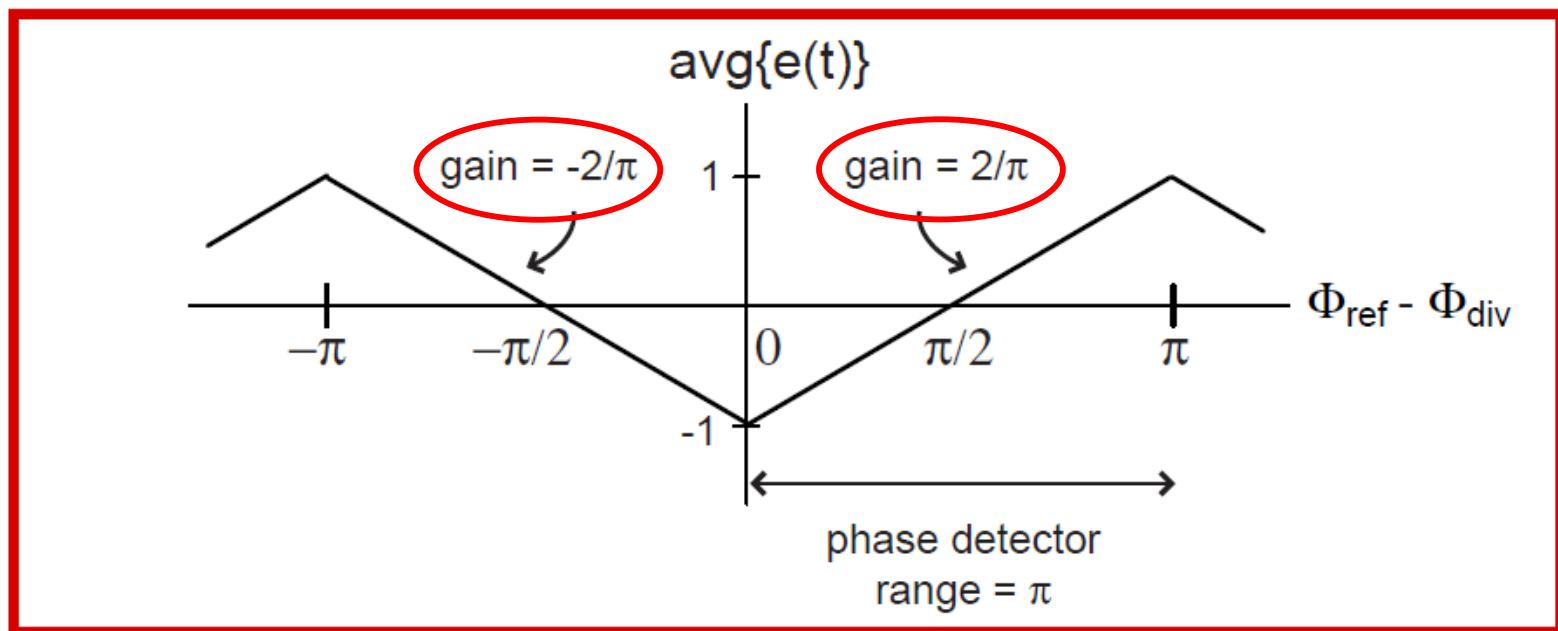
Cycle Slipping

- If there is a frequency difference between the input reference and PLL feedback signals the phase detector can jump between regions of different gain
  - PLL is no longer acting as a linear system

avg{e(t)}

gain = -2/π   1   gain = 2/π   [**Perrott**]

$-\pi$ $-\pi/2$ 0 $\pi/2$ π $\Phi_{ref} - \Phi_{div}$

-1

phase detector
range = π

(positive feedback operation)   (negative feedback operation)

Cycle Slipping

Synthesizer Response To Divider Step
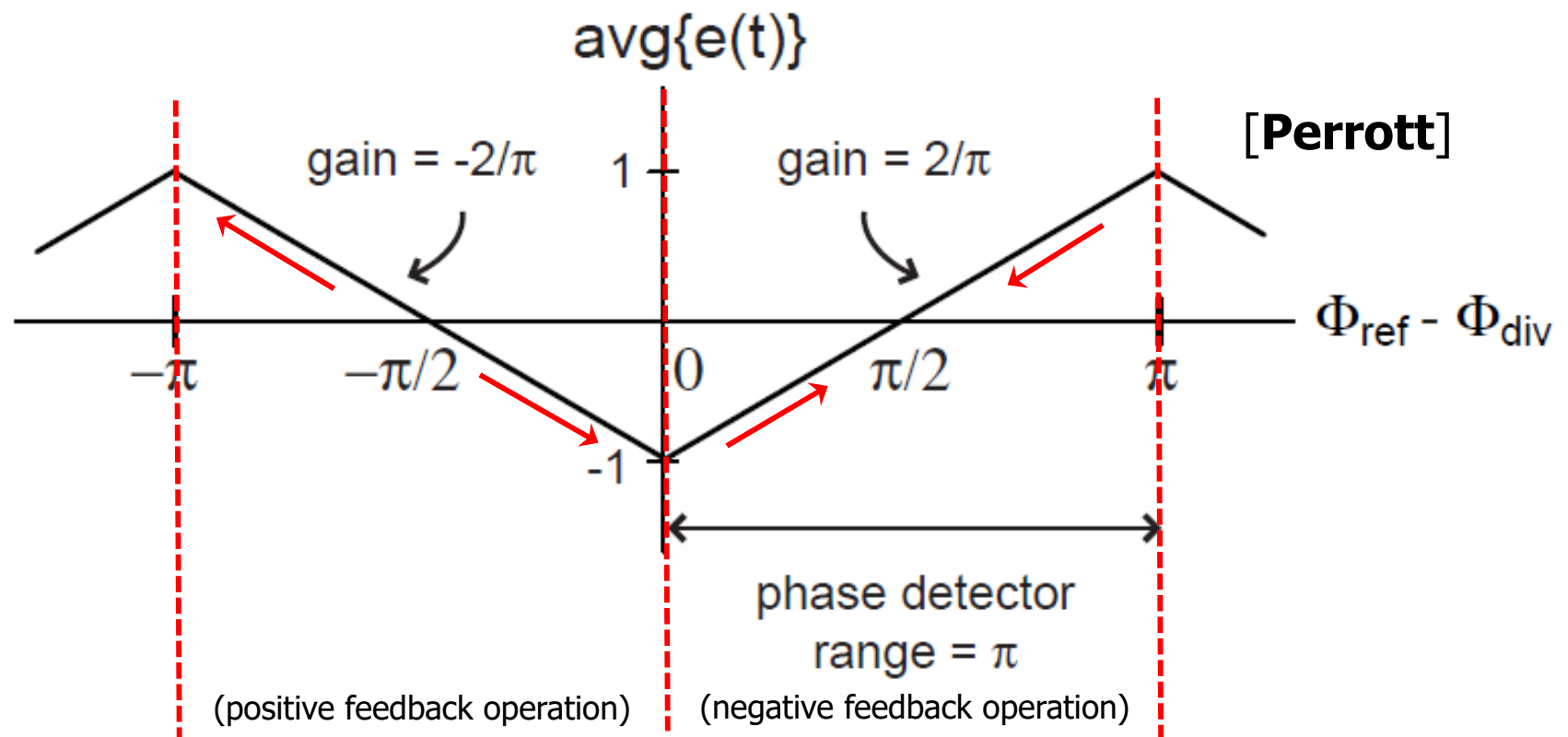
Cycle Slipping
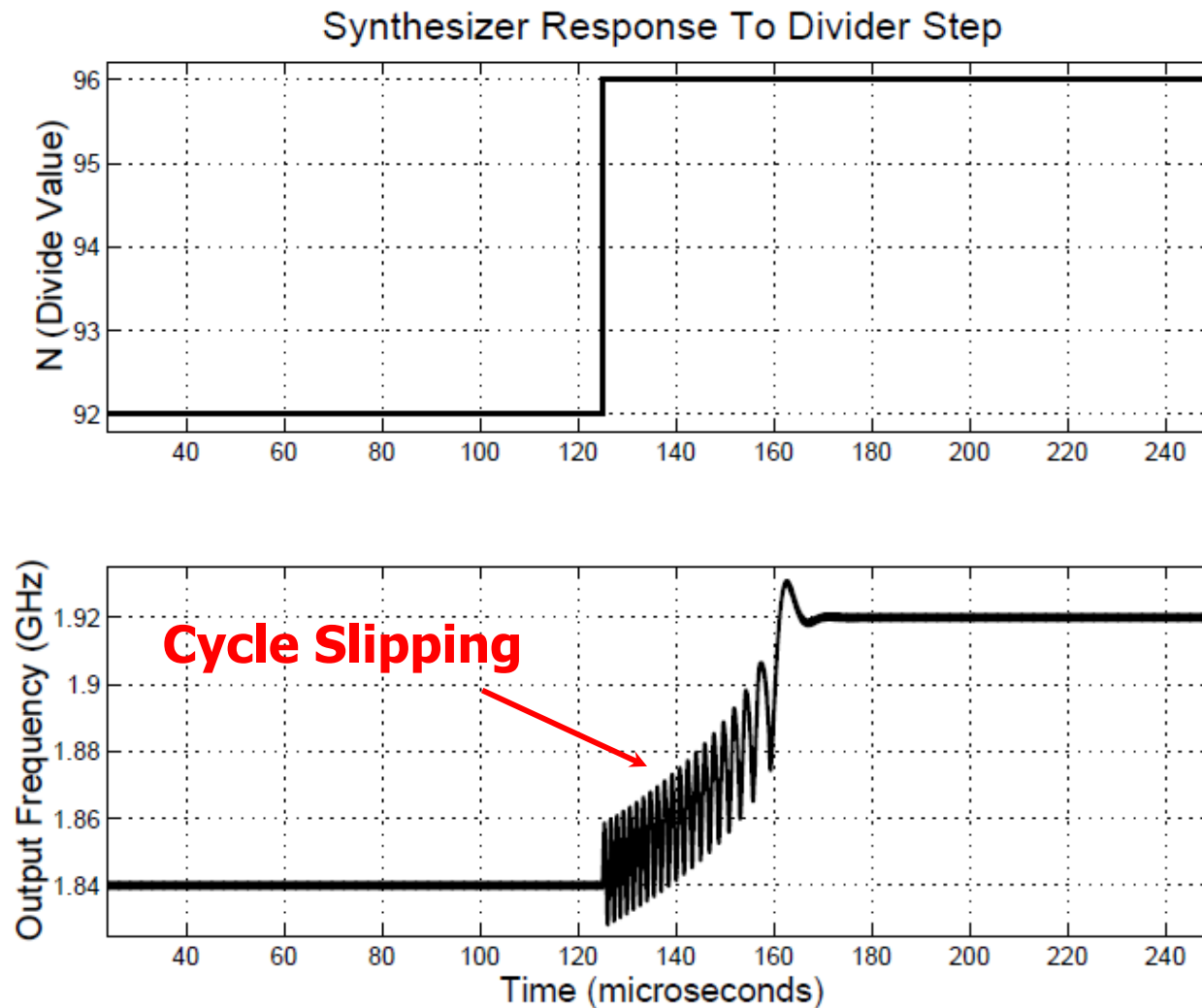
[**Perrott**]

- If frequency difference is too large the PLL may not lock

Phase Frequency Detector (PFD)

- Phase Frequency Detector allows for wide frequency locking range, potentially entire VCO tuning range
- 3-stage operation w/ UP & DN outputs
- Rising edge-triggered results in duty cycle insensitivity
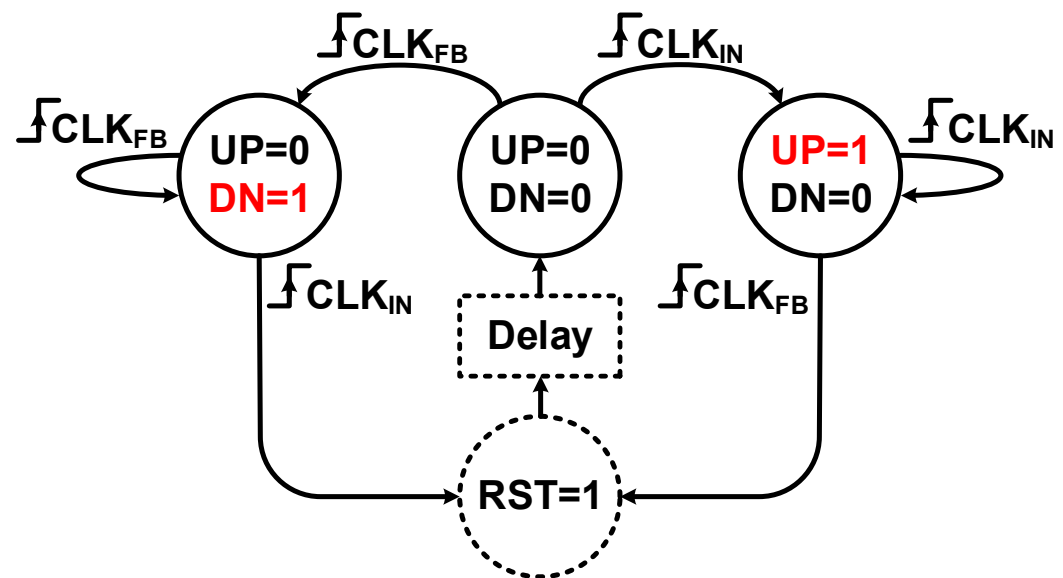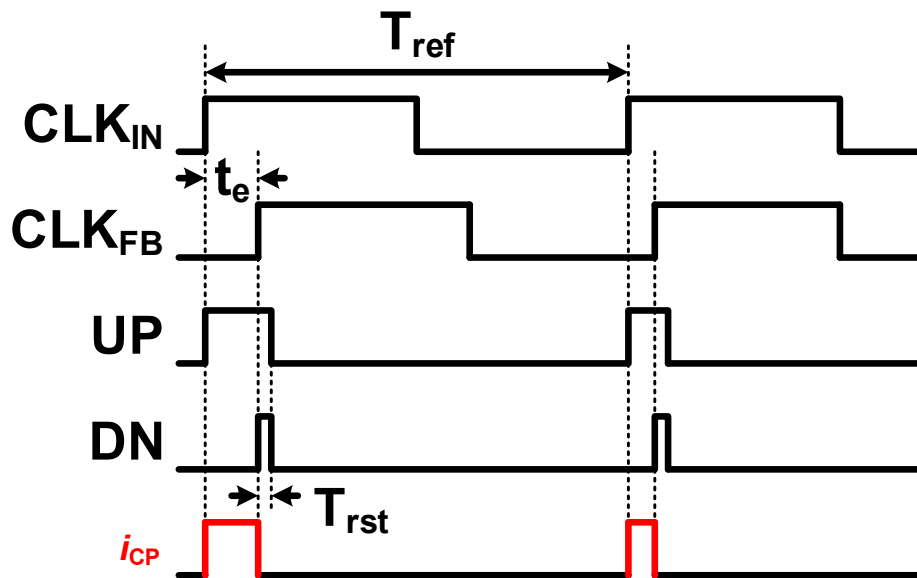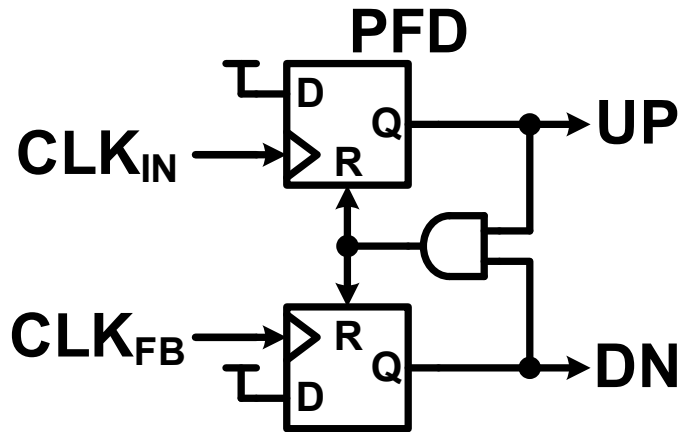
Averaged PFD Transfer Characteristic

UP=1 & DN=-1
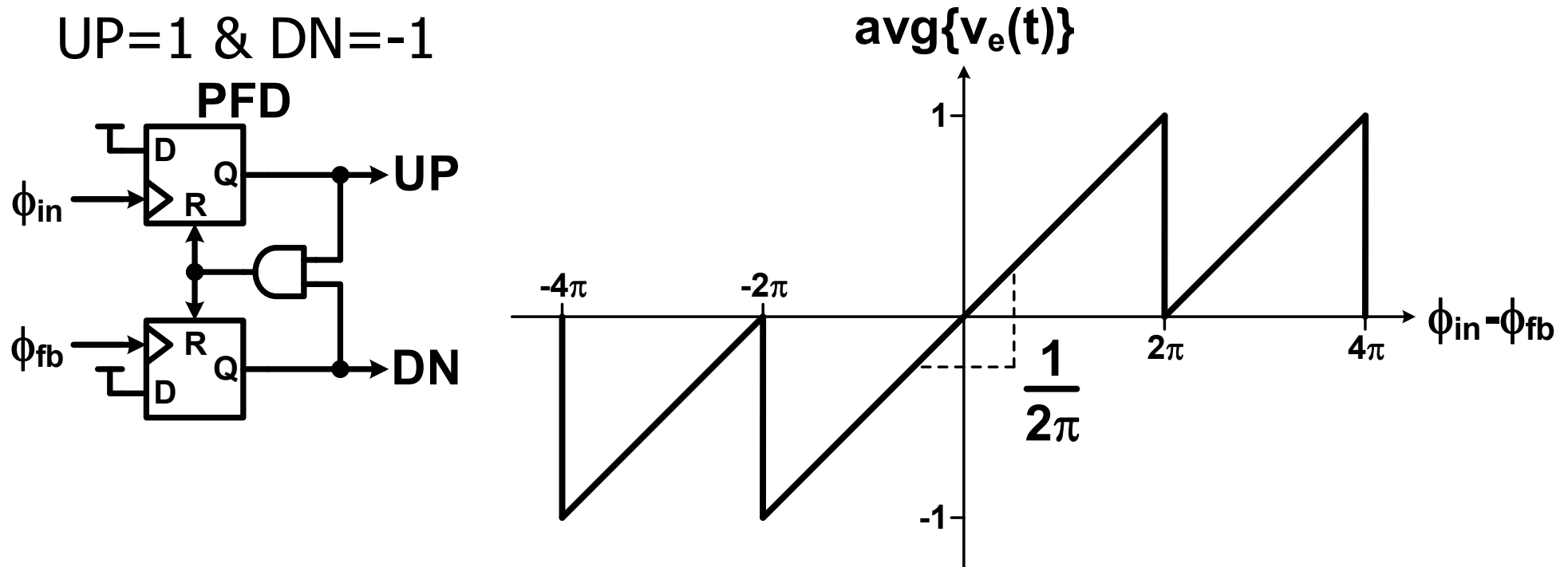
- Constant slope and polarity asymmetry about zero phase allows for wide frequency range operation

- The averaged PFD gain is $1/(2\pi)$ with units of rad^{-1}

Phase Detector
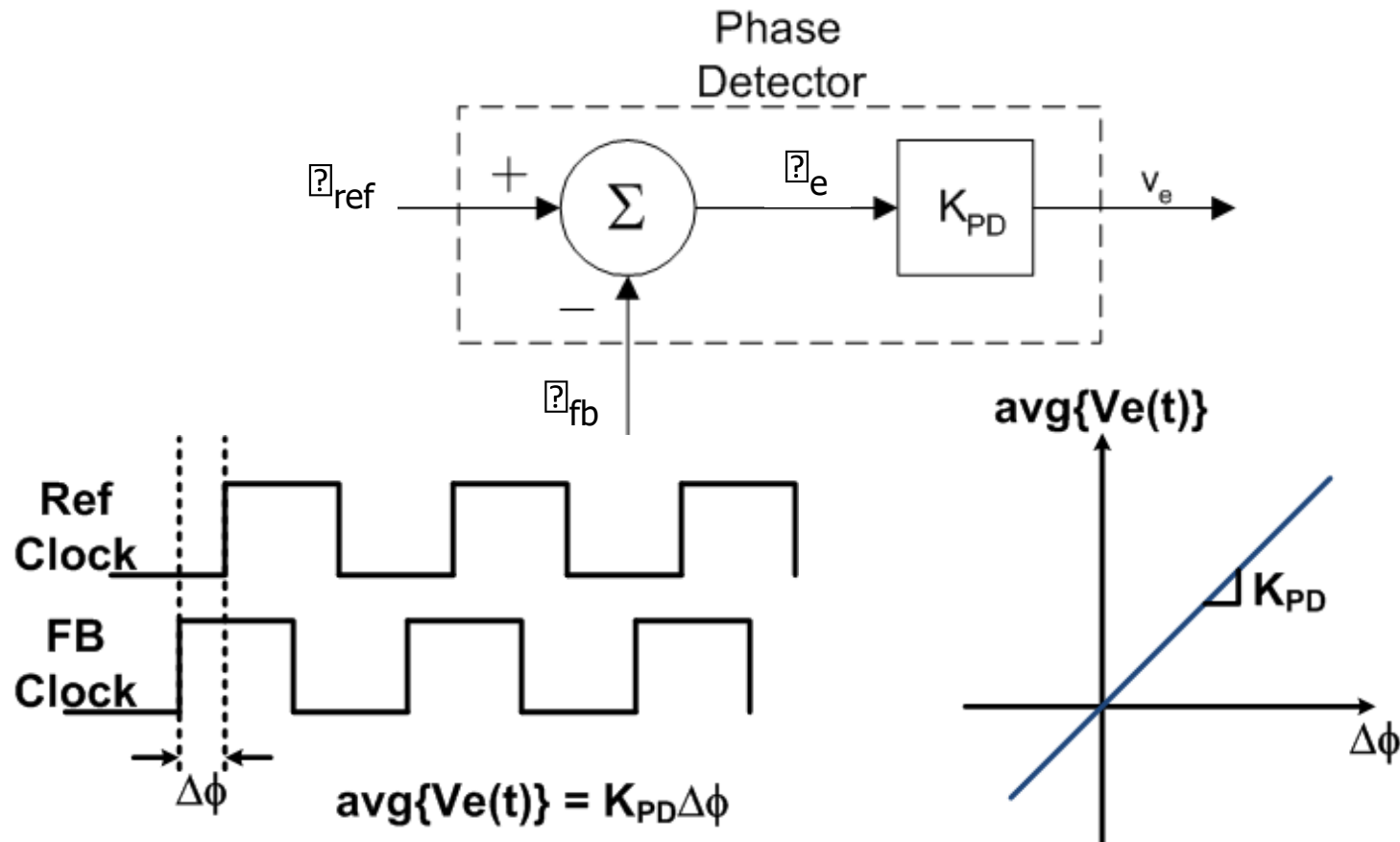
- Detects phase difference between feedback clock and reference clock
- The loop filter will filter the phase detector output, thus to characterize phase detector gain, extract average output voltage (or current for charge-pump PLLs)

PFD Deadzone
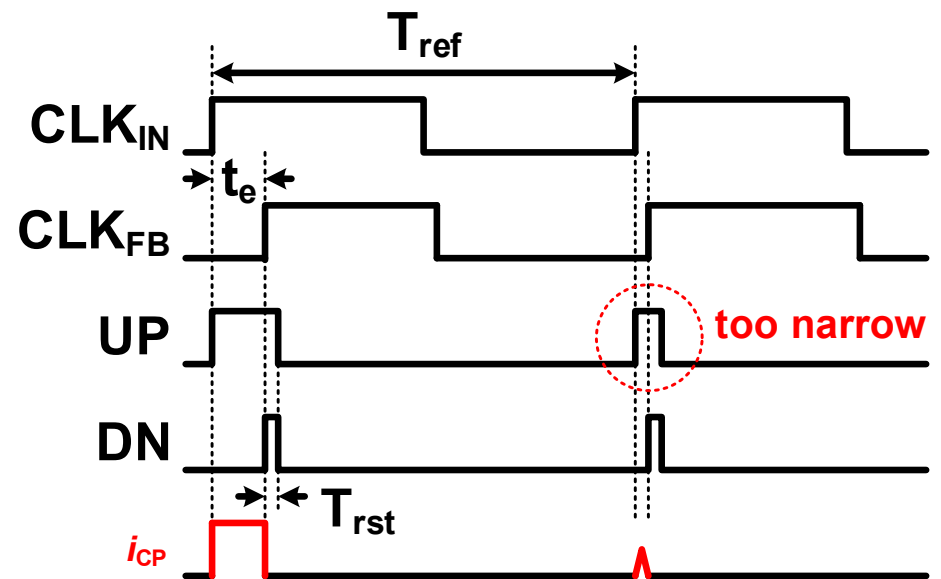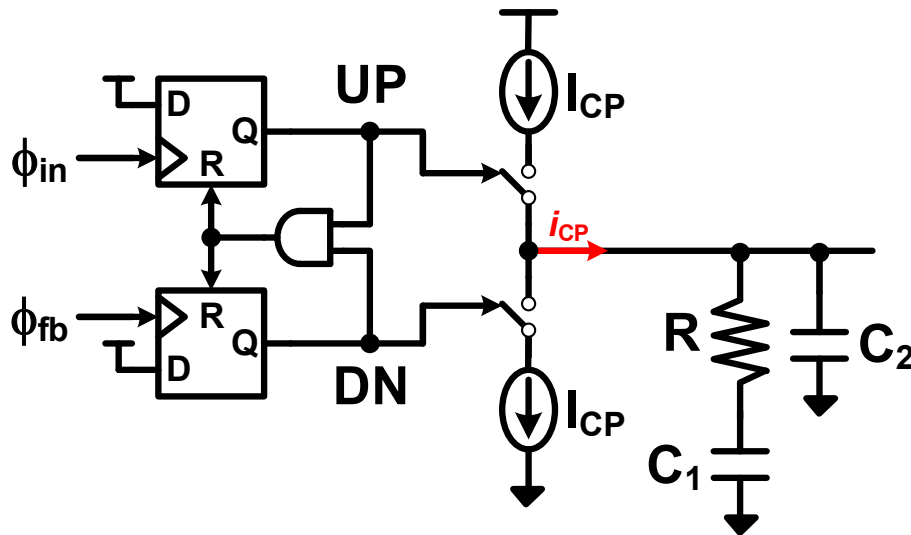
- If phase error is small, then short output pulses are produced by PFD
- Cannot effectively propagate these pulses to switch charge pump
- Results in phase detector "dead zone" which causes low loop gain and increased jitter
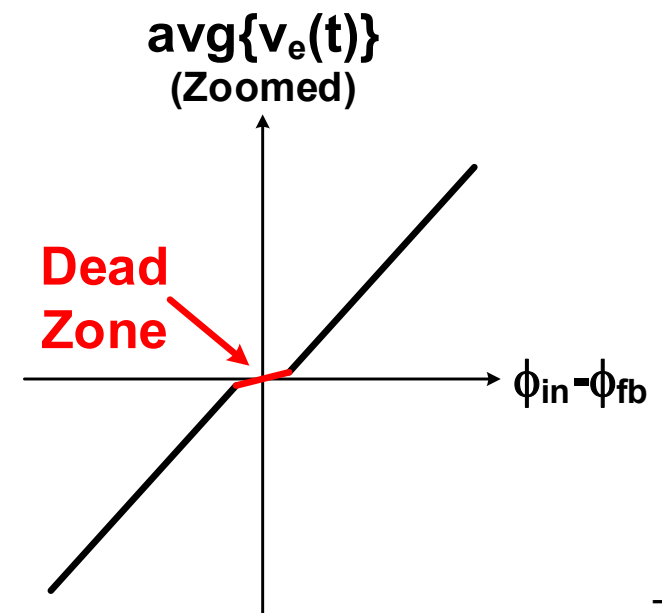
PFD Operation w/ Reset Delay

- Solution is to add delay in PFD reset path to force a minimum UP and DN pulse length

- In locked state both UP and DN current sources are on for T_{rst}, but ideally no net current is delivered to loop filter

Problems Near 2π

- PFD cannot react to input rising edges during reset

- This can result in the next rising edge driving the loop in the wrong direction

- Reset delay can increase acquisition time and sets a max PFD operating frequency

PFD Transfer Characteristic w/ Reset Delay
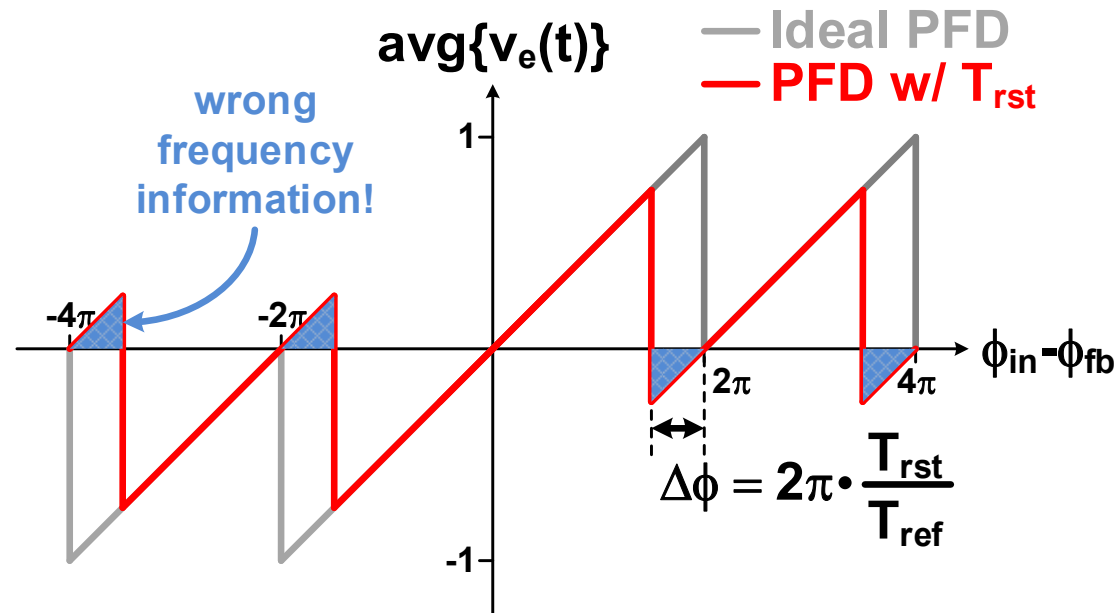
- PFD reset delay generates wrong frequency information
- If this becomes a large percentage of the reference cycle, then the PFD can fail to acquire frequency lock

$$\text{Max } T_{rst} = \frac{T_{ref}}{2}$$

$$\boxed{\text{Max PFD Frequency} = \frac{1}{2T_{rst}}}$$

Charge-Pump PLL Circuits

- Phase Detector

- Charge-Pump

- Loop Filter

- VCO

- Divider
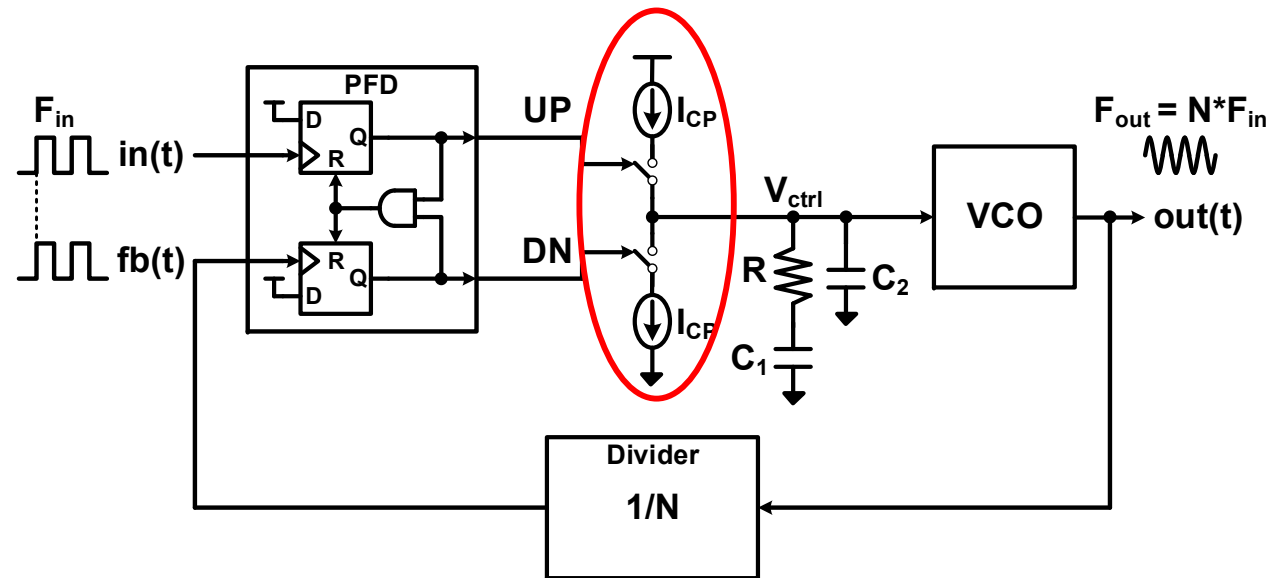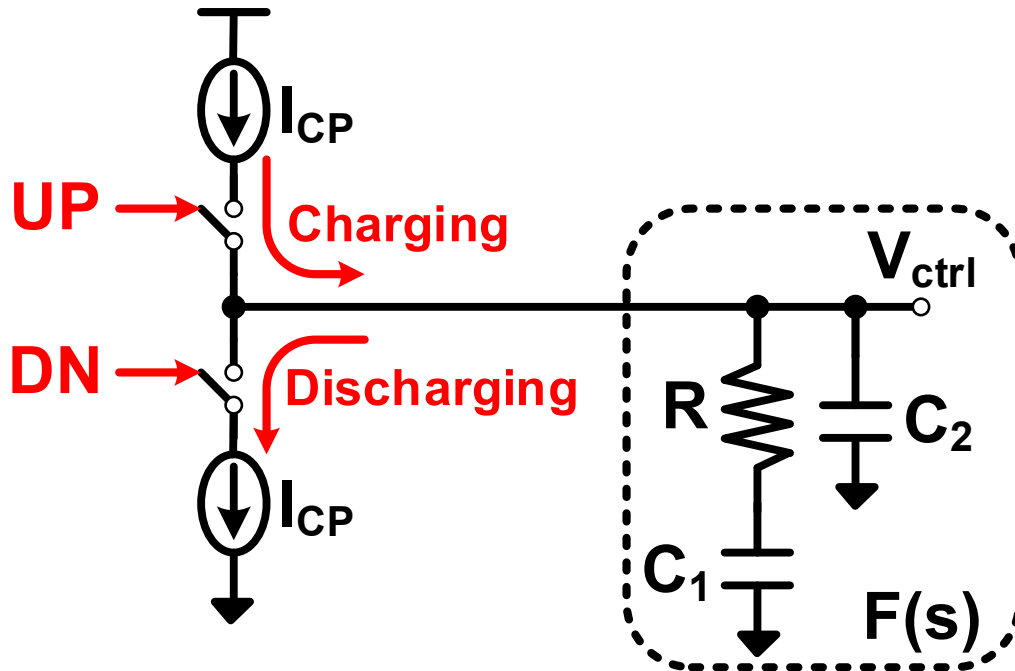
Charge Pump

- Converts PFD output signals to charge

- Charge is proportional to PFD pulse widths

$$\text{Un - Averaged Charge - Pump Gain} = I_{CP} \; (\text{Amps})$$

$$\text{Averaged Charge - Pump Gain} = \frac{I_{CP}}{2\pi} \left(\frac{\text{Amps}}{\text{rad}} \right)$$

$$\text{Total PFD \& Charge - Pump Gain} = \frac{I_{CP}}{2\pi} \left(\frac{\text{Amps}}{\text{rad}} \right)$$

This gain can vary if a different phase detector is used

Simple Charge Pump
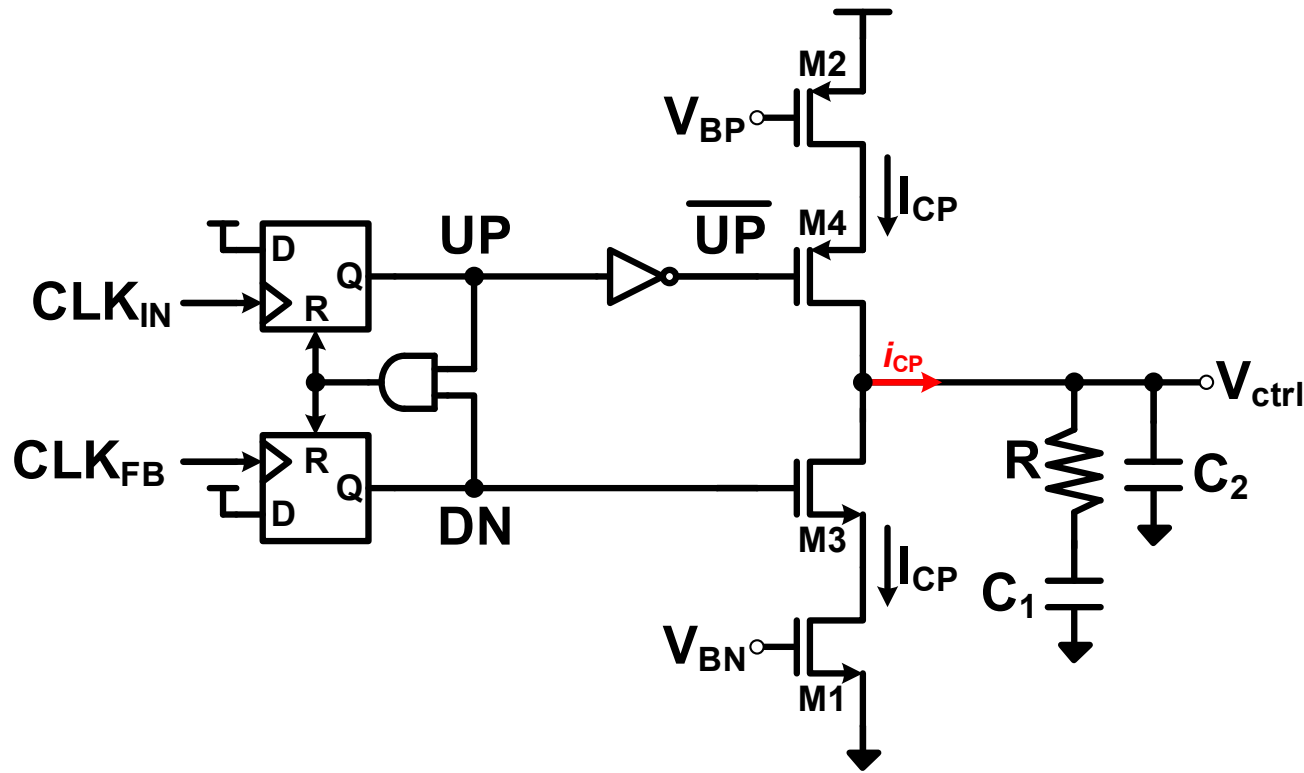
- Issues
  - Skew between UPB and DN control signals
  - Matching of UP/DN current sources
  - Clock feedthrough and charge injection from switches onto V_{ctrl}
  - Charge sharing between current source drain nodes' capacitance and V_{ctrl}

Simple Charge Pump Skew Compensation

T-gate
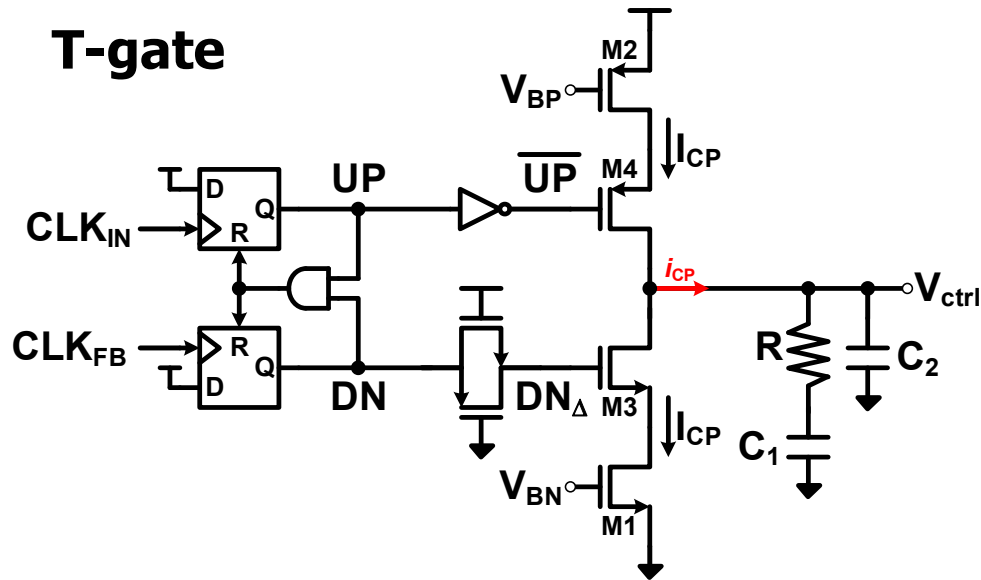
- Adding a transmission gate in the DN signal path helps to equalize the delay with the UPB signal for better overlap between the UP and DN current sources
- Poor matching of UPB and DN_Δ edge rates

3/2 Inverter Path
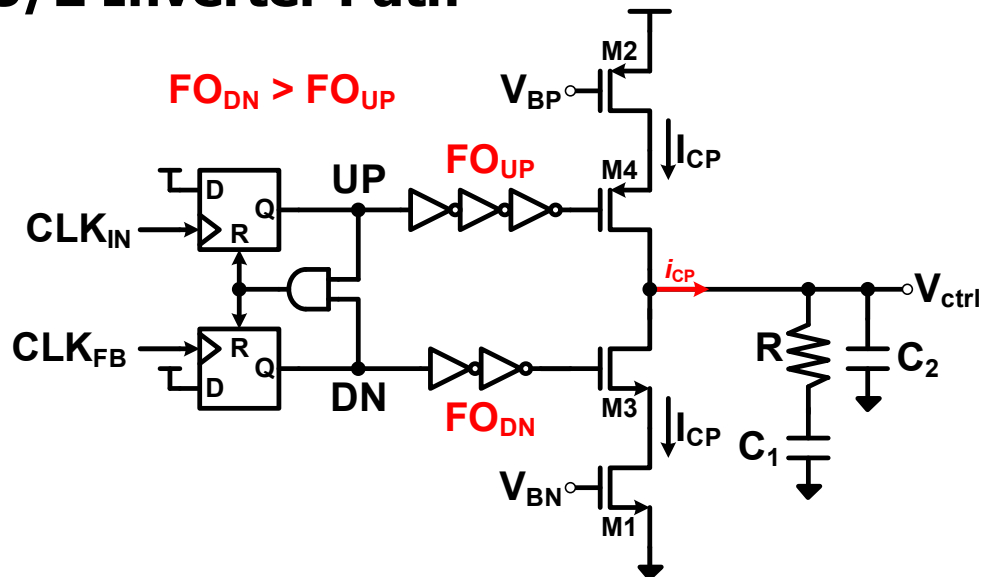
- Utilizing a 3-inverter UP path and a 2-inverter DN path with a higher fanout provides good matching of both delay and edge rates

Charge Pump Mismatch
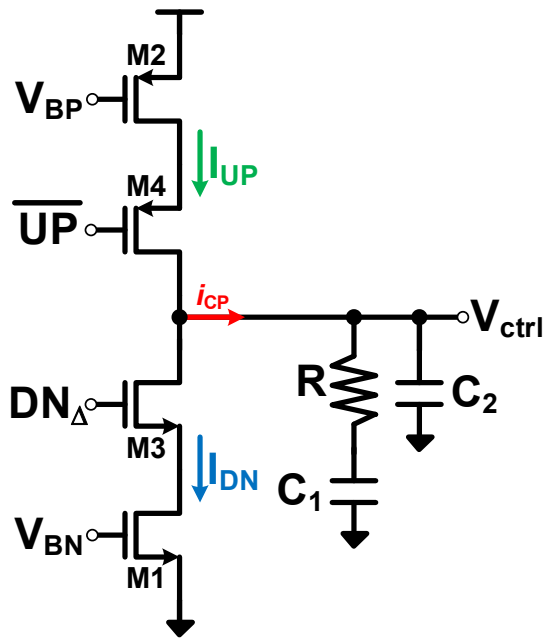
Ideal locked condition, but CP mismatch
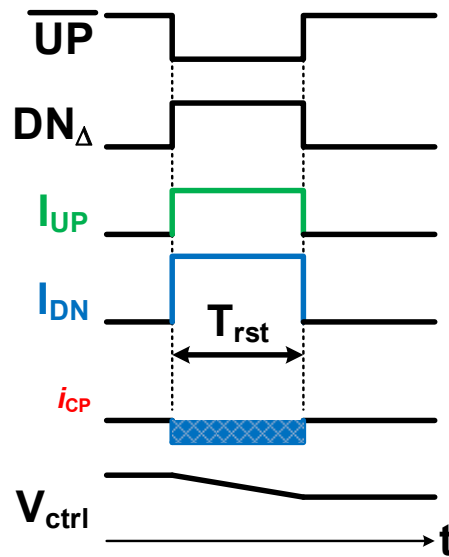
Actual locked condition w/ CP mismatch
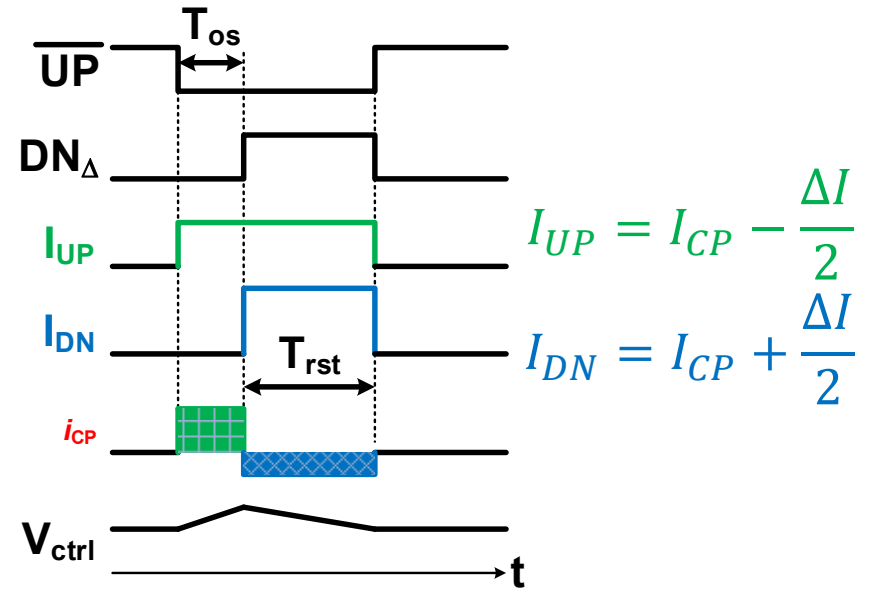
$$I_{UP} = I_{CP} - \frac{\Delta I}{2}$$

$$I_{DN} = I_{CP} + \frac{\Delta I}{2}$$

- PLL will lock with static phase error if there is a charge pump mismatch
- Extra "ripple" on V_{ctrl}
  - Results in frequency domain spurs at the reference clock frequency offset from the carrier

$$I_{UP}(T_{os}) = \Delta I(T_{rst})$$

$$T_{os} = \frac{\Delta I(T_{rst})}{I_{CP} - \frac{\Delta I}{2}}$$

$$\phi_{os} = 2\pi \left(\frac{\Delta I}{I_{CP} - \frac{\Delta I}{2}} \right) \left(\frac{T_{rst}}{T_{ref}} \right)$$

Charge Pump w/ Improved Matching
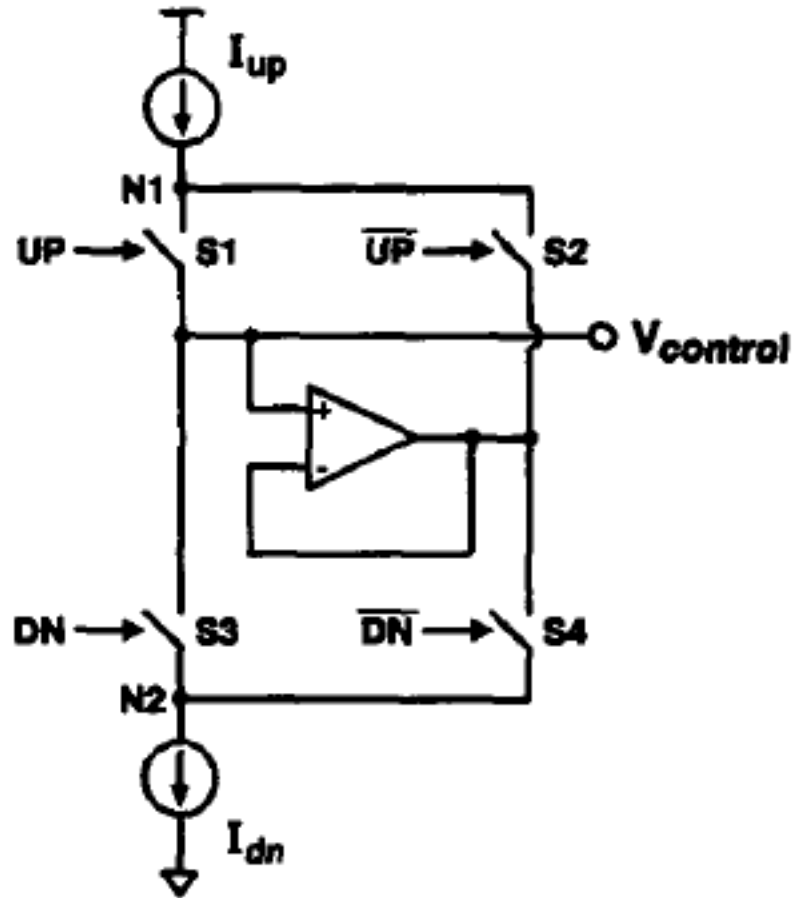
[**Young JSSC 1992**]

- Parallel path keeps current sources always on

- Amplifier keeps current source V_{DS} voltages constant resulting in reduced transient current mismatch (charge sharing)
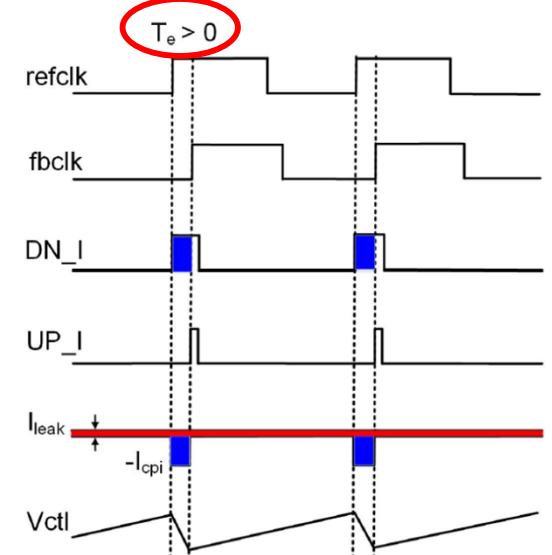
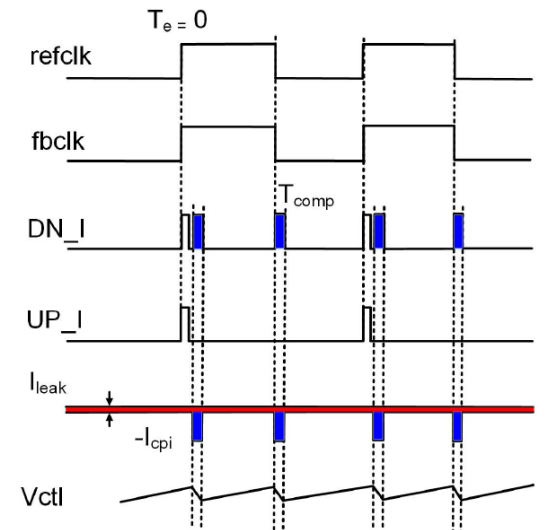# Digital Leakage Compensation

- Charge pump **off-state leakage** causes PLL to lock with static phase error

- Compensated by additional digitally-controlled charge pump current pulses

- TDC detects phase error between input reference clock and feedback clock
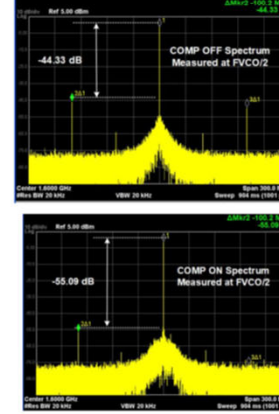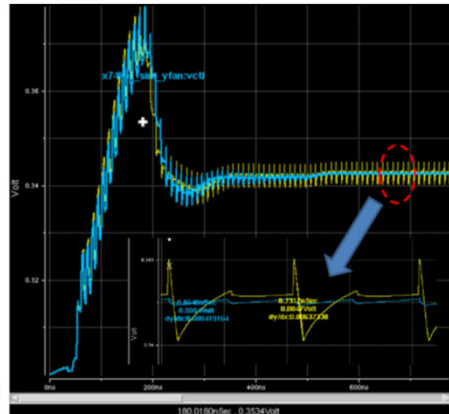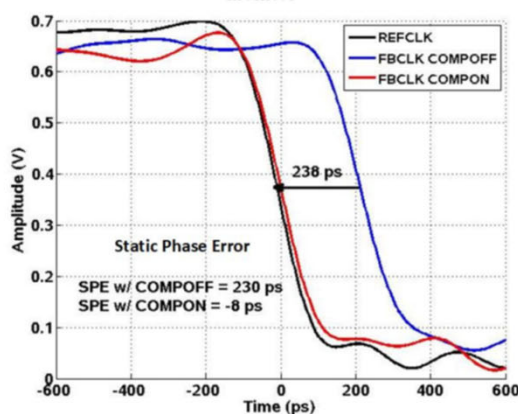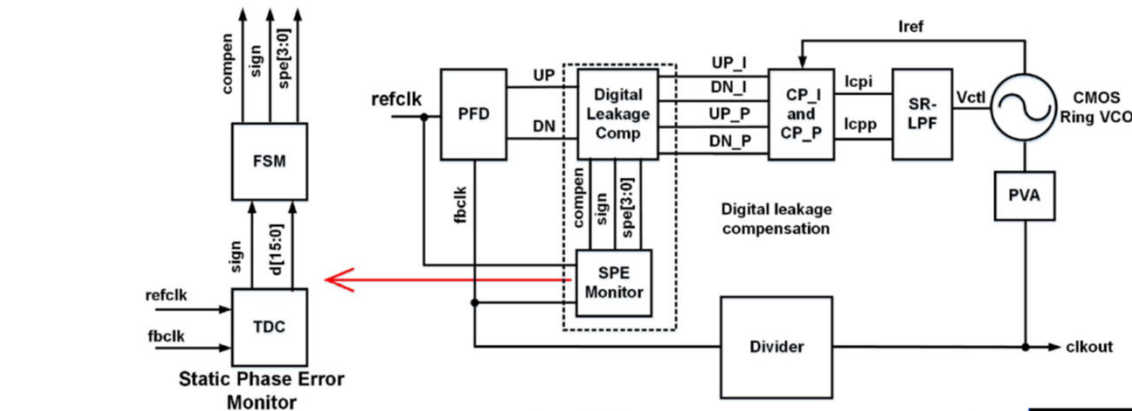
[**Fan ISSCC 2019**]

Static Phase Error due to leakage from supply

Two pulse digital leakage compensation for leakage from supply
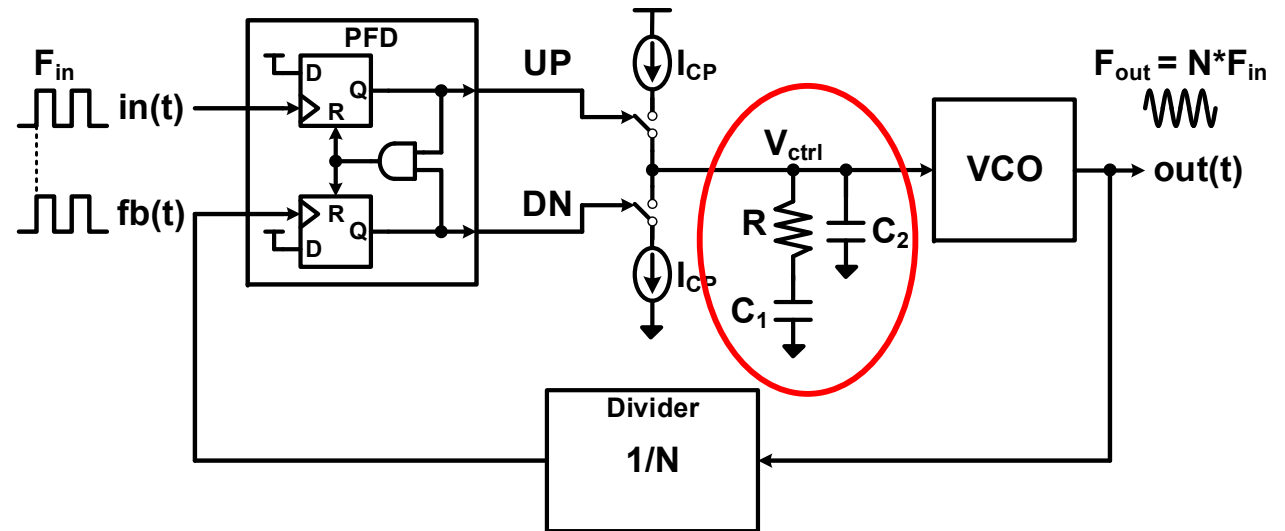

82

Charge Pump w/ Reversed Switches

- Swapping switches reduces **charge injection**
  - MOS caps (Md1-4) provide extra **clock feedthrough** cancellation
- Helper transistors Mx and My quickly turn-off current sources
- Dummy branch helps to match PFD loading
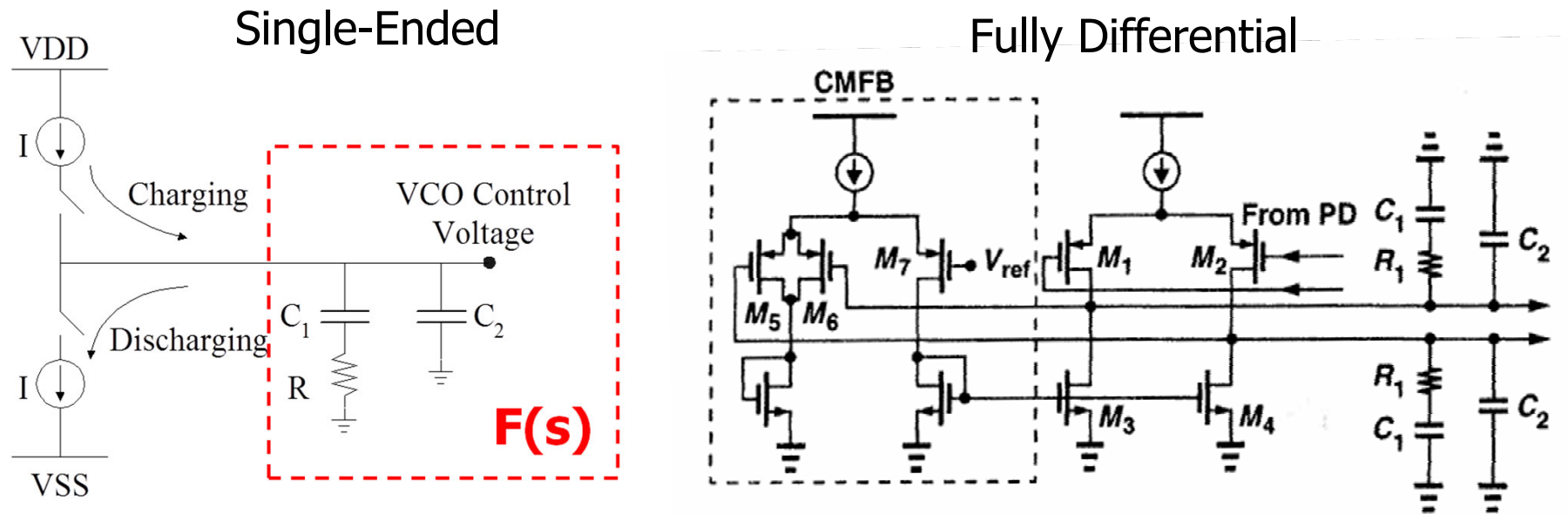- Helps with charge injection, but charge sharing is still an issue
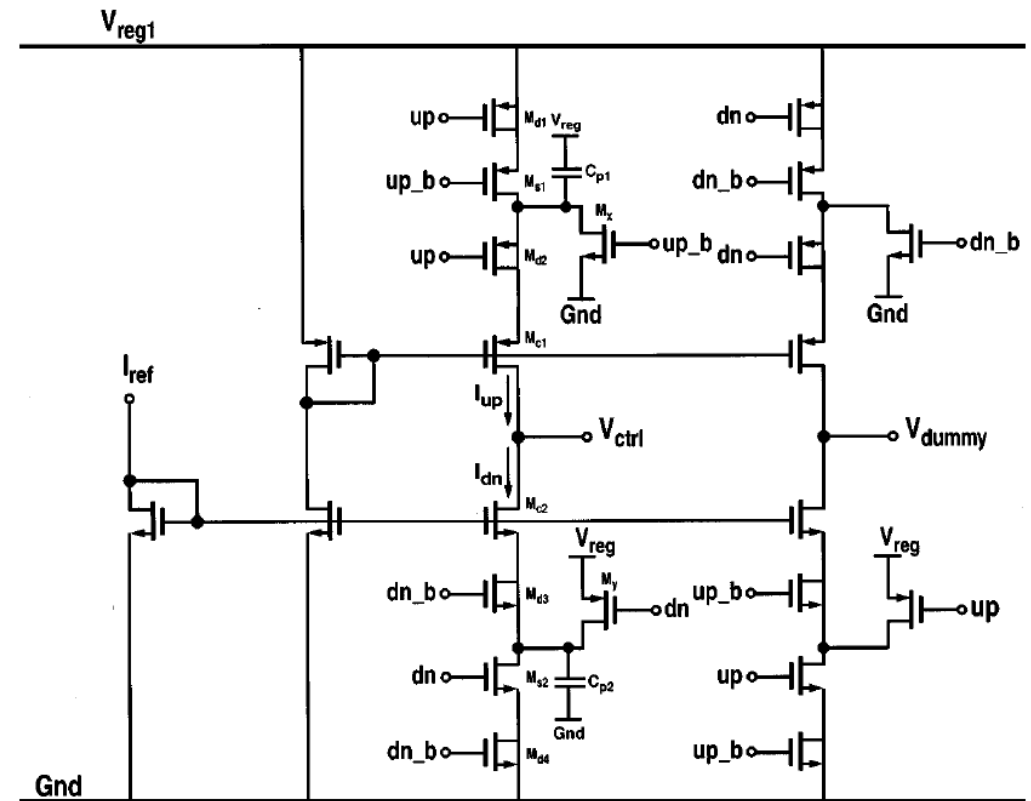
[**Ingino JSSC 2001**]

Charge-Pump PLL Circuits

- **Phase Detector**
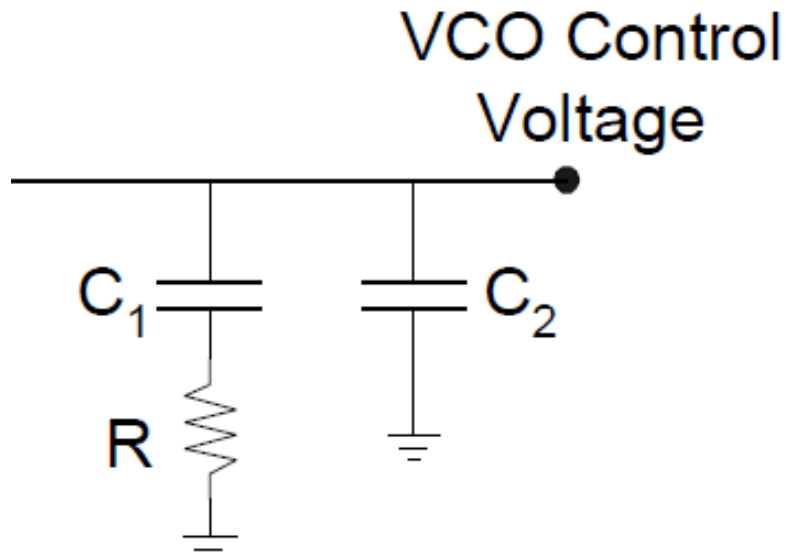
- **Charge-Pump**

- **Loop Filter**

- **VCO**

- **Divider**

Charge Pump PLL Passive PI Loop Filter

Single-Ended

Fully Differential

- Simple passive filter is most commonly used
- Integrates low-frequency phase errors onto C1 to set average frequency
- Resistor (proportional gain) isolates phase correction from frequency correction
- Primary capacitor C1 affects PLL bandwidth
- Zero frequency affects PLL stability
- Resistor adds thermal noise which is band-pass filtered by PLL

Loop Filter Transfer Function

- Neglecting secondary capacitor, C_2

VCO Control Voltage

$$F(s) = \frac{V_c(s)}{I_e(s)} = \frac{R\left(s + \dfrac{1}{RC_1}\right)}{s}$$

Loop Filter Frequency Response

$R = 31.8k\Omega$
$C = 62.2pF$
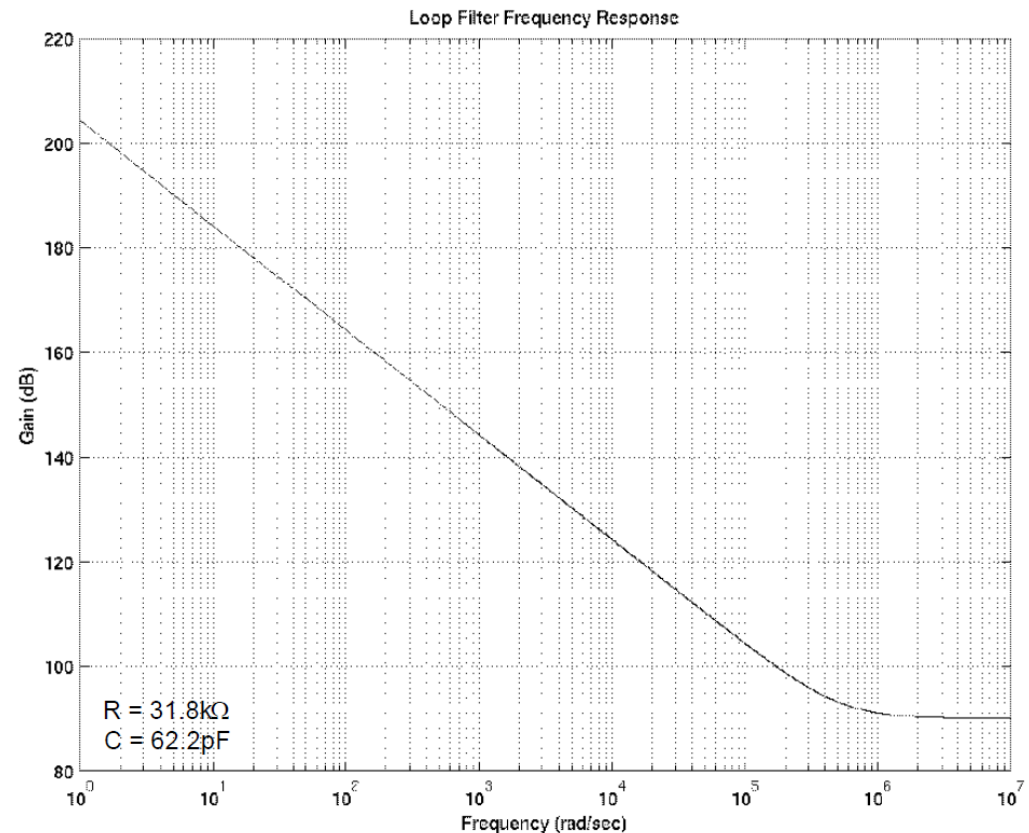
Loop Filter Transfer Function

- With secondary capacitor, C_2

VCO Control Voltage
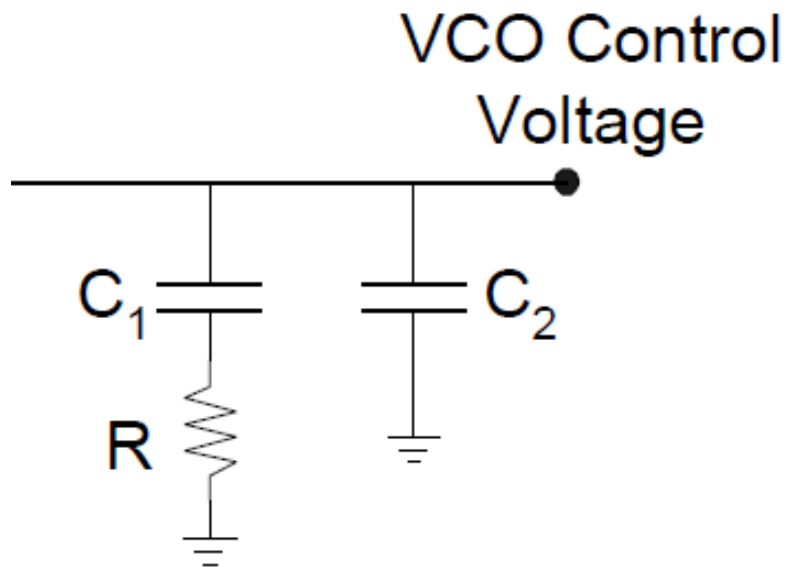
$$Z(s) = \frac{\dfrac{1}{C_2}\left(s + \dfrac{1}{RC_1}\right)}{s^2 + \dfrac{s(C_1 + C_2)}{RC_1C_2}}$$

Layout Extracted Loop Filter Frequency Response

□: Filter Output

Pole at 0Hz

Zero at f = $\dfrac{1}{2\pi RC_1}$ = 80.5kHz

Second Pole at f = $\dfrac{C_1 + C_2}{2\pi RC_1C_2}$ = 915kHz

(dBV)

freq (Hz)
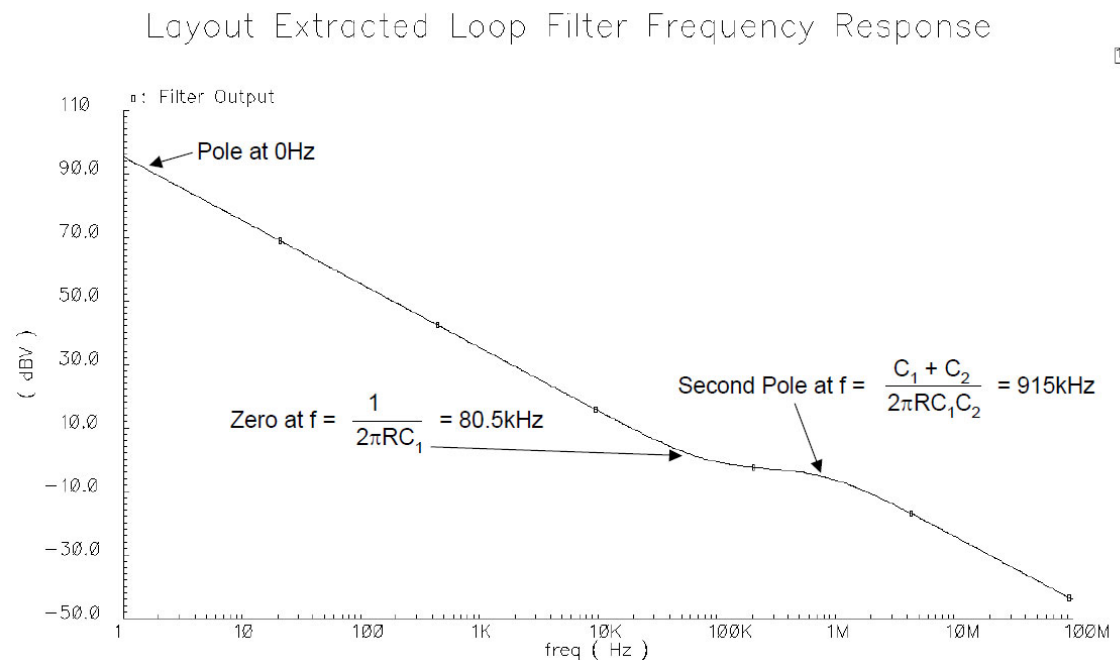
Why have C_2?

- Secondary capacitor smoothes control voltage ripple
- Can't make too big or loop will go unstable
  - $C_2 < C_1/10$ for stability
  - $C_2 > C_1/50$ for low jitter

PLL Synthesizing a 380MHz Signal
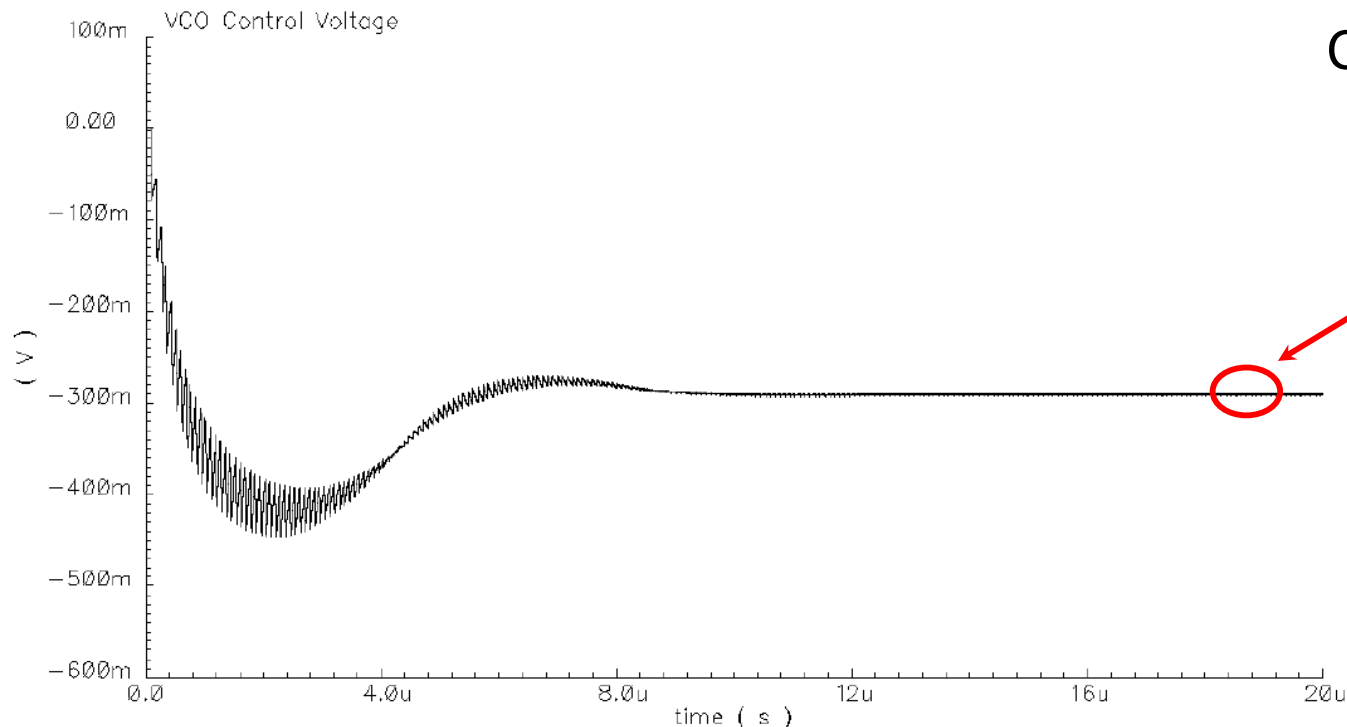
Control Voltage Ripple
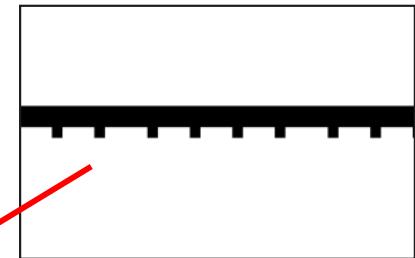
Loop Filter Capacitors

- To minimize area, we would like to use highest density caps

- Thin oxide MOS cap gate leakage can be an issue
  - Similar to adding a non-linear parallel resistor to the capacitor
  - Leakage is voltage and temperature dependent
  - Will result in excess phase noise and spurs

- Metal caps or thick oxide caps are a better choice
  - Trade-off is area

- Metal cap density can be <1/10 thin oxide caps

- Filter cap frequency response can be relatively low, as PLL loop bandwidths are typically 1-50MHz

Charge-Pump PLL Circuits

- Phase Detector
- Charge-Pump
- Loop Filter
- VCO
- Divider
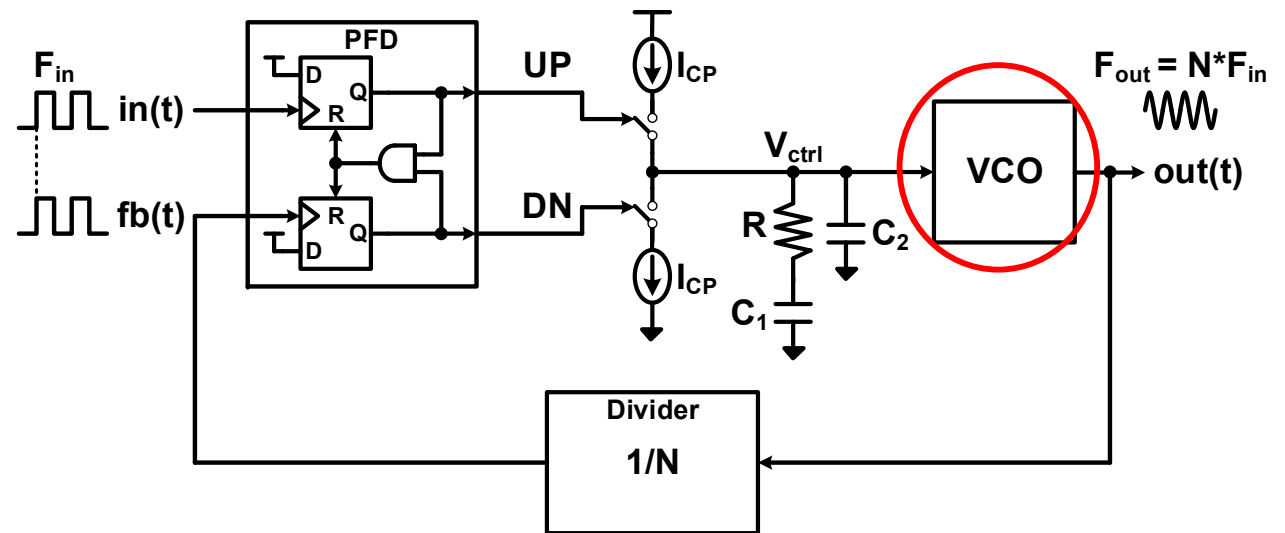
Voltage-Controlled Oscillator
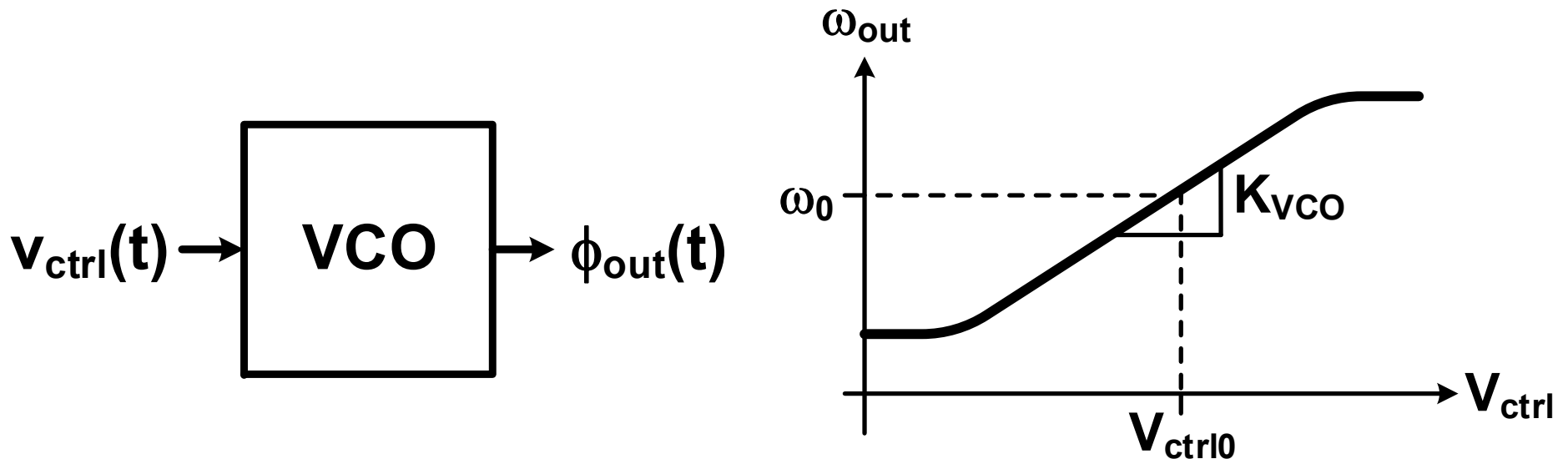
$$\omega_{out}(t) = \omega_0 + \Delta\omega_{out}(t) = \omega_0 + K_{VCO}v_{ctrl}(t)$$

- Time-domain phase relationship

$$\phi_{out}(t) = \int \Delta\omega_{out}(t)dt = \int K_{VCO}v_{ctrl}(t)dt$$

K_{VCO} units are $\dfrac{\text{rad}}{\text{s} \cdot \text{V}}$

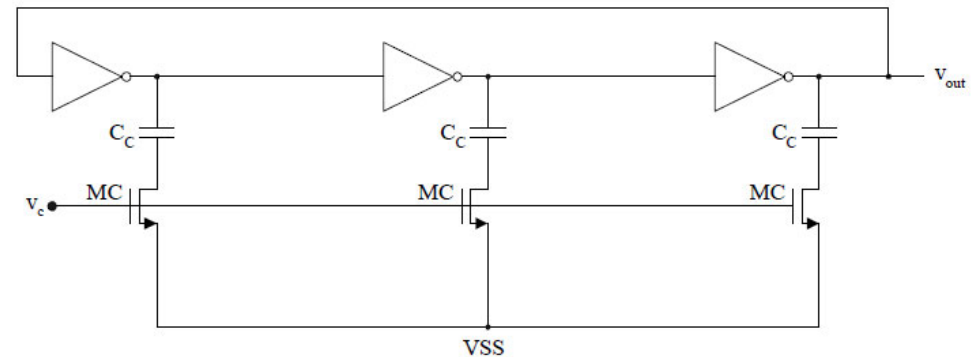$$\frac{2\pi(1\text{MHz})}{V} = 2\pi \times 10^6 \frac{\text{rad}}{\text{s} \cdot \text{V}}$$

Laplace Domain Model
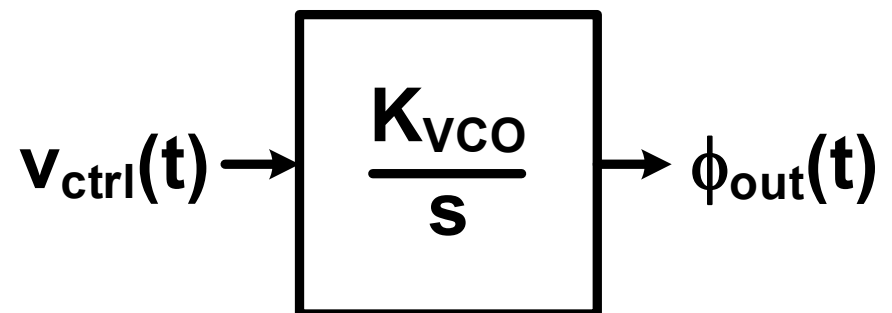
Voltage-Controlled Oscillators (VCO)

- ## Ring Oscillator
  - Easy to integrate
  - Wide tuning range (5x)
  - Higher phase noise

- ## LC Oscillator
  - Large area
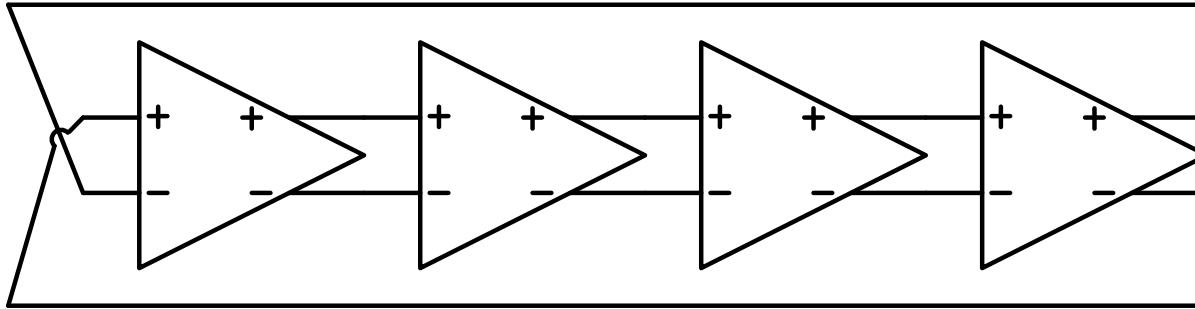 - Narrow tuning range (20-30%)
  - Lower phase noise
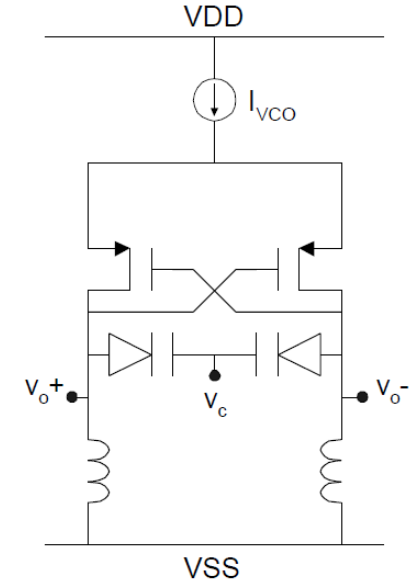
Barkhausen's Oscillation Criteria

[**Sanchez**]
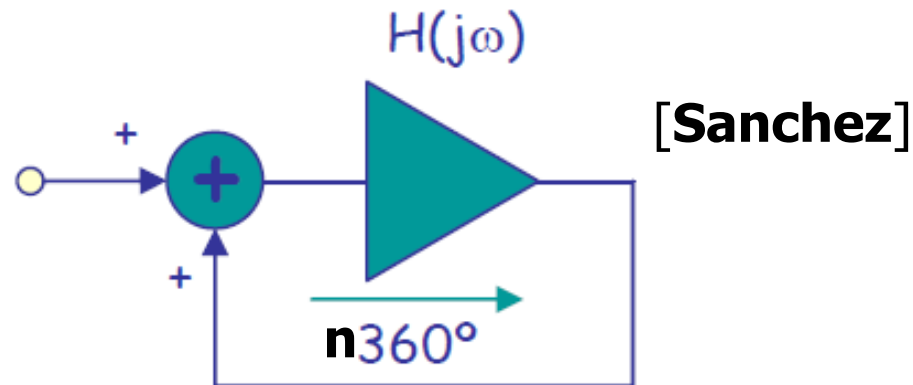
Closed-loop transfer function: $\dfrac{H(j\omega)}{1 - H(j\omega)}$

- Sustained oscillation occurs if $H(j\omega) = 1$

- 2 conditions:
  - Gain = 1 at oscillation frequency ω_0
  - Total phase shift around loop is n360° at oscillation frequency ω_0

Ring Oscillator Example
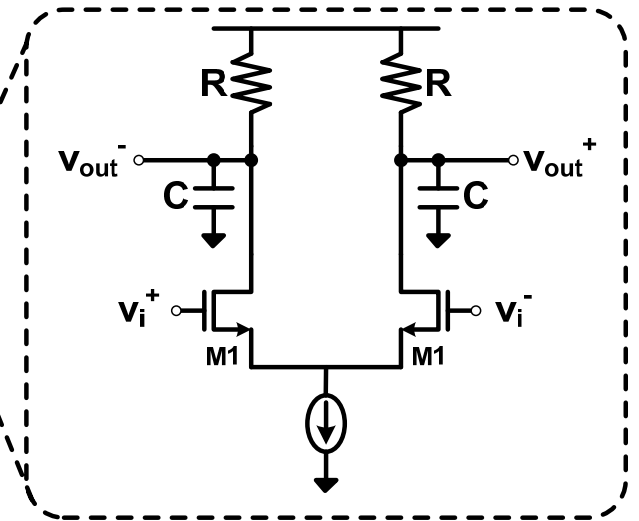
$$H(s) = -\frac{A_0^4}{\left(1 + \dfrac{s}{\omega_o}\right)^4}$$

Phase Condition: $\tan^{-1}\left(\dfrac{\omega_{osc}}{\omega_o}\right) = 45° \rightarrow \boxed{\omega_{osc} = \omega_o = \dfrac{1}{RC}}$

Gain Condition: $\dfrac{A_0^4}{\left[\sqrt{1 + \left(\dfrac{\omega_{osc}}{\omega_o}\right)^2}\right]^4} = 1 \rightarrow \boxed{A_0 = \sqrt{2} = g_{m1}R}$
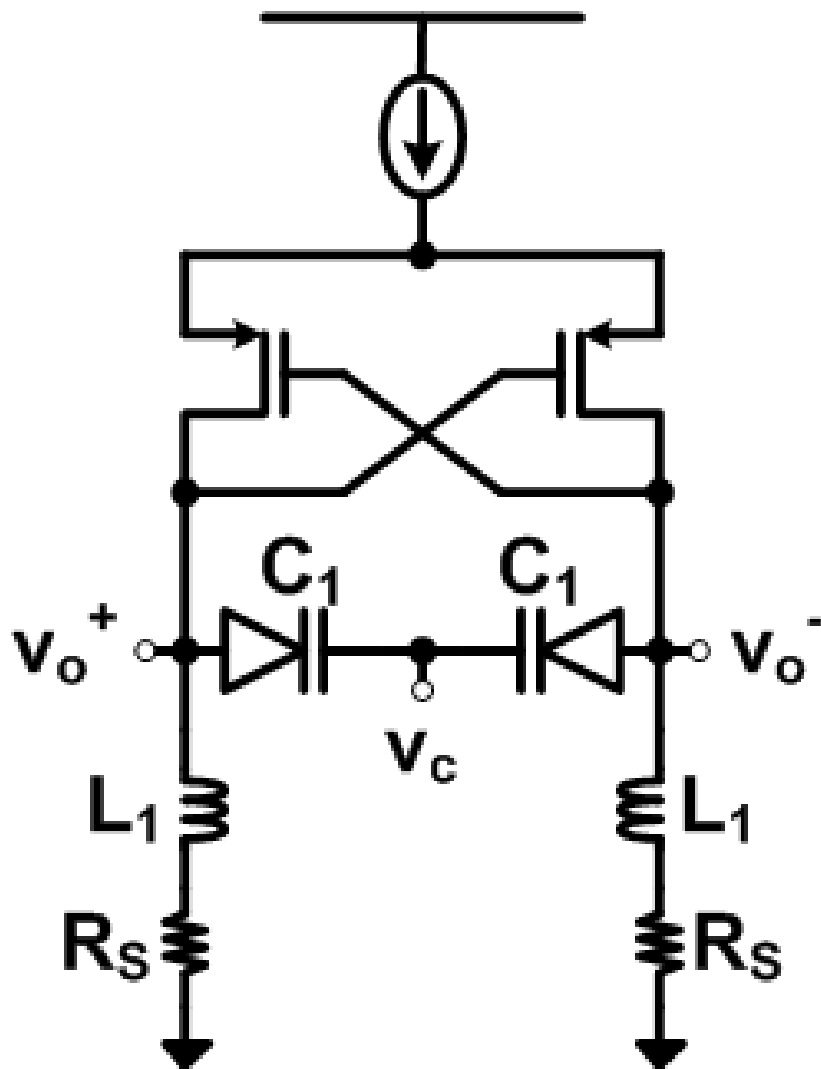
LC Oscillator Example
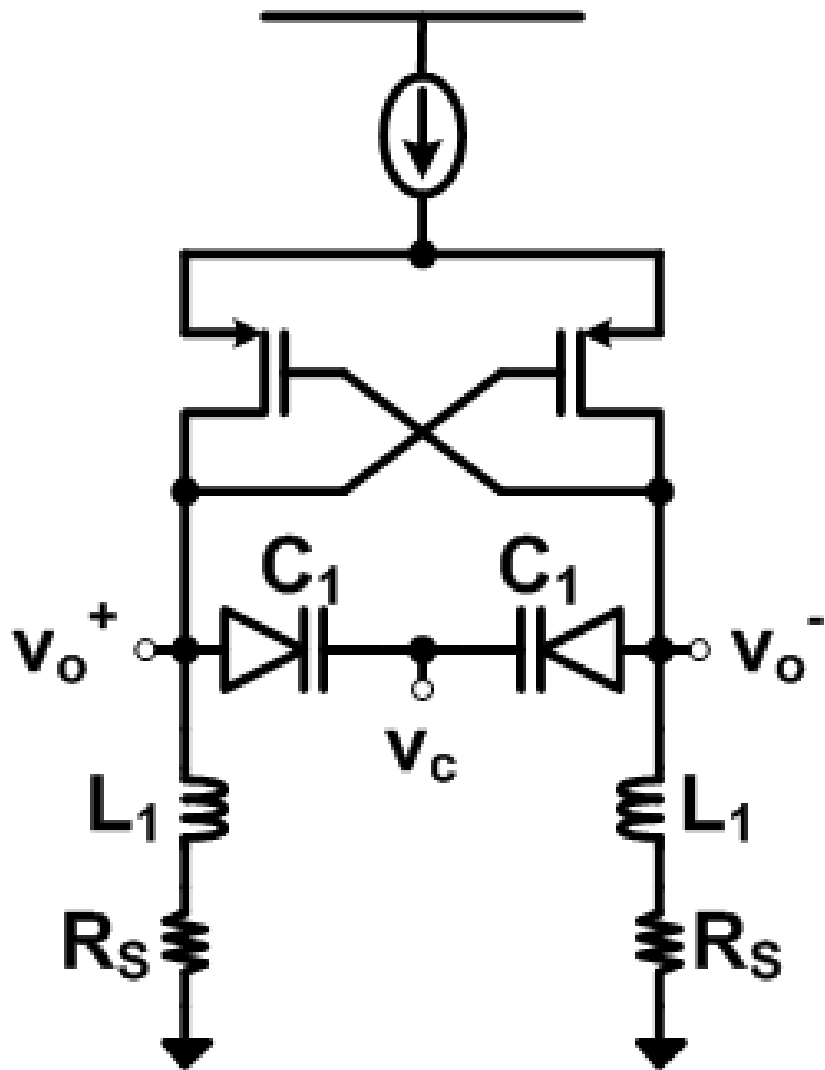
- Oscillation phase shift condition satisfied at the frequency when the LC (and R) tank load displays a purely real impedance, i.e. 0° phase shift

LC tank impedance

$$Z_{eq}(s) = \frac{R_S + L_1 s}{1 + L_1 C_1 s^2 + R_S C_1 s}$$

$$\left| Z_{eq}(s = j\omega) \right|^2 = \frac{R_S^2 + L_1^2 \omega^2}{\left(1 - L_1 C_1 \omega^2\right)^2 + R_S^2 C_1^2 \omega^2}$$
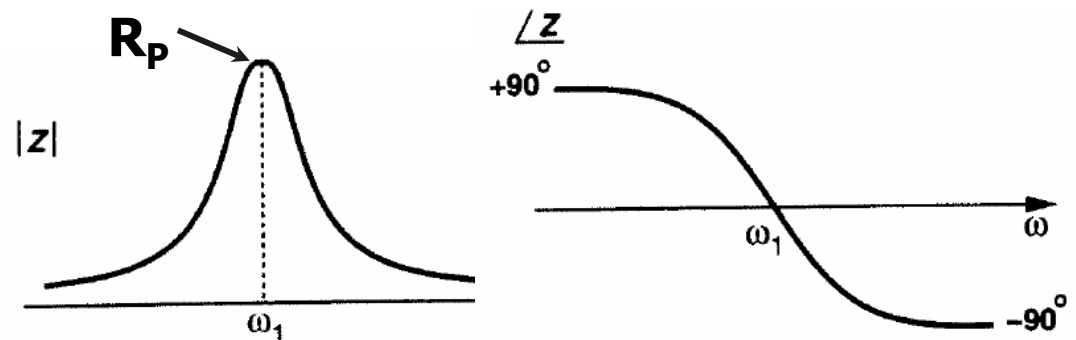
LC Oscillator Example

- Transforming the series loss resistor of the inductor to an equivalent parallel resistance
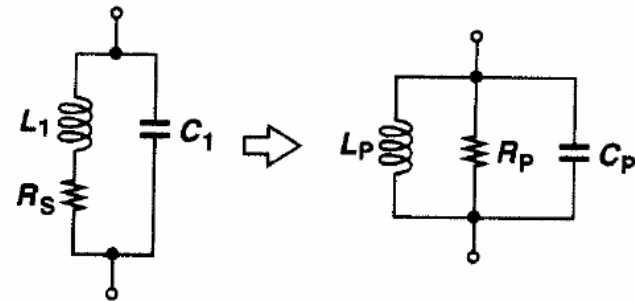
$$L_P = L_1\left(1 + \frac{R_S^2}{L_1^2\omega^2}\right), \quad C_P = C_1, \quad R_P \approx \frac{L_1^2\omega^2}{R_S}$$
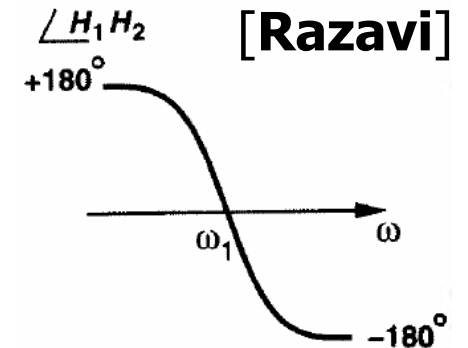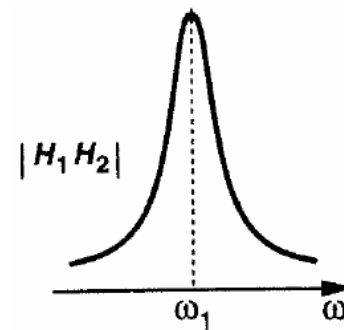
$$\omega_1 = \frac{1}{\sqrt{L_P C_P}}$$

[**Razavi**]

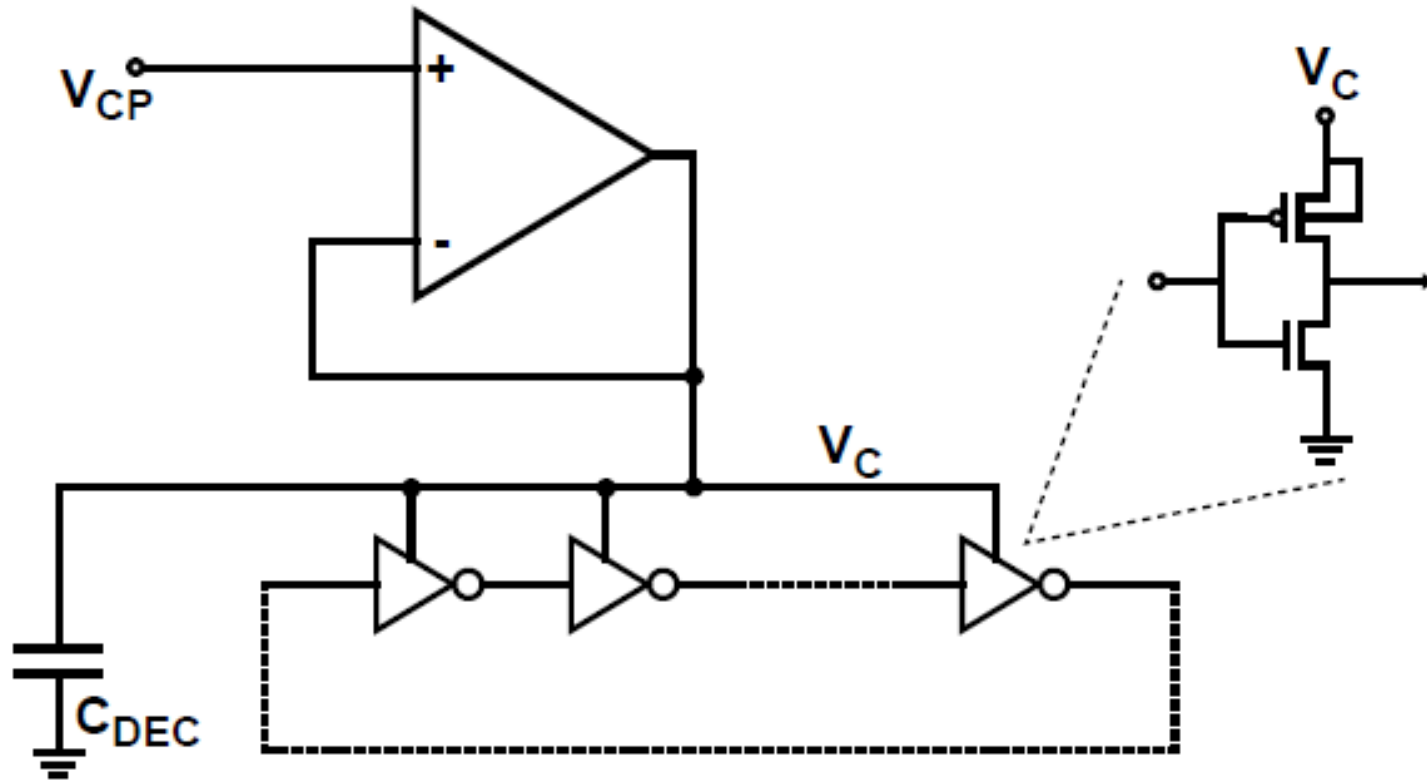# LC Oscillator Example

Loop Gain   [**Razavi**]
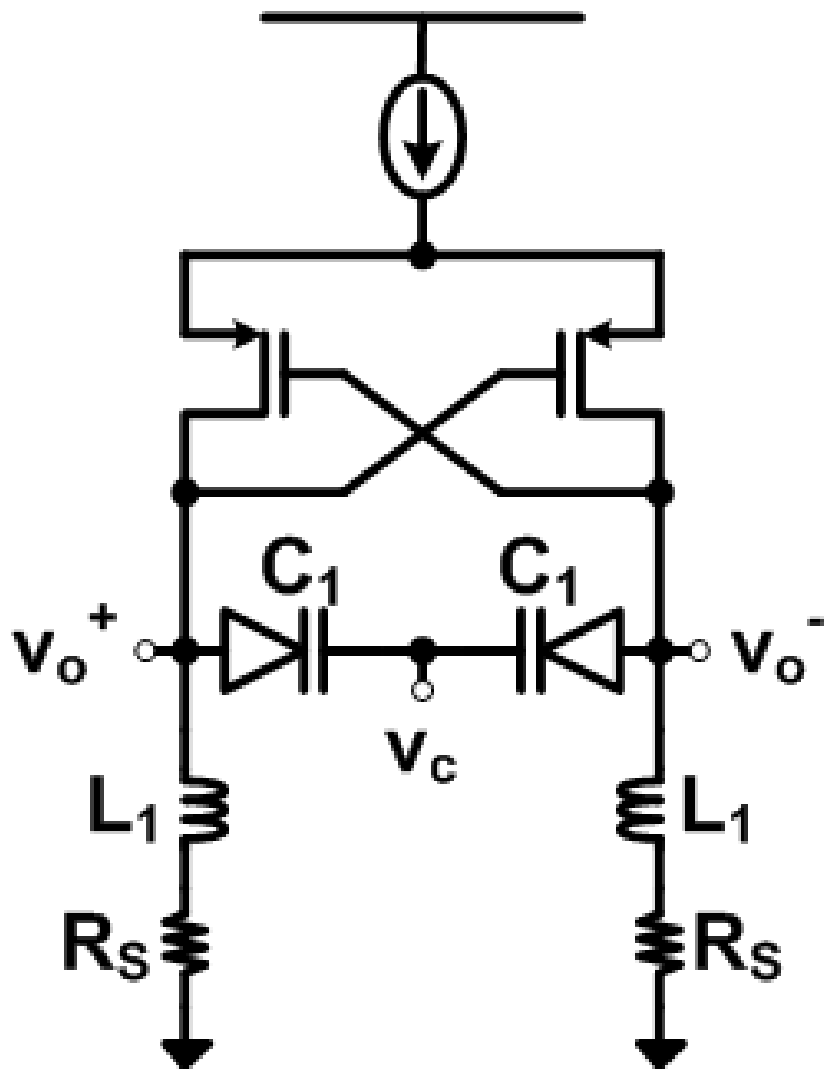
- Phase condition satisfied at $\omega_1 = \dfrac{1}{\sqrt{L_P C_P}}$

- Gain condition satisfied when $(g_m R_P)^2 \geq 1$

- Can also view this circuit as a parallel combination of a tank with loss resistance $2R_P$ and negative resistance of $2/g_m$

- Oscillation is satisfied when

$$\frac{1}{g_m} \leq R_P$$
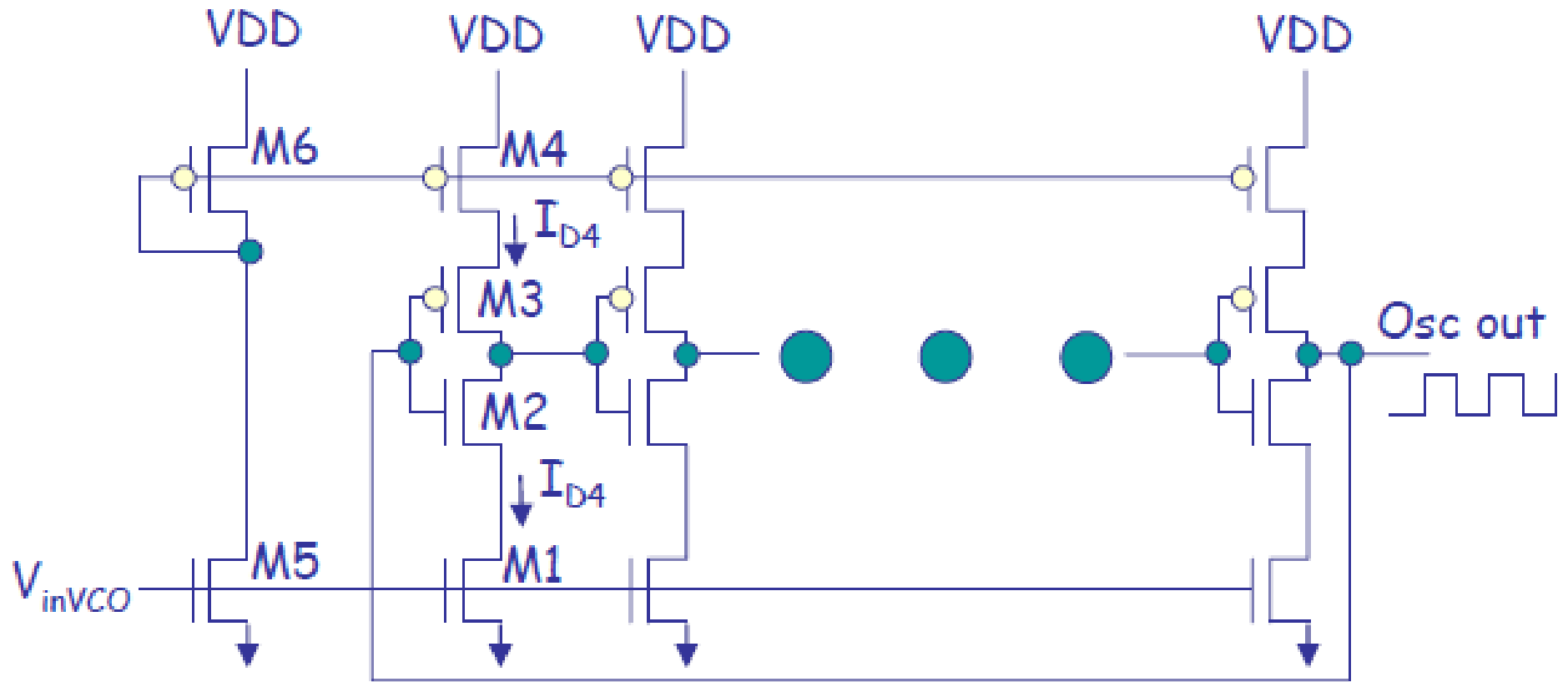
Supply-Tuned Ring Oscillator

[**Sidiropoulos VLSI 2000**]

$$T_{VCO} = 2nT_D \approx \frac{2nC_{stage}}{\beta(V_c - V_{th})}$$

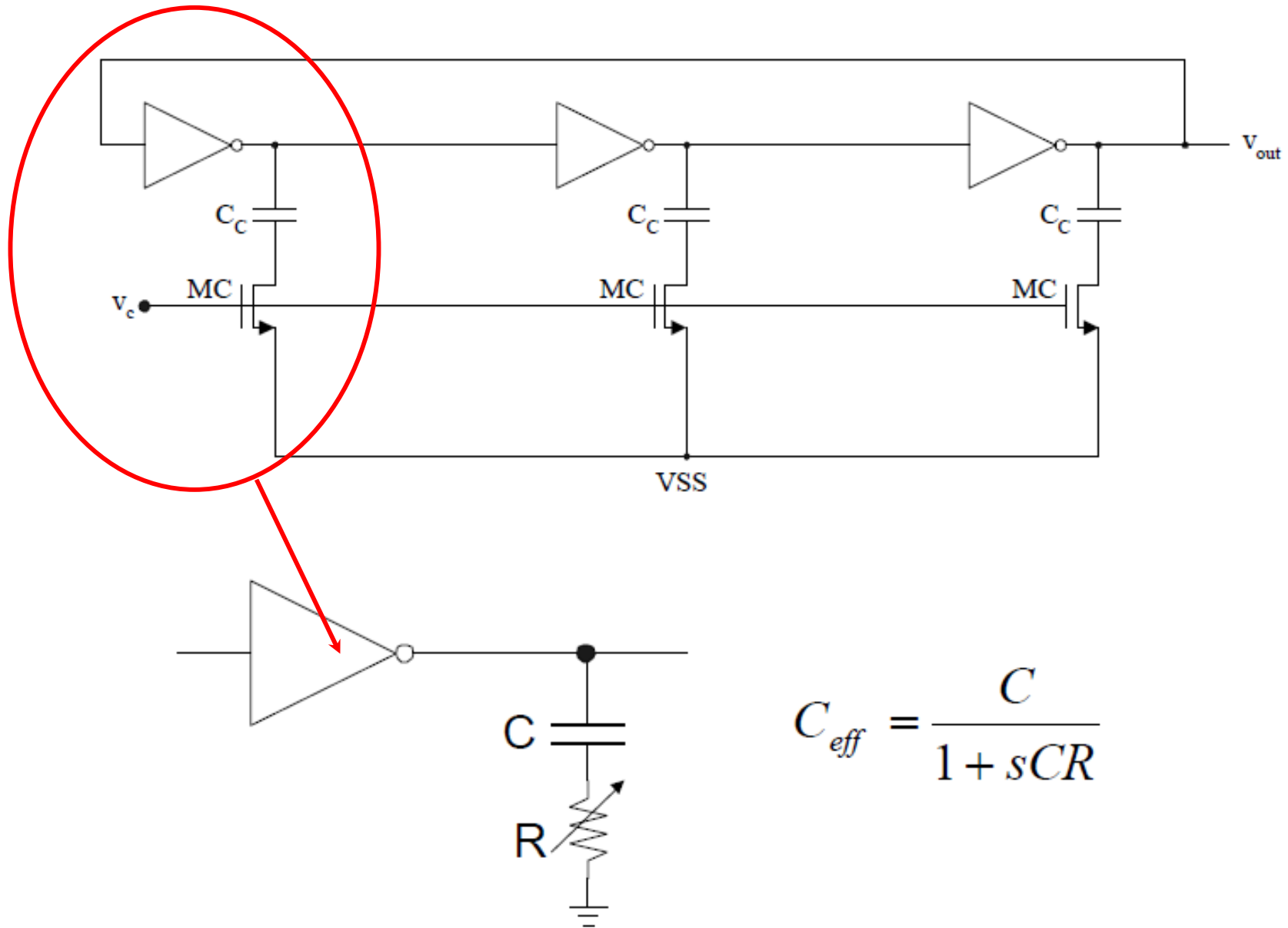$$K_{VCO} = \frac{\partial f_{VCO}}{\partial V_c} = \frac{\beta}{2nC_{stage}}$$
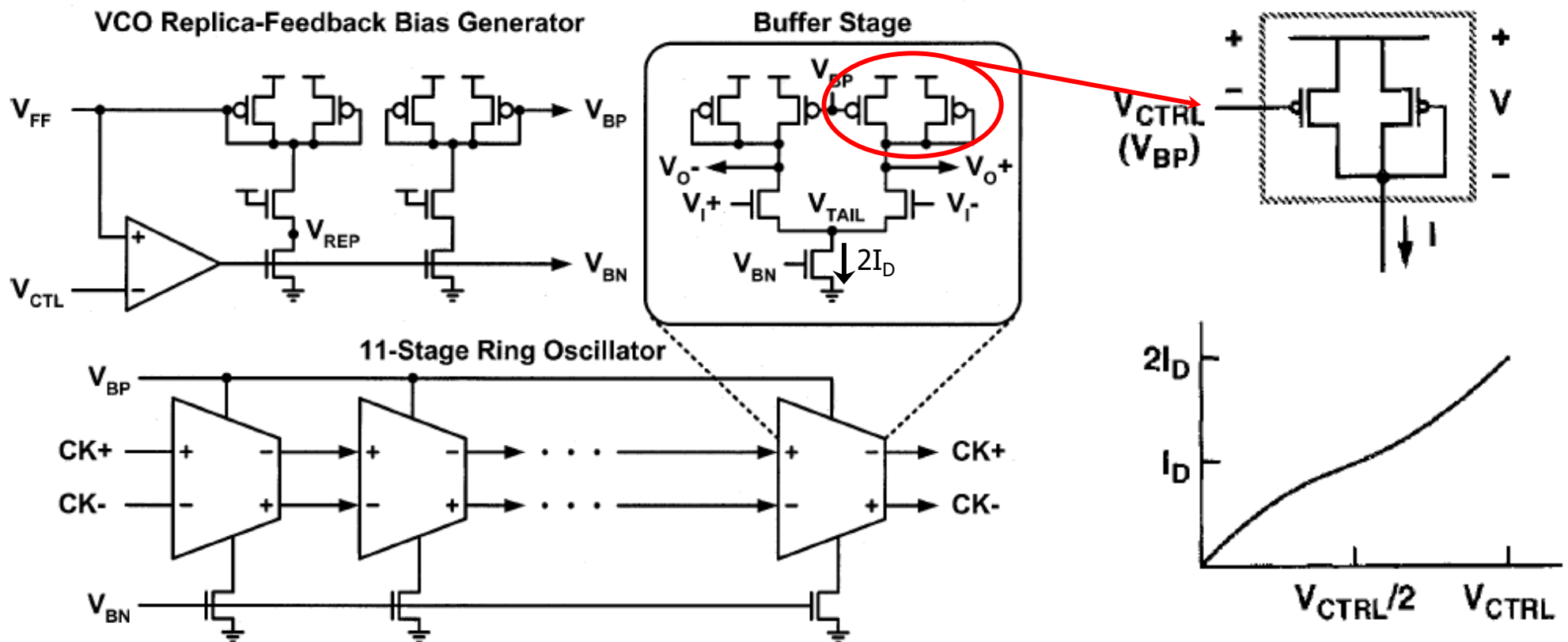
Current-Starved Ring Oscillator

[Sanchez]

Current – starved VCO.

Capacitive-Tuned Ring Oscillator

$$C_{eff} = \frac{C}{1 + sCR}$$

Symmetric Load Ring Oscillator

[Maneatis JSSC 1996 & 2003]

VCO Replica-Feedback Bias Generator

Buffer Stage

11-Stage Ring Oscillator

- Symmetric load provides frequency tuning at excellent supply noise rejection

- See Maneatis papers for self-biased techniques to obtain constant damping factor and loop bandwidth (% of ref clk)
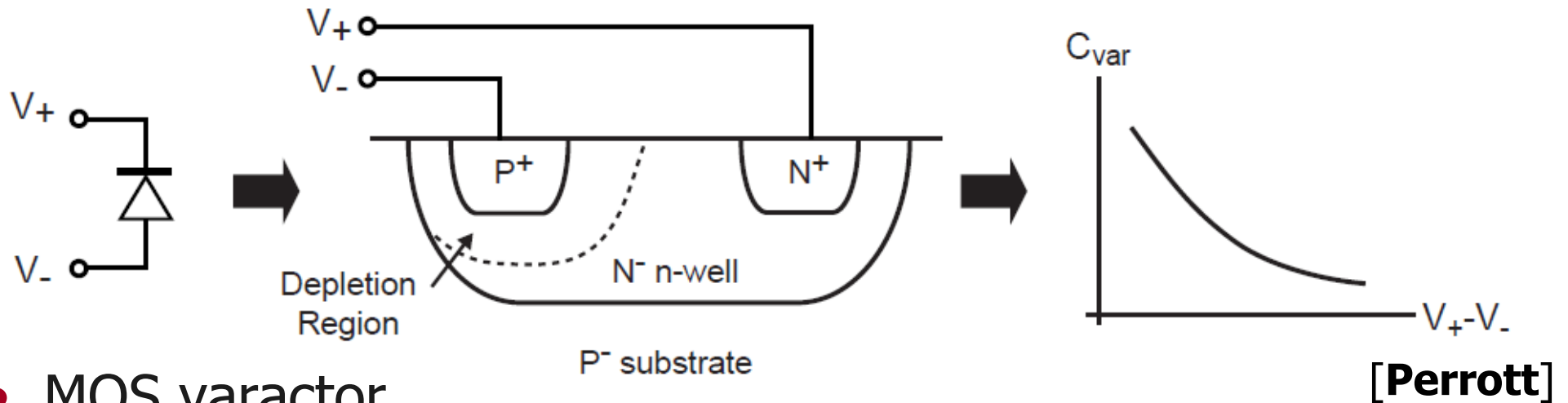
101

LC Oscillator

- A variable capacitor (varactor) is often used to adjust oscillation frequency

- Total capacitance includes both tuning capacitance and fixed capacitances which reduce the tuning range

$$\omega_{osc} = \frac{1}{\sqrt{L_P C_P}} = \frac{1}{\sqrt{L_P \left(C_{tune} + C_{fixed}\right)}}$$
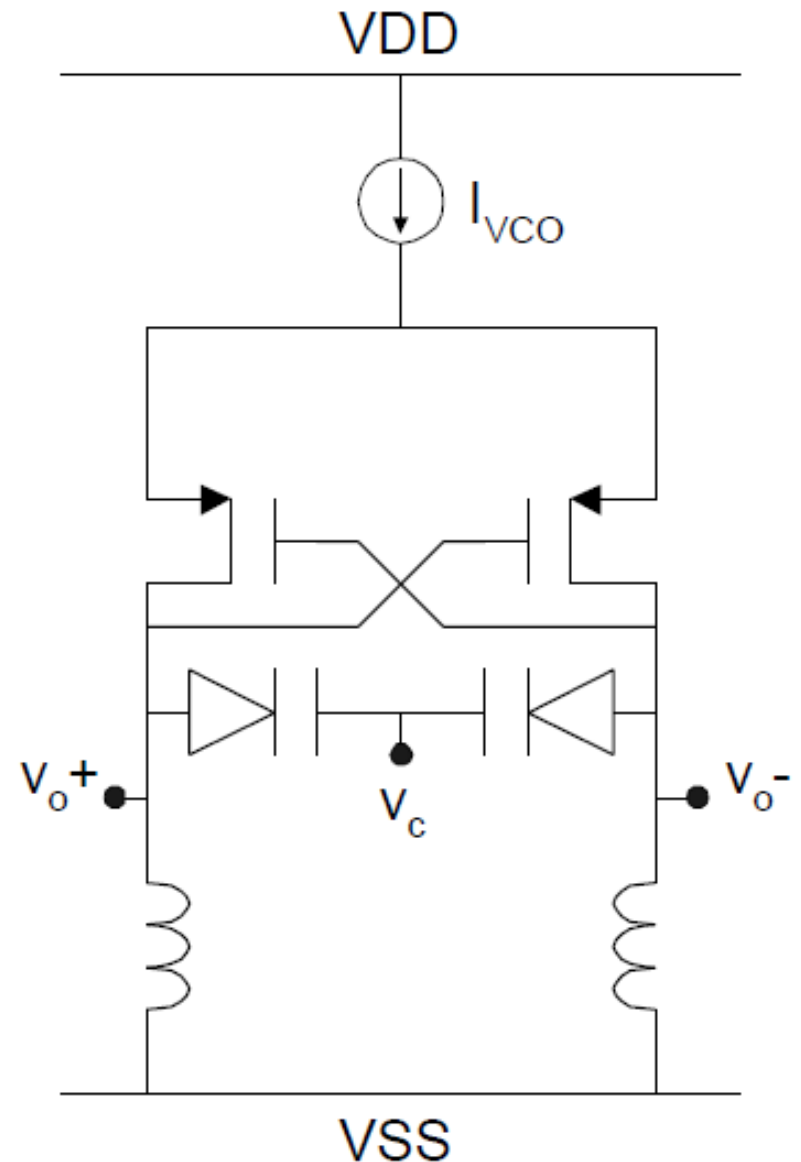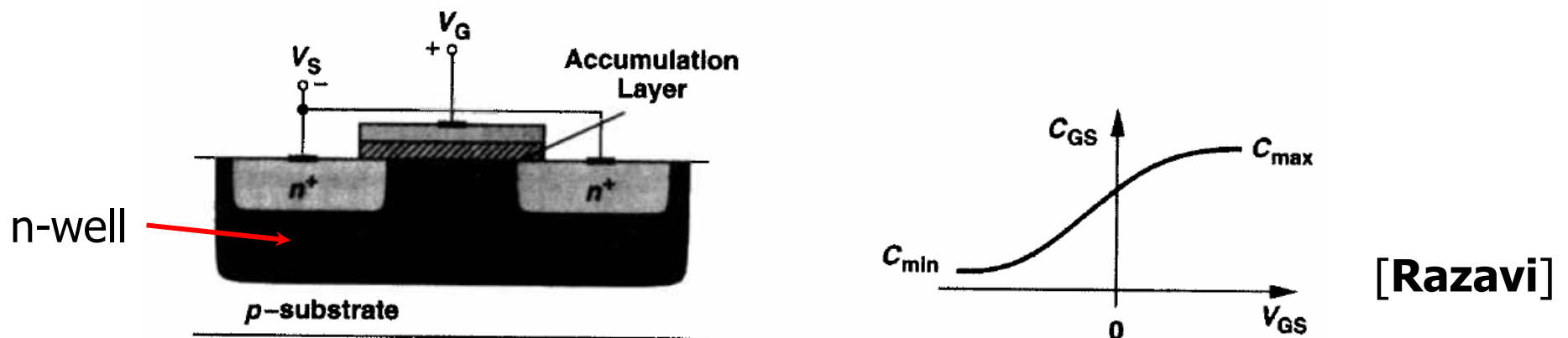
Varactors

- pn junction varactor
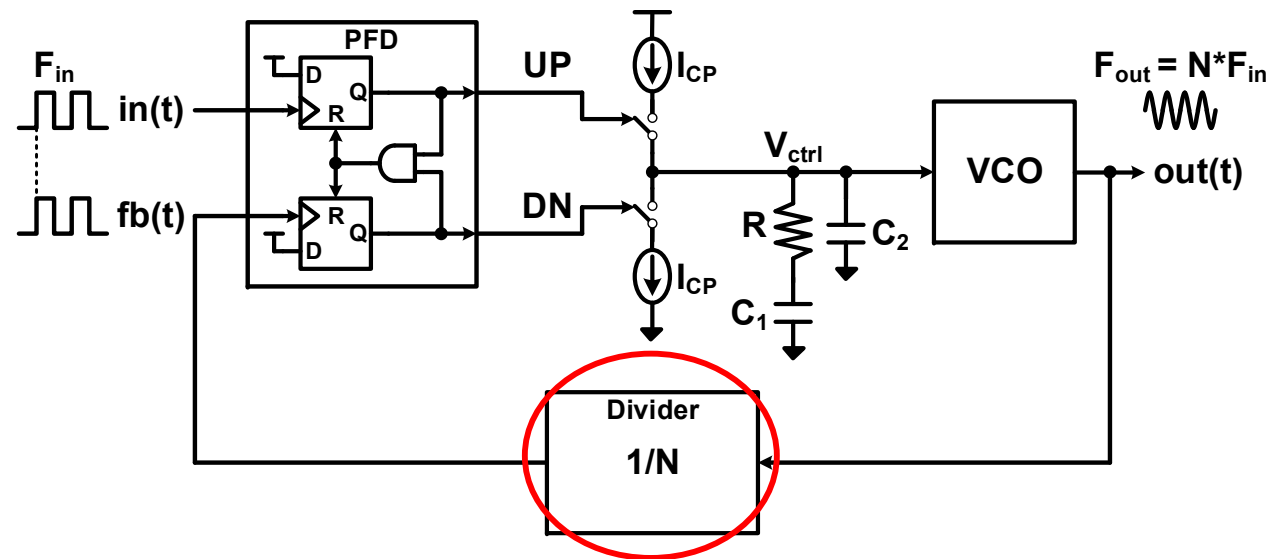 - Avoid forward bias region to prevent oscillator nonlinearity

[**Perrott**]

- MOS varactor
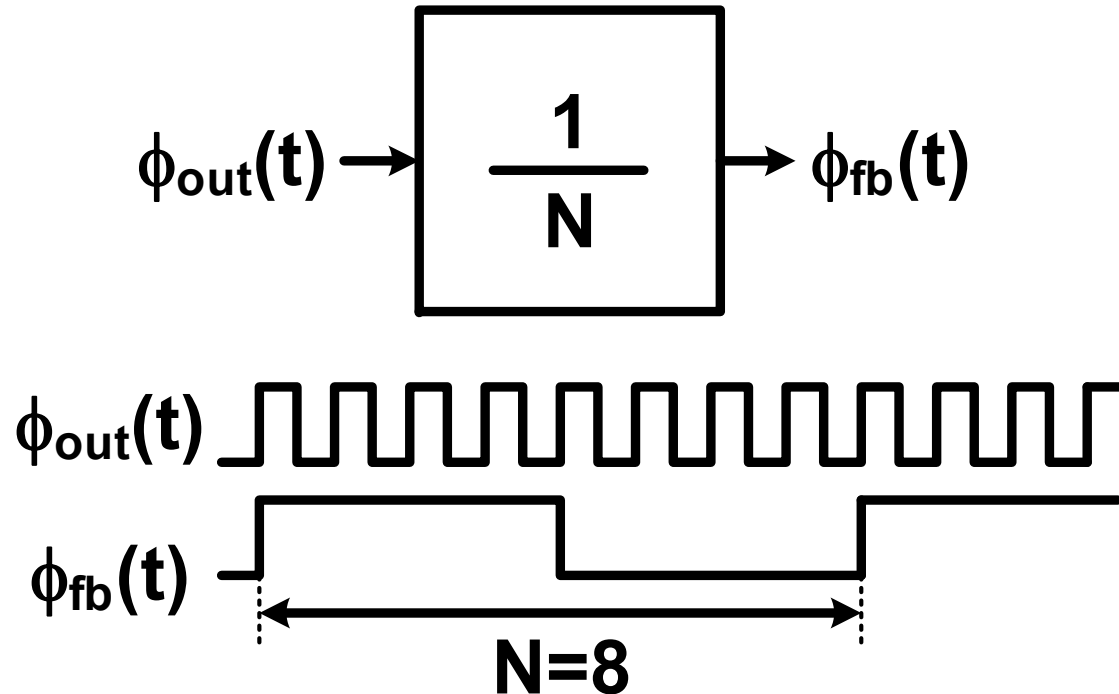 - Accumulation-mode devices have better Q than inversion-mode

[**Razavi**]

Charge-Pump PLL Circuits

- Phase Detector

- Charge-Pump

- Loop Filter

- VCO

- Divider

Loop Divider

$$\phi_{out}(t) \rightarrow \boxed{\frac{1}{N}} \rightarrow \phi_{fb}(t)$$

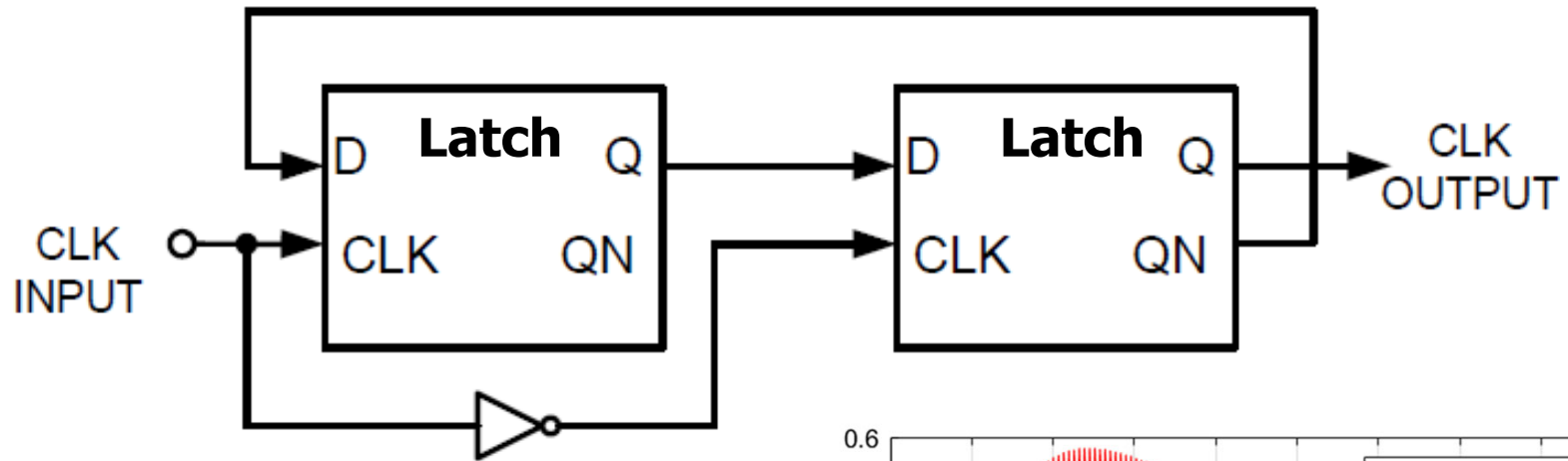$\phi_{out}(t)$ ⊓⊔⊓⊔⊓⊔⊓⊔⊓⊔⊓⊔⊓⊔⊓⊔

$\phi_{fb}(t)$

N=8

- Time-domain model
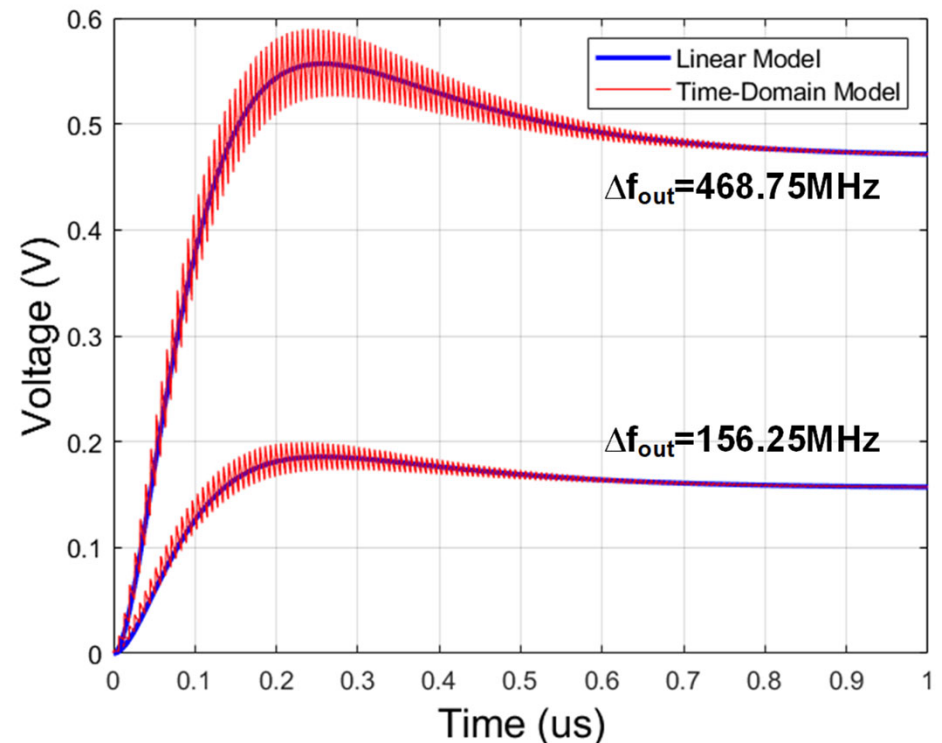
$$\omega_{fb}(t) = \frac{1}{N}\omega_{out}(t)$$

$$\phi_{fb}(t) = \int \frac{1}{N}\omega_{out}(t)\mathrm{dt} = \frac{1}{N}\phi_{out}(t)$$

- The loop divider is dimension-less in the PLL linear model
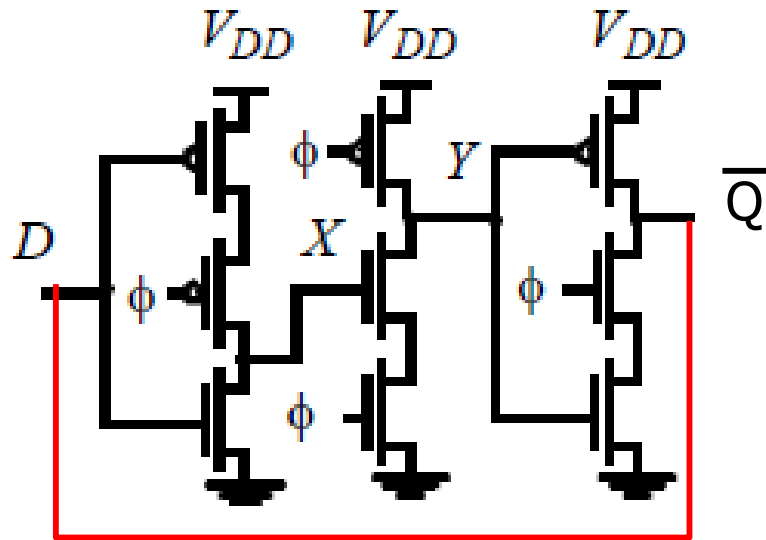
Basic Divide-by-2

- Divide-by-2 can be realized by a flip-flip in "negative feedback"

- Divider should operate correctly up to the maximum output clock frequency of interest **PLUS** some margin

Divide-by-2 with TSPC FF

True Single Phase Clock Flip-Flop

Divider Equivalent Circuit
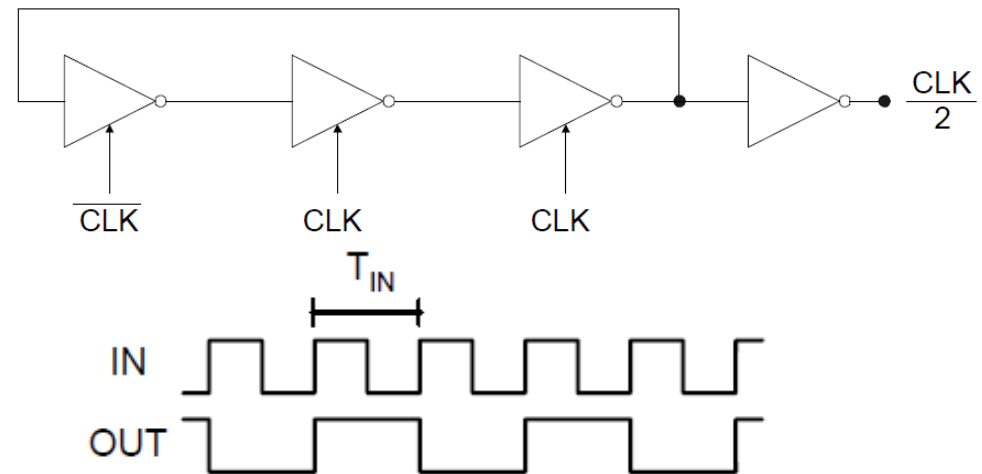**Note: output inverter not in left schematic**

- Advantages
  - Reasonably fast, compact size, and no static power
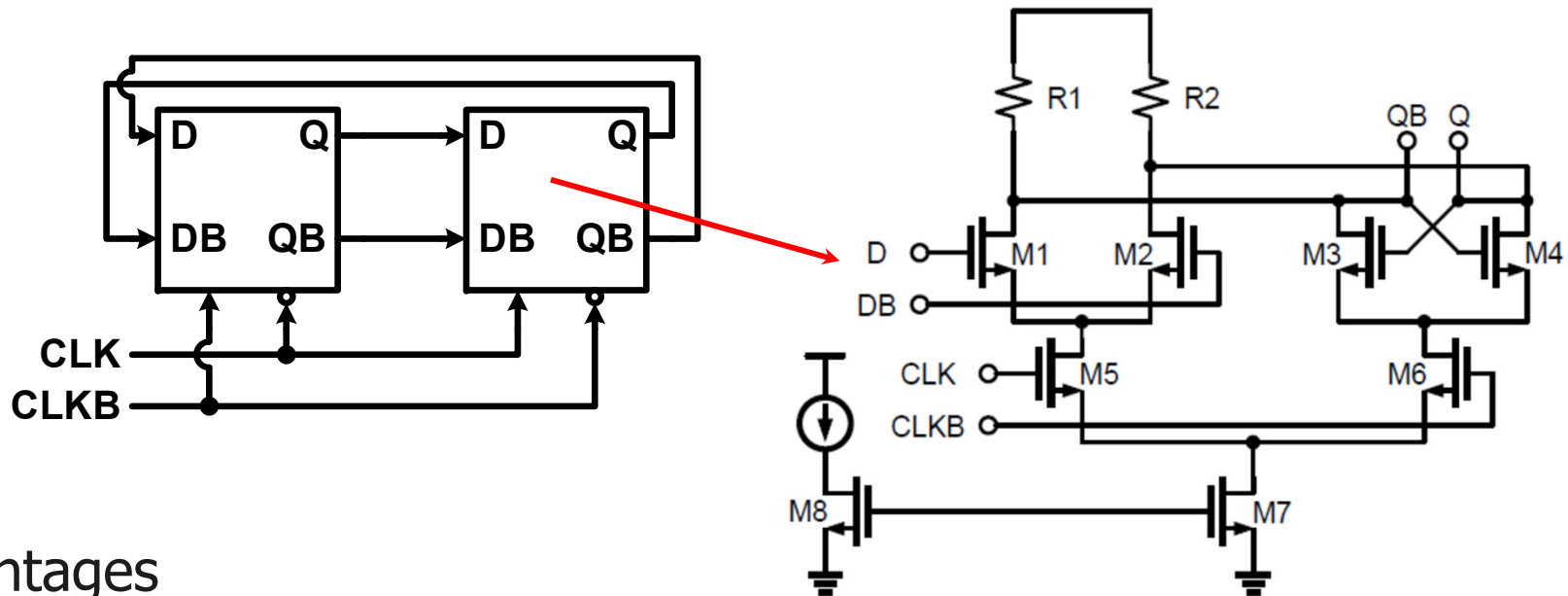 - Requires only one phase of the clock
- Disadvantages
  - Signal needs to propagate through three gates per input cycle
  - Need full swing CMOS inputs
  - Dynamic flip-flop can fail at low frequency (test mode) due to leakage, as various nodes are floating during different CLK phases & output states
    - Ex: Q_bar is floating during when CLK is low

107

Divide-by-2 with CML FF

- Advantages
  - Signal only propagates through two CML gates per input cycle
  - Accepts CML input levels
- Disadvantages
  - Larger size and dissipates static power
  - Requires differential input
  - Need tail current biasing
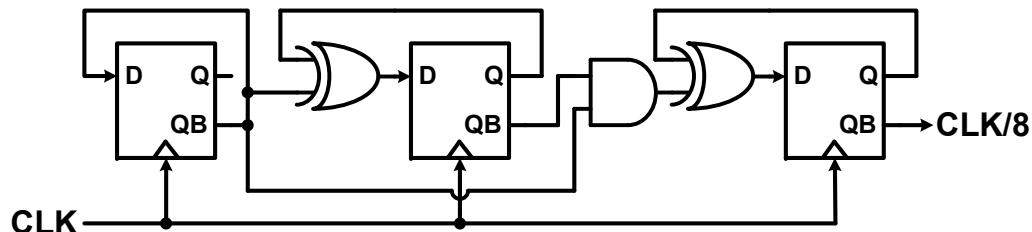- Additional speedup (>50%) can be achieved with shunt peaking inductors

Binary Dividers:
Asynchronous vs Synchronous

Asynchronous Divider
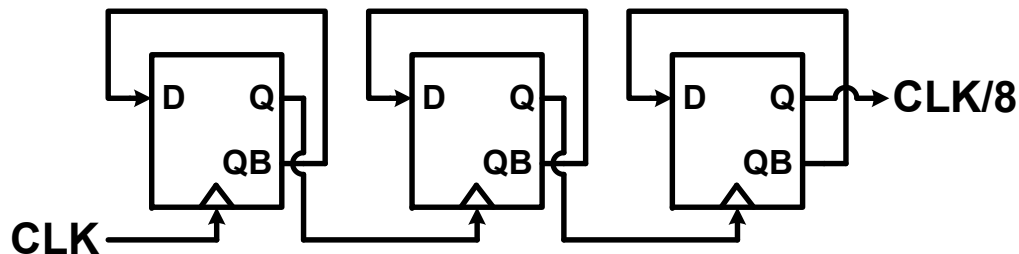
- Advantages
  - Each stage runs at lower frequency, resulting in reduced power
  - Reduced high frequency clock loading
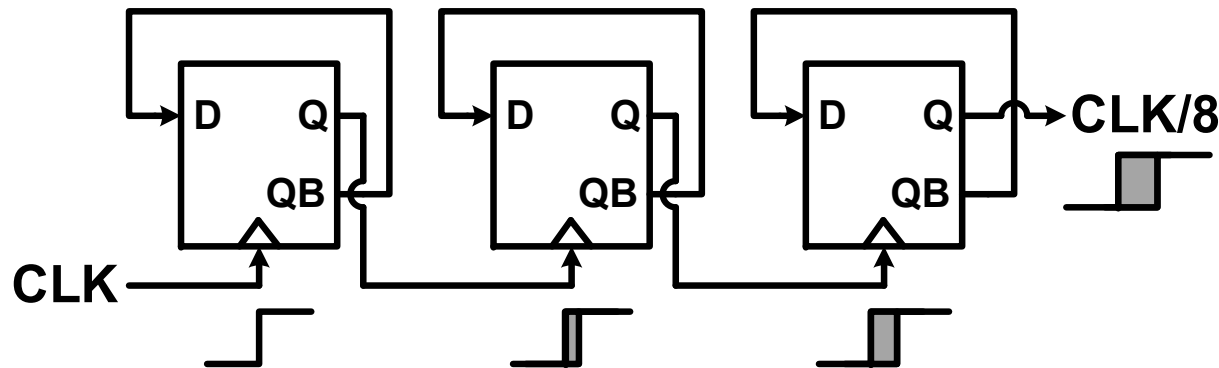- Disadvantage
  - Jitter accumulation

Synchronous Divider

- Advantage
  - Reduced jitter
- Disadvantage
  - All flip-flops work at maximum frequency, resulting in high power
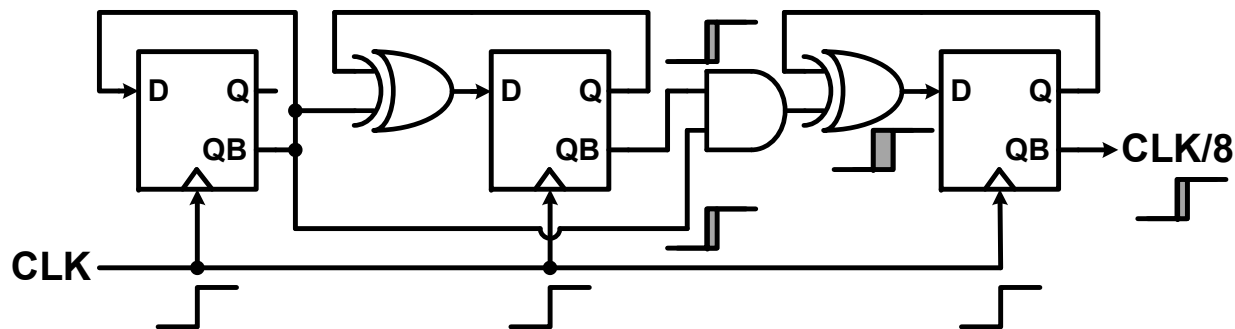 - Large loading on high frequency clock

# Jitter in Asynchronous vs Synchronous Dividers

Asynchronous

- Jitter accumulates with the clock-to-Q delays through the divider

- Extra divider delay can also degrade PLL phase margin
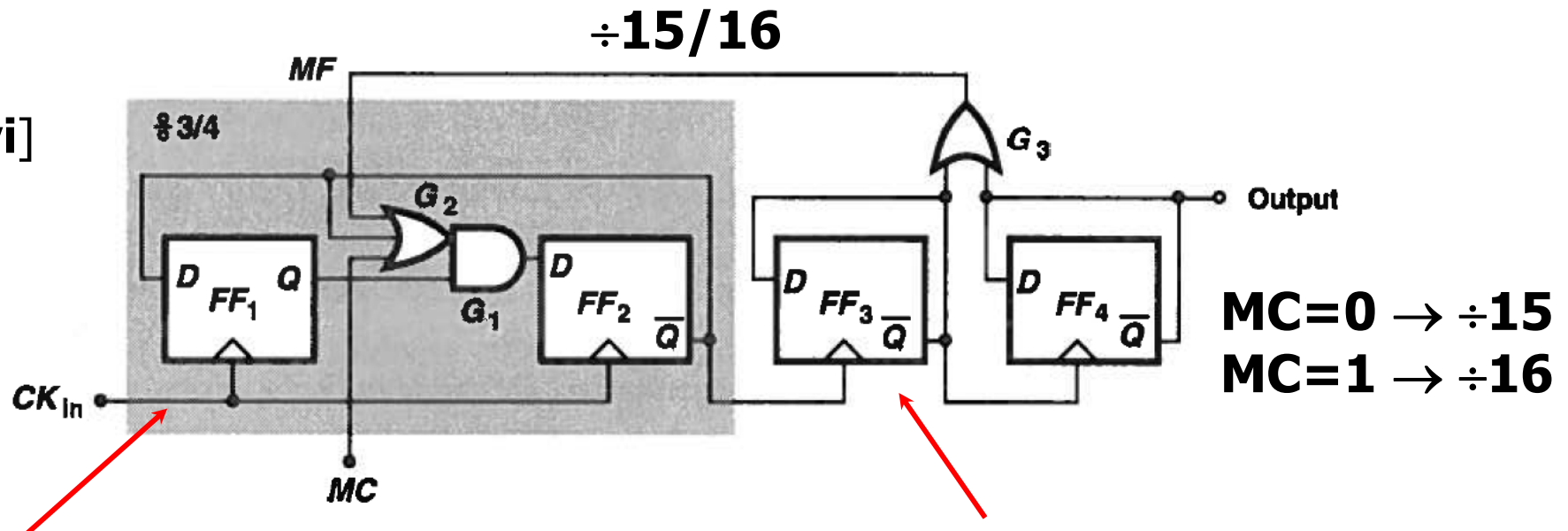
Synchronous

- Divider output is "sampled" with high frequency clock

- Jitter on divider clock is similar to VCO output
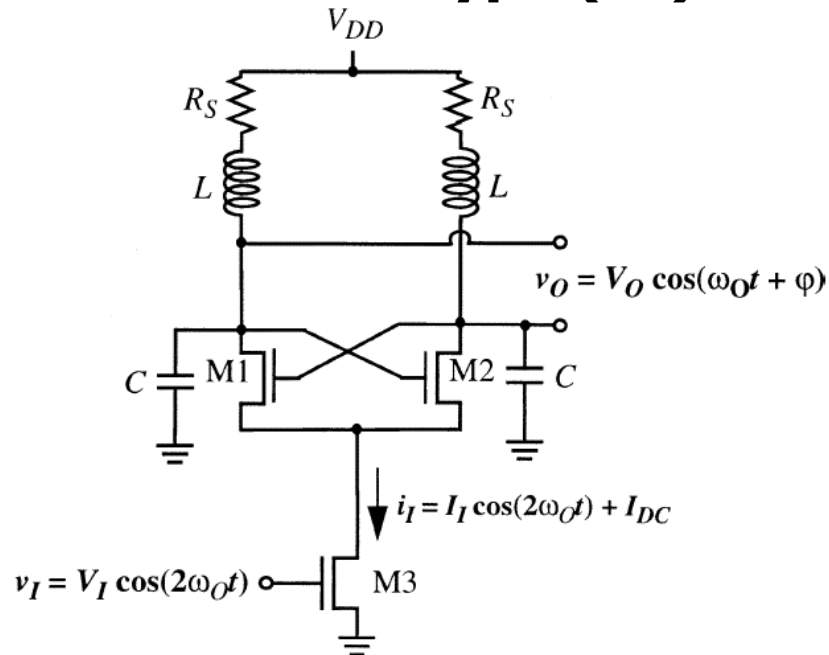
- Minimal divider delay

Dual Modulus Prescalers

÷2/3

MC=0 → ÷3
MC=1 → ÷2

÷15/16

[**Razavi**]

MC=0 → ÷15
MC=1 → ÷16
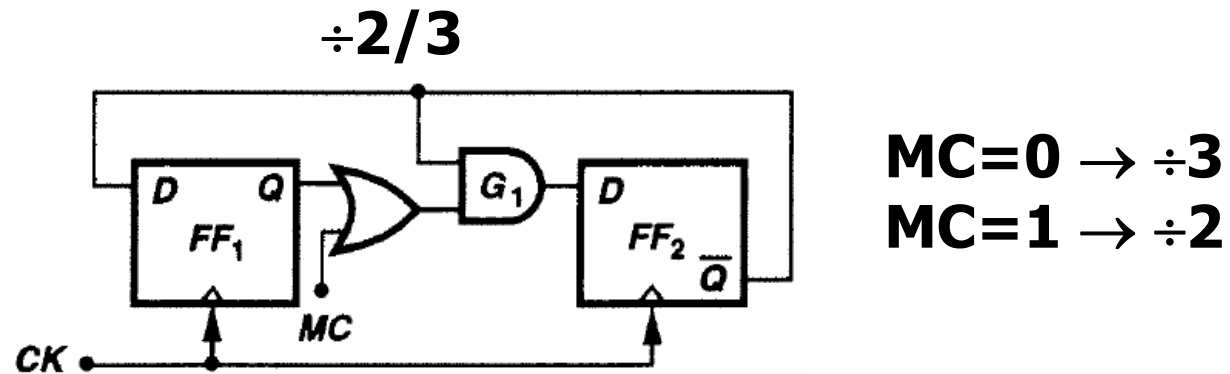
Synchronous ÷3/4

Asynchronous ÷4

- For /15, first prescaler circuit divides by 3 once and 4 three times during the 15 cycles

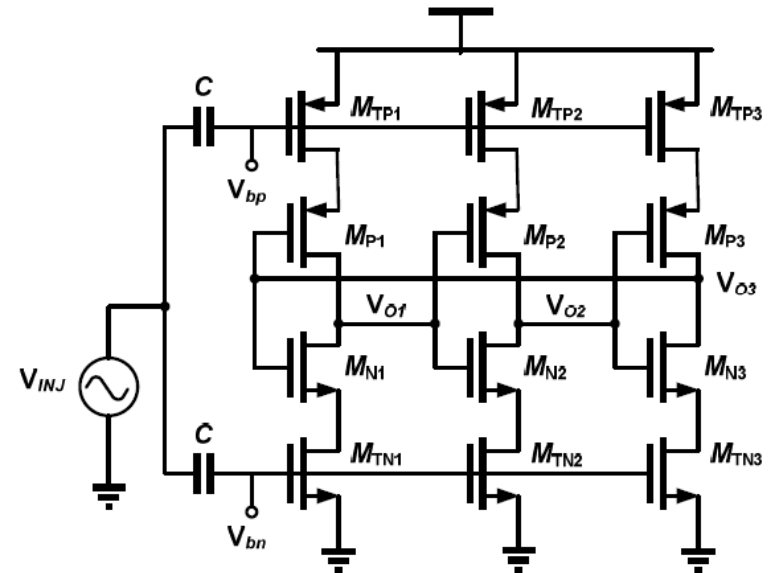# Injection-Locked Frequency Dividers

LC-oscillator type (/2)

$$v_O = V_O \cos(\omega_O t + \varphi)$$

$$i_I = I_I \cos(2\omega_O t) + I_{DC}$$

$$v_I = V_I \cos(2\omega_O t)$$

Ring-oscillator type (/3)

[**Verma JSSC 2003, Rategh JSSC 1999**]   [**Lo CICC 2009**]

- Superharmonic injection-locked oscillators (ILOs) can realize frequency dividers
- Faster and lower power than flip-flop based dividers
- Injection locking range can be limited