Jitter Optimization Based on Phase-Locked Loop Design Parameters

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***Abstract*—This paper investigates the effects of varying phase-locked loop (PLL) design parameters on timing jitter. The noise due to voltage-controlled oscillator (VCO), input clock and buffering clock are considered. First, a closed-form equations are derived that relate PLL output clock jitter to parameters of a second-order PLL, i.e., damping factor and bandwidth. Then the second-order analysis is extended to a third-order PLL with inherent feedback/sampling delay. The sensitivity study clearly illustrates how to select design parameters to obtain minimum output jitter. To verify the analysis experimentally, a digitally tunable PLL architecture is designed and fabricated that allows independent adjustment of loop parameters. The design not only demonstrates the agreement between analysis and theory, but also shows an architecture that minimizes jitter.**

***Index Terms*—Jitter, phase noise, phase-locked loops.**

I. Introduction

PHASE-LOCKED loops (PLLs) are widely used in high-speed digital systems to generate low jitter on-chip clocks. Jitter requirements are more and more stringent as system speed increases. Timing jitter has been the subject of numerous studies [1]–[4] which provide many models to predict the jitter of different types of voltage controlled oscillators (VCOs) due to device noise and supply/substrate noise. This paper extends the work by investigating the effect of PLL parameters such as bandwidth and damping factor toward minimizing output clock jitter.

The common design practice for systems with low-noise input clock is to critically damp or overdamp a PLL to minimize peaking in jitter transfer function and to design the loop with the highest possible bandwidth to eliminate the effects of noise sources at the output. Very low bandwidth and high damping factor are commonly used to filter a noisy input clock with a clean oscillator within the PLL. By understanding the sensitivity of jitter to loop parameters, we can refine these common practices in designing low-jitter PLLs. Section II reviews major timing jitter sources and extracts the relationship between the overall rms jitter at the PLL output clock, the power spectral density of each noise source and the correspondent PLL noise transfer function. In Section III, the sensitivity of jitter to PLL damping factor and bandwidth is first derived for second-order loops and then extended to third-order loops. Section IV describes a tunable PLL design that is used to minimize jitter and to verify our analysis.

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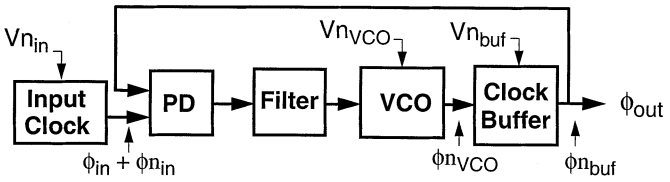

Fig. 1. Noise sources in a PLL.

II. Quantifying Jitter

Phase jitter is defined as the standard deviation, $\sigma_{\Delta\phi}$, of the phase difference between the first cycle and mth cycle of the clock. Timing jitter can be expressed in terms of phase jitter by $\sigma_{\Delta T} = (T/2\pi) \cdot \sigma_{\Delta\phi} = 1/\omega_0 \cdot \sigma_{\Delta\phi}$ where the clock period, T, is $2\pi/\omega_0$. Timing jitter is called short-term jitter for small ΔT ($\Delta T = m \cdot T$) and long-term jitter as ΔT goes to infinity. Prior research in [1] has shown that for an open loop VCO, jitter from random noise sources is proportional to the square root of measurement interval (ΔT), $\sigma_{\Delta T} \approx \kappa\sqrt{\Delta T}$, where the proportionality constant, κ, is a time-domain figure of merit which depends on the VCO design. For the case of a first-order PLL with bandwidth of $f_{-3\,\mathrm{dB}}$, the output clock jitter due to VCO noise is calculated in [1] as $\sigma_{\Delta T\to\infty} = \sigma_T = \kappa\sqrt{1/(2\pi f_{-3\,\mathrm{dB}})}$. The first-order loop roughly approximates an overdamped second-order PLL. The tracking jitter, σ_{tr}, is a commonly used metric for a PLL output clock. It is measured as the phase difference between a clean reference clock and the PLL output clock and is related to timing jitter by $\sigma_{\mathrm{tr}} = \sigma_T/\sqrt{2}$ at very large ΔT [1].

In this paper, we extend the analysis to different noise sources and to any second-order and third-order PLL loop parameters. This research includes the three primary noise sources: input clock noise (Vn_{in}), VCO noise (Vn_{VCO}) and clock buffer noise (Vn_{buf}) (shown in Fig. 1). The transfer functions from each noise source to the output shape the noise. As a result Vn_{in}, Vn_{VCO}, and Vn_{buf} are filtered through lowpass, bandpass, and highpass filters, respectively.

The filtering is included in the timing jitter by expressing $\sigma_{\Delta T}$ as a function of phase noise power spectral density (psd) $S_\phi(f)$, as derived in [2].

$$\sigma_{\Delta T}^2 = \frac{8}{\omega_0^2}\int_0^\infty S_\phi(f)\sin^2(\pi f \Delta T)df. \tag{1}$$

At long delays ($\Delta T \to \infty$), the expression is simplified as

$$\sigma_T^2 = \frac{2}{\omega_0^2}R_\phi(0) = \frac{4}{\omega_0^2}\int_0^\infty S_\phi(f)df. \tag{2}$$

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Equation (2) suggests that reducing the area under the phase noise psd lowers jitter at the output. Under closed-loop condition, the psd of each noise source is calculated by $S_\phi(f) = S_{\phi\,\mathrm{closed}}(f) = S_{\phi\,\mathrm{open}}(f)\cdot|Hn_i(j2\pi f)|^2$ where $|Hn_i(j2\pi f)|^2$ is the square magnitude of noise transfer function (NTF) from each input phase noise to PLL output phase, i.e., $(\phi_{\mathrm{out}}/\phi n_i)(f) = Hn_i(j2\pi f)$.

Open-loop noise psd of a clock source is equal to $S_{\phi\,\mathrm{open}}(f) = N_{\mathrm{in}}/f^2$. N_{in} is $K_0^2 \cdot e_n^2/2$ [7] where K_0 (Hz/V) represents the gain of the clock source oscillator and e_n ($\mathrm{V}/\sqrt{\mathrm{Hz}}$) is a white noise source. N_{in} is related to κ through $\kappa = \sqrt{N_{\mathrm{in}}}/(\omega_0/2\pi)$ [7]. Being a clock source as well, the VCO has a similar noise that can be characterized using N_{vco} to represent the noise sources in the VCO. For the buffer, open-loop noise psd is calculated by $S_{\phi\mathrm{open}}(f) = N_{\mathrm{buf}}/(f^2/f_{\mathrm{buf}}^2 + 1)$ where f_{buf} is the buffer 3-dB bandwidth (typically much larger than PLL bandwidth) and $N_{\mathrm{buf}} = (K_{\mathrm{delay}} \cdot \omega_0)^2 \cdot e_n^2/2$. K_{delay} (s/V) represents buffer delay variation to voltage noise. Multiplying K_{delay} by clock frequency (ω_0) converts delay to phase variation due to noise.

The total noise psd at the output is given by

$$S_{\phi\mathrm{closed}}(s) = \frac{N_{\mathrm{in}}}{f^2}\cdot|Hn_{\mathrm{in}}(j2\pi f)|^2 + \frac{N_{\mathrm{VCO}}}{f^2} \cdot|Hn_{\mathrm{VCO}}(j2\pi f)|^2 + \frac{N_{\mathrm{buf}}}{\frac{f^2}{f_{\mathrm{buf}}^2}+1}\cdot|Hn_{\mathrm{buf}}(j2\pi f)|^2. \tag{3}$$

Note that this analysis assumes white noise sources. The same analysis can be done for colored noise sources (such as supply and substrate noise) by replacing $e_n^2/2$ by $e_n^2/2\cdot 1/(f^2/f_{\mathrm{noise}}^2 + 1)$ where f_{noise} is the 3-dB bandwidth of the noise.

III. PLL Noise Transfer Function (NTF)

The second-order model of PLL with charge pump type of filter is shown in Fig. 2. The NTFs for each of noise sources are calculated as

$$\begin{aligned} Hn_{\mathrm{in}}(s) &= \frac{\phi_{\mathrm{out}}}{\phi n_{\mathrm{in}}} \\ &= \frac{K_{\mathrm{loop}}RCs + K_{\mathrm{loop}}}{s^2 + K_{\mathrm{loop}}RCs + K_{\mathrm{loop}}} \\ &= \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \\ Hn_{\mathrm{VCO}}(s) &= Hn_{\mathrm{buf}}(s) \\ &= \frac{\phi_{\mathrm{out}}}{\phi n_{\mathrm{VCO,buf}}} \\ &= \frac{s^2}{s^2 + K_{\mathrm{loop}}RCs + K_{\mathrm{loop}}} \\ &= \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \end{aligned} \tag{4}$$

where $K_{\mathrm{loop}} = I_{CP}/(2\pi C)K_{PD}K_{\mathrm{VCO}}$, $\omega_n = \sqrt{K_{\mathrm{loop}}}$ and $\zeta = \sqrt{K_{\mathrm{loop}}}RC/2$.[1]

[1]The loop multiplication factor is one.

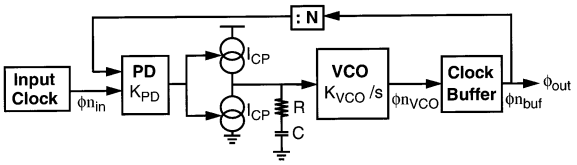

Fig. 2. A conventional PLL.

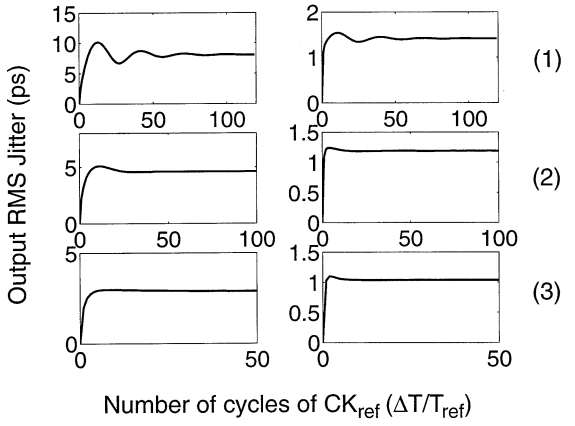

Fig. 3. Short-term jitter behavior with different $f_{-3\,\mathrm{dB}}$ and ζ due to (a) VCO and (b) clock buffering noise. ((1) $f_{-3\,\mathrm{dB}} = 5.5\%f_{\mathrm{ref}}$, $\zeta = 0.2$ (2) $f_{-3\,\mathrm{dB}} = 6.4\%f_{\mathrm{ref}}$, $\zeta = 0.65$ (3) $f_{-3\,\mathrm{dB}} = 11.4\%f_{\mathrm{ref}}$, $\zeta = 1.63$).

The total jitter at the PLL output clock is calculated by substituting (3) and (4) in (1). To study the effect of each noise source on jitter, we first consider the VCO noise term

$$\sigma_{\Delta T}^2 = \frac{4N_{\mathrm{VCO}}}{\omega_0^2}\int_{-\infty}^{\infty}\left|\frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}\right|_{s=jw}^2 \frac{\sin^2(\pi f\Delta T)}{f^2}df. \tag{5}$$

The equation is simplified as follows (see Appendix A):

$$\sigma_{\Delta T}^2 = \frac{4\pi^2 N_{\mathrm{VCO}}}{\omega_0^2}\int_{-\infty}^{\infty}\left[x\left(t+\frac{\Delta T}{2}\right) - x\left(t-\frac{\Delta T}{2}\right)\right]^2 dt \tag{6}$$

where $x(t)$ is inverse Fourier transform of $s/(s^2 + 2\zeta\omega_n s + \omega_n^2)|_{s=j\omega}$. For damping factors smaller and larger than one, the jitter expression is shown in (7) at the bottom of the next page, where $\omega_d = \omega_n \cdot \sqrt{1-\zeta^2}$, $\cos\theta = \sqrt{1-\zeta^2}$, $a, b = \zeta\omega_n \mp \omega_n \cdot \sqrt{\zeta^2 - 1}$, $\alpha = -a/(b-a)$ and $\beta = b/(b-a)$.

Fig. 3(a) shows the short-term jitter behavior for different damping factors. For ΔT of within a few cycles, jitter accumulates as with an open-loop VCO. As ΔT increases, jitter behaves similarly to the time-domain step response of the PLL output phase with similar dependence on the damping factor and bandwidth. The lower damping factor appears as more peaking in short-term jitter. For small short-term jitter, damping factor should be designed to be equal to or greater than one to avoid ringing in the jitter response. At large ΔT, long-term jitter converges to final value of $\kappa \cdot \sqrt{1/(2\zeta\omega_n)}$. Note that this result is similar to the result derived in [6]. The sensitivity of jitter to loop parameters can be illustrated graphically. Sweeping loop bandwidth ($f_{-3\,\mathrm{dB}}$) (or equivalently $f_n = \omega_n/(2\pi)$) while ζ

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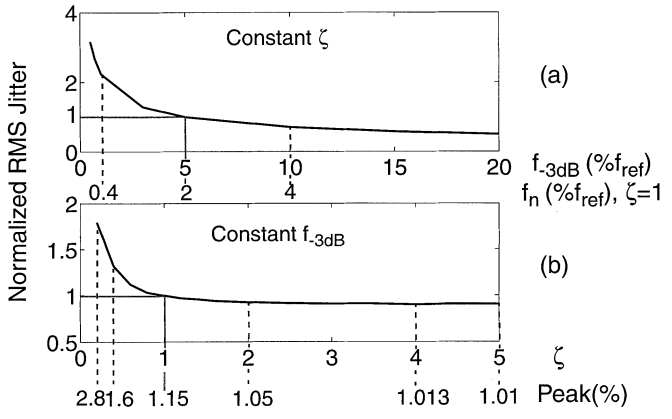

Fig. 4. Long-term jitter (due to VCO noise) sensitivity to: (a) loop bandwidth and (b) loop damping factor.

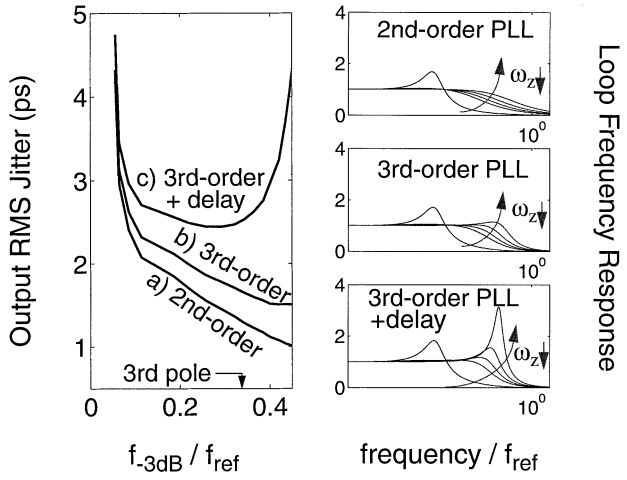

Fig. 5. Comparison of long-term jitter (due to VCO noise) in: second, third order loop without loop delay and with loop delay.

is constant results in Fig. 4(a) in which jitter is reduced proportional to $1/\sqrt{f_{-3\text{ dB}}}$. Fig. 4(b) illustrates the effects of varying ζ (or peaking in the frequency response) with constant $f_{-3\text{ dB}}$. In the plot, f_n is adjusted to maintain the same $f_{-3\text{ dB}}$ while sweeping ζ. For ζ less than one (or greater peaking in frequency response), long-term jitter is proportional to $1/\sqrt{\zeta}$, but the sensitivity reduces as ζ increases. For ζ greater than 2 with constant loop bandwidth, long-term jitter is relatively constant, independent of ζ value.

So far we investigated the effect of VCO noise using an ideal second-order PLL without considering the effects of the third-order pole or the inherent loop delay in a sampled system. In many PLLs, a third-order pole is often included to filter control voltage ripple. For high loop bandwidths, this pole degrades the phase margin and causes peaking in the frequency response. A similar frequency response peaking occurs when accounting for the delay in the feedback loop and the sampled-nature of the loop. These nonidealities can be taken into account using (2) with a more accurate NTF.

We included these nonidealities into a MATLAB analysis. Fig. 5 compares the output long-term jitter as bandwidth is increased for a second-order loop (curve-a), third-order loop without loop delay (curve-b) and third-order loop with loop delay (curve-c). In the plot, the third-order pole is kept constant while the zero frequency is decreased which simultaneously increases the loop crossover frequency, ω_c and the damping factor. The plots on the right illustrate the loop frequency responses for a second-order, third-order PLL without and with loop delay as zero frequency (ω_z) is decreased. Curve-a shows the anticipated decrease in jitter due to the higher bandwidth and damping factor. In curve-b, as the loop bandwidth nears the third-order pole, the peaking in frequency response increases due to phase margin degradation. Thus jitter is roughly flattened at bandwidths higher than third pole due to the opposing effect of peaking and bandwidth on jitter. Accounting for loop delay (curve-c), the jitter increases at high bandwidth due to the additional peaking in the NTF from more phase margin degradation. [2] A minimum exists and is modestly flat over a significant range of loop parameter variations. This implies that a loop designed near this minimum has an output jitter that is relatively insensitive to the parameter variations that may be due to process, voltage, and temperature (PVT).

Analysis of the minimum indicates that it depends on all four variables (loop gain, zero frequency, third-order pole frequency and loop delay) because each contribute to phase margin degradation. The phase margin (PM) for a third-order PLL with loop delay of t_{delay} can be approximated with:

$$\text{PM} = a\tan\left(\frac{\omega_c}{\omega_z}\right) - a\tan\left(\frac{\omega_c}{\omega_{p3}}\right) - \frac{360^\circ}{2\pi}\cdot\omega_c\cdot t_{\text{delay}} \quad (8)$$

where ω_z and ω_{p3} are the zero and the third-pole frequencies. The analytical results show that jitter is minimum with PM between 30° and 45°. Consequently, the PLL bandwidth at minimum jitter reduces as third-pole frequency decreases or loop delay increases as shown in Fig. 6. This result counters common practice of designing with large phase margins and damping factor of $1/\sqrt{2}$.

[2]To the first order, using the loop delay accounts for the effect of the sampled system. The measurement results of Section IV matches the simulated results from this model better than that from a z-domain model using impulse invariant transformation.

$$\sigma^2_{\Delta T} = \underbrace{\left(\frac{4\pi^2 N_{\text{VCO}}}{\omega_0^2}\right)}_{\kappa^2}\cdot\begin{cases}\dfrac{1}{2\zeta\omega_n} + \dfrac{e^{-\zeta\omega_n\Delta T}}{2\left(1-\zeta^2\right)}\cdot\left(\dfrac{\sin\left(\omega_d\Delta T+\theta\right)}{\omega_n} - \dfrac{\cos\left(\omega_d\Delta T\right)}{\zeta\omega_n}\right), & \zeta<1\\ \dfrac{1}{2\zeta\omega_n} - e^{-a\Delta T}\left(\dfrac{2\alpha\beta}{a+b}+\dfrac{\alpha^2}{a}\right) - e^{-b\Delta T}\left(\dfrac{2\alpha\beta}{a+b}+\dfrac{\beta^2}{b}\right), & \zeta\geq 1\end{cases} \quad (7)$$

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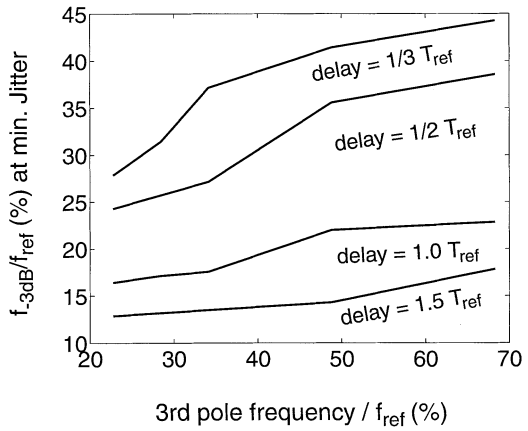

Fig. 6. PLL bandwidth (at minimum jitter) as a function of third pole frequency and PLL delay.

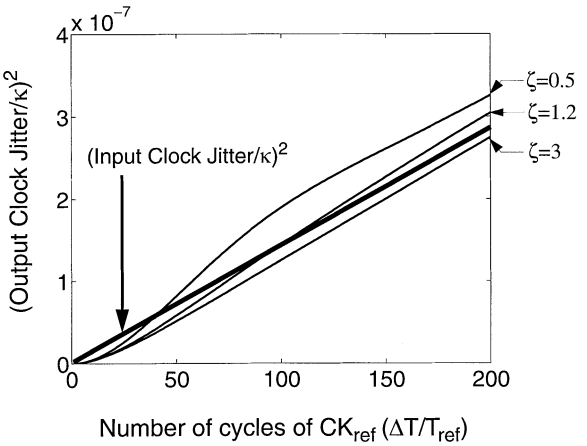

Fig. 7. Output clock jitter (due to input clock noise) behavior vs. input clock jitter behavior.

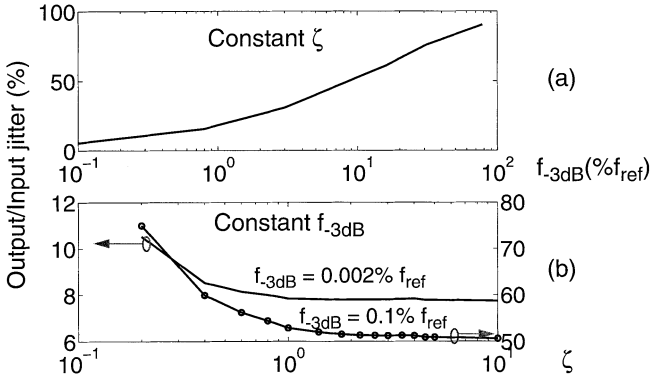

Fig. 8. Output to input jitter ratio sensitivity of a second-order loop to: (a) loop bandwidth and (b) loop damping factor.

Noise from the buffering and the input clock can be similarly analyzed using the corresponding closed-loop noise psds. The final equations are summarized in Appendix B. Jitter behavior due to buffer noise over different time intervals has similar behavior to VCO noise except for small ΔT where jitter is increased sharply due to the high-pass filtering of the buffer NTF. Fig. 3(b) illustrates the output jitter for different ΔT with different damping factors.

To compare buffer noise magnitude with VCO noise, the jitter values are extracted from (7) and (14) for $\Delta T \to \infty$. The ratio of the buffer noise variance with VCO noise variance is

$$\frac{\sigma_{\rm buf}^2}{\sigma_{\rm VCO}^2} \approx \frac{\left(\frac{N_{\rm buf}}{\omega_0^2}\right)\cdot\omega_{\rm buf}}{\left(4\pi^2\cdot\frac{N_{\rm VCO}}{\omega_0^2}\right)\cdot\left(\frac{1}{2\zeta\omega_n}\right)} = \frac{m\cdot K_{\rm delay}^2\cdot\omega_0^2\cdot\omega_{\rm buf}\cdot\frac{e_{n_{\rm buf}}^2}{2}}{4\pi^2\cdot K_{\rm VCO}^2\cdot\left(\frac{1}{2\zeta\omega_n}\right)\cdot\frac{e_{n_{\rm VCO}}^2}{2}} \tag{9}$$

where m is the number of buffer stages. For a ring oscillator with the same delay elements as the buffering, the $K_{\rm VCO}$ can be expressed in terms of $K_{\rm delay}$, $K_{\rm VCO} = K_{\rm delay}\cdot -1/(2n\cdot t_d^2)$ where n is the number of stages in ring oscillator VCO and t_d is the delay of each stage. This simplifies (8) to

$$\frac{\sigma_{\rm buf}^2}{\sigma_{\rm VCO}^2} \approx \frac{m\zeta\omega_n}{nf_{\rm osc}}\cdot\frac{e_{n_{\rm buf}}^2}{e_{n_{\rm VCO}}^2}. \tag{10}$$

With $\omega_n = 0.2f_{\rm osc}$ and $\zeta = 1$, in order for the noise contribution of the buffer to be less than that of the VCO, either $m < 5n$ or the VCO element must have $5\times$ lower noise sensitivity than the buffer elements. With lower loop bandwidths, buffer noise contribution decreases proportionally.

Since the long-term jitter behavior due to buffer and VCO noise are similar, the jitter analysis results (due to VCO noise) for higher-order sampled PLLs are applicable to the buffer noise as well.

For the effect of the PLL filtering on a noisy input clock, the analytical results (15) for a second-order PLL show that the output clock timing jitter is suppressed at small ΔT and asymptotically approaches a value, $\kappa\sqrt{1/(2\zeta\omega_n)}$, greater than the input jitter at large ΔT. The shape and final value depend on the bandwidth and the damping factor. Fig. 7 illustrates the behavior of output clock jitter for different damping factors with constant bandwidth. The figure also includes the behavior of input clock jitter. The ΔT at which the jitter exceeds the input jitter (the crossover time, $\Delta T_{\rm cr}$) is larger for higher damping factors and lower bandwidths. For most clock source PLLs, jitter of the overall system is suppressed as long as $\Delta T_{\rm cr}$ is longer than the response time of any subsequent PLLs locking to the output clock. The jitter analysis due to noisy input clock not only confirms the common practice design but also elaborates the roles of bandwidth and damping factor on the output jitter. Fig. 8(a) shows how the output jitter (at $\Delta T = 100$ cycles) is reduced as bandwidth is decreased. Fig. 8(b) demonstrates that the output jitter (at $\Delta T = 100$ cycles) is reduced as damping factor is increased for two different bandwidths. Similar to VCO noise analysis, output jitter is roughly constant for damping factor greater than 2. For instance, for output jitter to be less than 0.1 input jitter at $\Delta T > 100$ cycles, the PLL should be designed with a damping factor greater than 2 and bandwidth less than 0.002% of operating frequency.

To investigate the effects of the loop nonidealities, the jitter of an ideal second-order loop is compared to that of a third-order PLL with loop delay. To better show the comparison, we assume white noise at PLL input phase instead of $1/f^2$ noise (of a noisy input clock). Fig. 9 illustrates the output long-term jitter

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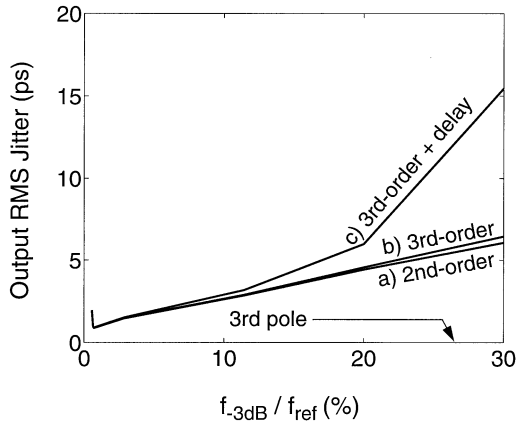

Fig. 9. Comparison of long-term jitter (due to white noise at PLL input) in: (a) second- and (b) third-order loop, without loop delay, and (c) third-order with loop delay.

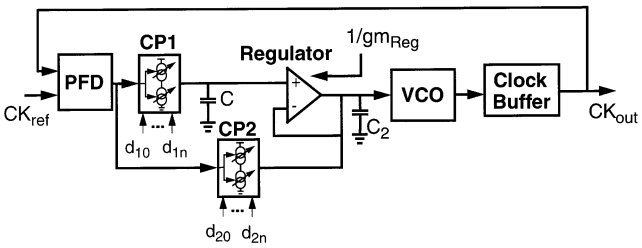

Fig. 10. Tunable and adaptive bandwidth PLL.

while the zero frequency is decreased which simultaneously increases the loop cross-over frequency and the damping factor. Jitter decreases initially for all three curves due to the lower frequency-response peaking where the bandwidth changes only slightly. As the zero frequency decreases further, the bandwidth increases causing jitter to increase. At bandwidths close to third pole, the peaking is increased due to phase margin degradation which results in more jitter increase in curve-b compared with curve-a. Accounting for loop delay (curve-c), additional peaking in the NTF from more phase margin degradation manifests the sharp jitter increase.

Clearly, a tradeoff is present between input noise and the noise from within the loop. By knowing the amount of noise, our model can be used to properly optimized loop parameters to minimize jitter. Since input noise is not easily predetermined, as part of the investigation, we design a PLL with adjustable loop parameters so that the loop can be adapted to improve performance significantly under a variety of input noise conditions.

IV. Experimental Methods and Results

A tunable and adaptive bandwidth PLL clock generator (Fig. 10) is designed and fabricated in 0.25-μm CMOS technology based on the design in [5]. The design employs two digitally controllable charge pump currents to adjust the loop parameters. The natural frequency varies proportional to $\sqrt{I_{CP1}}$. The stabilizing loop resistor is equal to $R = 1/(gm_{\rm Reg}) \cdot I_{CP2}/I_{CP1}$ where $gm_{\rm Reg}$ is the output resistance of the regulator; thus ζ is proportional to $I_{CP2}/\sqrt{I_{CP1}}$. Varying I_{CP1} or I_{CP2} does not change the position of the third-order pole. The PLL die photogragh is shown in Fig. 11 where the area overhead due to digital controller logic is approximately 15% of PLL core area.

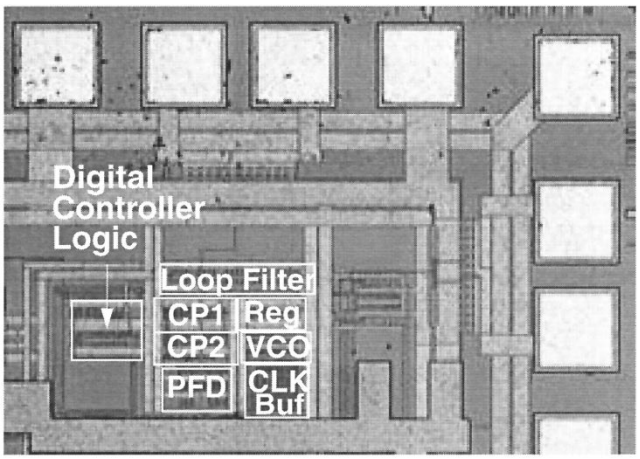

Fig. 11. PLL die photogragh.

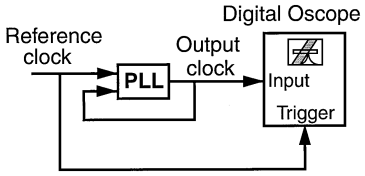

Fig. 12. Measurement technique in time domain, referenced to reference clock.

TABLE I
Tracking Jitter (in ps) for Different Loop Parameters (@ 700-MHz Reference Clock)

I_{CP2} \ I_{CP1}	$2.I_1$ rms jitter	$3.I_1$ rms jitter	$4.I_1$ rms jitter	$5.I_1$ rms jitter	$6.I_1$ rms jitter
$2.I_2$	4.49	4.67	5	5.57	6.8
$3.I_2$	3.4	3.41	3.45	3.57	3.76
$4.I_2$	2.8	2.81	2.96	2.87	2.99
$5.I_2$	2.58	2.54	2.6	2.52	2.55
$6.I_2$	2.37	2.35	2.3	2.35	2.37
$7.I_2$	2.24	2.2	2.17	2.23	2.18
$8.I_2$	2.14	2.1	2.08	2.1	2.1
$9.I_2$	2.04	2	2.03	1.99	2.03
$10.I_2$	2.01	1.97	1.9	1.99	1.93
$16.I_2$	1.88	1.87	1.87	1.8	1.85
$17.I_2$	1.9	1.8	1.72	1.73	1.84
$18.I_2$	1.91	1.88	1.73	1.71	1.85
$19.I_2$	1.89	1.89	1.77	1.73	1.88
$21.I_2$	1.94	1.86	1.73	1.72	1.83
$24.I_2$	2.03	1.99	1.8	1.77	2
$32.I_2$	2.4	2.1	2.16	2.21	2.32

To observe only VCO noise, a clean signal generator (with rms jitter of less than 1 ps) produces the reference clock and the design uses only a few buffer stages in the feedback so that the buffer noise is small compared to VCO noise.

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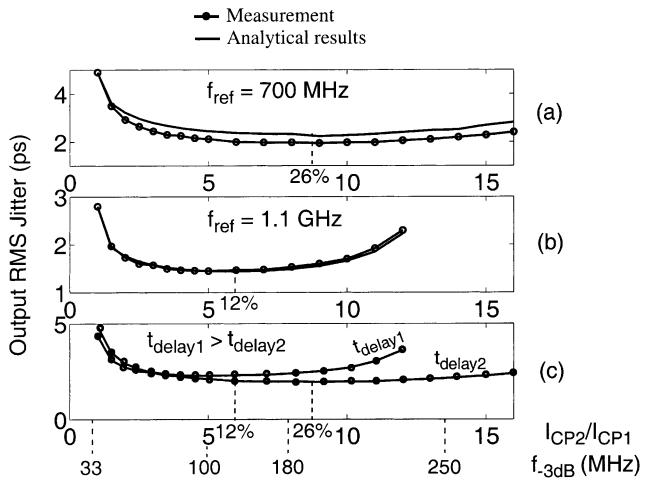

Fig. 13. Measured and calculated tracking jitter for different I_{CP2} at constant I_{CP1}.

To verify the presence of minimum tracking jitter due to VCO noise, the first charge pump current (I_{CP1}) is kept constant (i.e., $K_{\rm loop}$ = constant) while the second charge pump current (I_{CP2}) is swept (i.e., ω_z is decreased). For each value of I_{CP2}, the rms tracking jitter of PLL output clock is measured based on the configuration of Fig. 12. The same measurement is repeated when I_{CP1} is varied. Table I summarizes some of the results at reference clock equal to 700 MHz where I_1 and I_2 are constant currents. Fig. 13(a) and (b) show the measured and calculated jitter for one set of measurements repeated for two reference clock frequencies. As seen in the figures, the measured jitter corresponds closely with the analytical results and there is a minimum jitter with a low sensitivity to loop parameter variations. For example, $+/-20\%$ of bandwidth variation increases jitter by less than 5%. In each set of measurements, jitter initially decreases because the peaking decreases (or ζ grows linearly) with I_{CP2} and the $f_{-3\ \rm dB}$ increases with the decreasing zero frequency (f_n is held constant). As I_{CP2} increases, the cross-over frequency approaches the third-order pole and degrades the phase margin. Jitter reaches a relatively flat minimum before increasing due to the loop delay (approximately 0.47 ns). Increasing reference clock frequency from 700 MHz to 1.1 GHz in our adaptive bandwidth PLL, effectively measures the result of changing the loop's feedback delay from 1/3 to 1/2 of the reference clock period. The bandwidth at minimum jitter is reduced from 26% to 12% of reference clock [Fig. 13(c)].

The short-term jitter sensitivity to PLL parameters is also verified. The short-term jitter is calculated with the analytical model. The time domain figure of merit of the VCO is equal to $\kappa \approx 5.4e-8\sqrt{s}$ at 700-MHz oscillating frequency. The 3-dB bandwidth and peaking used for the model are first calculated through circuit simulations and then verified with direct measurements. The test setup that measures the loop parameters is shown in Fig. 14. A radio frequency (RF) signal is added to the input clock. The output clock jitter is measured over different RF frequencies. The measured PLL loop transfer functions with their effective $f_{-3\ \rm dB}$ and peaking (see Appendix C) are shown in Fig. 15 for four different values of I_{CP2} with constant I_{CP1}.

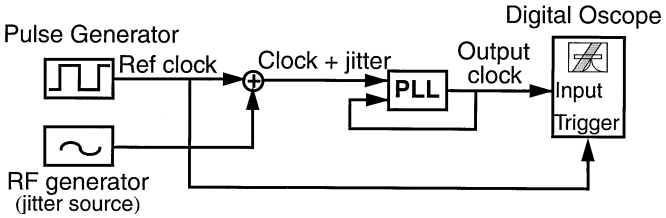

Fig. 14. Measurement technique for calculating PLL loop transfer function.

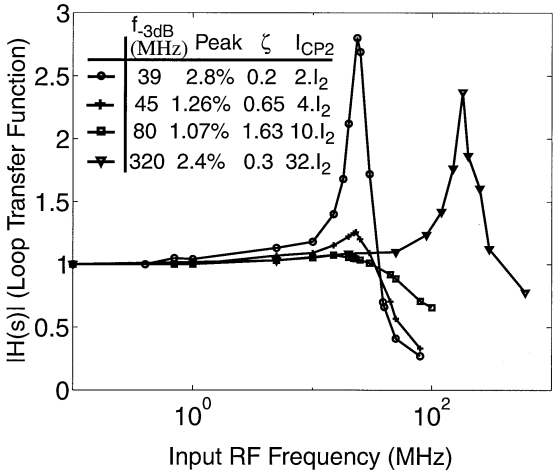

Fig. 15. Measured PLL loop transfer function (@ 700-MHz reference clock) at a constant I_{CP1}.

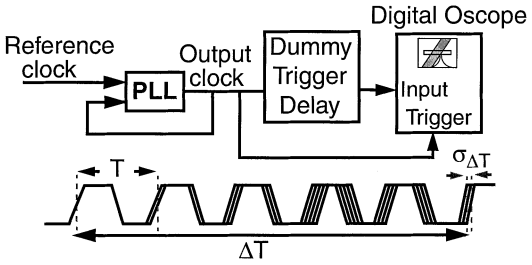

Fig. 16. Measurement technique in time domain, referenced to output clock.

The rms jitter is measured over different time interval (ΔT) for each of the four different settings of loop parameters. The measurement uses a self-referenced technique shown in Fig. 16. The delay in the test setup is critical to compensate for the triggering delay of an oscilloscope. Fig. 17 shows the measured and calculated jitter. A slight timing shift between predicted and measured jitter is present because of time uncertainty due to the delay of input trigger and dummy trigger delay at the input of oscilloscope.

Finally, to verify the jitter analysis due to input clock noise, we apply a free running VCO at 700 MHz as the reference clock of the PLL. A white noise source is injected to the control voltage of the free running VCO so that the input clock noise is the dominant noise source. As the baseline measurement, we measure the rms jitter of this reference input over different time interval (ΔT) based on the self-referenced technique. We also measure the PLL output rms jitter while varying ΔT for three different loop parameters. The measurement results in Fig. 18(a) demonstrate the same behavior to the analytical results Fig. 18(b) with approximately the same $\Delta T_{\rm cr}$.

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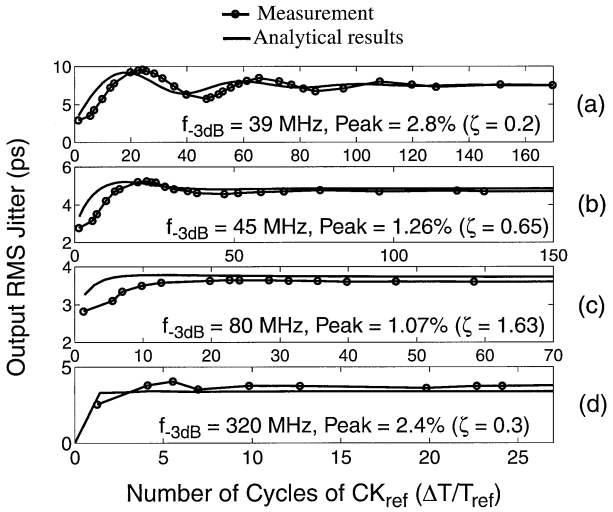

Fig. 17. Measured and calculated short-term jitter (@ 700-MHz reference clock) for four different loop parameters.

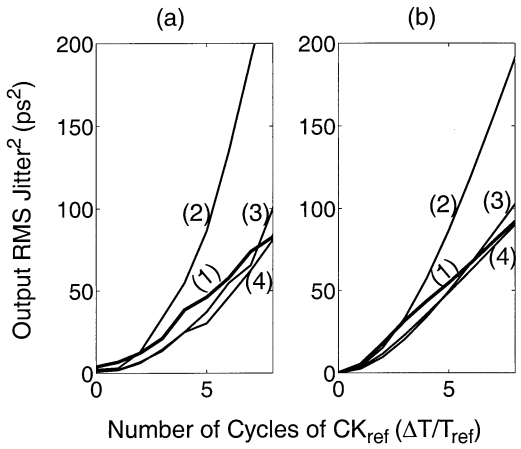

Fig. 18. Output jitter (due to input clock noise) behavior for three different PLL loop parameters: (a) measurement results and (b) analytical results. (1) Input jitter; (2) $\zeta = 0.2$, $f_{-3\,\mathrm{dB}} = 39$ MHz; (3) $\zeta = 0.65$, $f_{-3\,\mathrm{dB}} = 45$ MHz; (4) $\zeta = 1.63$, $f_{-3\,\mathrm{dB}} = 80$ MHz.

V. Conclusion

This paper investigates the role of PLL parameters on timing jitter. Several common noise sources have been included in the analysis. We develop an intuition for designing low-jitter PLLs both by deriving a closed-form solution for a second-order loop and by plotting the sensitivity to various loop parameters for higher order loops. A PLL with digitally-controllable loop parameters is designed that can optimize jitter performance. Furthermore, the loop serves as a test bench to verify our analysis.

The analysis shows a simple expression for long-term jitter due to VCO and buffering noise to the damping factor and natural frequency. We derive an expression that relates the jitter contribution of clock buffering (in the feedback) and VCO to the same parameters. We validate the common design practice of using high loop bandwidth to reduce VCO-induced jitter. However, to minimize jitter, we find that accounting for the loop delay in the phase margin is critical. Interestingly, this minimum is very insensitive to PVT and parameter variations making such a design robust. For applications that require small short-term jitter (i.e., short distance links and block to block interconnect), an underdamped loop can result in much higher short-term rms jitter. For applications that filters input jitter, our modeling shows that very low bandwidths (0.002% f_{osc}) are necessary to reduce noise by a factor of 10 while a damping factor greater than 2 is sufficient.

Appendix A

Relationship Between Output Jitter and NTF

Timing jitter is expressed in terms of noise power spectral density

$$\sigma^2_{\Delta T} = \frac{4}{\omega_0^2}\int_{-\infty}^{\infty} S_\phi(f)\sin^2(\pi f \Delta T)df$$

or

$$\sigma^2_{\Delta T} = \frac{4}{\omega_0^2}\int_{-\infty}^{\infty} S_{\phi_{\mathrm{open}}}(f)\left|Hn_i(j2\pi f)\right|^2\sin^2(\pi f \Delta T)df. \tag{11}$$

To simplify the equation, Parseval's relation is used, $1/(2\pi)\int_{-\infty}^{\infty}|Z(\omega)|^2 d\omega = \int_{-\infty}^{\infty}|z(t)|^2 dt$. To do so, $z(\omega)$ is expressed as

$$Z(\omega) = X(\omega)\cdot Y(\omega) = \underbrace{H_{\mathrm{open}}(j\omega)\cdot Hn_i(j\omega)}\cdot\underbrace{j\omega\cdot\frac{\sin\left(\omega\frac{\Delta T}{2}\right)}{\omega}} \tag{12}$$

where $S_{\phi_{\mathrm{open}}}(f) = |H_{\mathrm{open}}(j\omega)|^2$. $z(t)$ is equal to convolution of $x(t)$ and $y(t)$. Since $y(t) = (1/2)\delta(t+\Delta T/2) - (1/2)\delta(t-\Delta T/2)$ where $\delta(t)$ represents dirac's delta function, $z(t) = (1/2)x(t+\Delta T/2) - (1/2)x(t-\Delta T/2)$ where $x(t)$ is the inverse Fourier of $H_{\mathrm{open}}(j\omega)\cdot Hn_i(j\omega)$.

Therefore timing jitter equation is simplified as

$$\sigma^2_{\Delta T} = \frac{4\cdot 2\pi}{\omega_0^2}\int_{-\infty}^{\infty}\frac{1}{4}\left[x\left(t+\frac{\Delta T}{2}\right) - x\left(t-\frac{\Delta T}{2}\right)\right]^2 dt. \tag{13}$$

Appendix B

Relationship Between Output Jitter and Clock Buffering Noise

See (14), at the bottom of the next page, where $\omega_{\mathrm{Buf}} = 2\pi f_{\mathrm{Buf}}$, $\upsilon = (2\zeta\omega_n a - \omega_n^2)/(b-a)$ and $\gamma = (-2\zeta\omega_n b + \omega_n^2)/(b-a)\cdot\omega_d$, θ, a, and b are the same as (7).

Relationship Between Output Jitter and Input Clock Noise

See (15), at the bottom of the next page, where ω_d, θ, a, b, α, and β are the same as (7).

Appendix C

Jitter Estimation by Applying Effective Second-Order Model to any PLLs

Although a complete third-order model of a PLL is needed to understand the jitter contribution of different loop parameters, our analytical results and measurements have found that tracking jitter due to VCO and buffering for a particular design can be easily estimated by simply using the second-order equations. As shown in the jitter analysis of Section III, tracking jitter

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TABLE II
COMPARISON OF ESTIMATED TRACKING JITTER (BY 2ND-ORDER ANALYSIS) WITH MEASURED TRACKING JITTER ($f_{\text{ref}} = 700$ MHz)

f_{-3dB} (MHz)	Peak (%)	f_n (MHz)	ζ	ratio (Fig. 4(a), (b))	estimated rms jitter (ps)	measured rms jitter (ps)
39	1.61	22.4	0.42	1	$\sigma = \kappa/(2.\sqrt{\zeta\omega_n}) = 3.51$	3.67
39	2.73		0.2	1.8/1.38 = 1.3	$\sigma = 1.3\ .\ 3.51 = 4.56$	5
45	1.19	19.5	0.9	1	$\sigma = \kappa/(2.\sqrt{\zeta\omega_n}) = 2.57$	2.83
45	1.31		0.65	1.1/1.02 = 1.07	$\sigma = 1.07\ .\ 2.57 = 2.75$	2.94
26	1.66	15.3	0.4	1	$\sigma = \kappa/(2.\sqrt{\zeta\omega_n}) = 4.35$	4.49
42	1.66		0.4	$\sqrt{26/42} = 0.79$	$\sigma = 0.79\ .\ 4.35 = 3.42$	3.45
30	1.22	13.8	0.8	1	$\sigma = \kappa/(2.\sqrt{\zeta\omega_n}) = 3.25$	3.4
50	1.22		0.8	$\sqrt{30/50} = 0.77$	$\sigma = 0.77\ .\ 3.25 = 2.51$	2.6

(σ_{tr}) is the integral of the noise shaped by the frequency response. The critical parameters that determine the jitter are the $f_{-3\text{ dB}}$ and the peaking in the NTF.

In a higher order loop, the parameters, such as ζ and f_n, cannot be directly applied to the equations for the second-order loop because the resulting frequency response can differ greatly. To still use the equation, for a given frequency response, we find an effective f_n and effective ζ that result in the same bandwidth and peaking. Fig. 4(a) and (b) shows the corresponding $f_{-3\text{ dB}}$ for each value of f_n and the corresponding peaking for each value of ζ. This method is verified by measuring the tracking jitter for the different loop bandwidths and frequency-response peaking. Jitter is calculated for the same parameters using $\sigma_{\text{tr}} = \kappa/\sqrt{2} \cdot \sqrt{1/(2\zeta\omega_n)}$. Table II compares the measured and calculated jitter. By changing only one variable, we express the change in the jitter as a ratio. The ratio can be directly predicted from Fig. 4(a) or (b). The small error between measurement and predicted result is primarily due to the oscilloscope's inherent noise.

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$$\sigma_{\Delta T}^2 = \frac{N_{\text{buf}}}{\omega_0^2} \cdot \begin{cases} \omega_{\text{buf}} + \omega_n \dfrac{1-12\zeta^2}{2\zeta} - e^{-\omega_{\text{buf}}\Delta T}\left(\omega_{\text{buf}} - 4\zeta\omega_n\right) \\ \quad -e^{-\zeta\omega_n\Delta T}\left(-\dfrac{\omega_n \sin\left(\omega_d\Delta T + 3\theta - \pi\right)}{2\left(1-\zeta^2\right)} + \dfrac{\omega_n\cos\left(\omega_d\Delta T\right)}{2\left(1-\zeta^2\right)\zeta} - \dfrac{2\omega_n\sin\left(\omega_d\Delta T + 2\theta\right)}{\sqrt{1-\zeta^2}}\right), & \zeta < 1 \\ \omega_{\text{buf}} + \dfrac{\gamma^2}{a} + \dfrac{v^2}{b} + \dfrac{4v\gamma}{a+b} + \dfrac{4\omega_{\text{buf}}v}{a+\omega_{\text{buf}}} + \dfrac{4\omega_{\text{buf}}\gamma}{b+\omega_{\text{buf}}} - e^{-a\Delta T}\left(\dfrac{2v\omega_{\text{buf}}}{a+\omega_{\text{buf}}} + \dfrac{2v\gamma}{a+b} + \dfrac{v^2}{a}\right) \\ \quad -e^{-b\Delta T}\left(\dfrac{2\gamma\omega_{\text{buf}}}{b+\omega_{\text{buf}}} + \dfrac{2v\gamma}{a+b} + \dfrac{\gamma^2}{b}\right) - e^{-\omega_{\text{buf}}\Delta T}\left(\omega_{\text{buf}} + \dfrac{2v\omega_{\text{buf}}}{a+\omega_{\text{buf}}} + \dfrac{2\gamma\omega_{\text{buf}}}{b+\omega_{\text{buf}}}\right), & \zeta \geq 1 \end{cases} \tag{14}$$

$$\sigma_{\Delta T}^2 = \underbrace{\kappa^2 \cdot \Delta T}_{\text{Input jitter square}} \cdot \begin{cases} 1 + \dfrac{1}{2\zeta\omega_n \cdot \Delta T} + \dfrac{e^{-\zeta\omega_n\Delta T}}{\Delta T} \cdot \left(\dfrac{\sin\left(\omega_d\Delta T + \theta\right)}{2\left(1-\zeta^2\right)\omega_n} - \dfrac{\cos\left(\omega_d\Delta T\right)}{2\left(1-\zeta^2\right)\zeta\omega_n} - \dfrac{2\sin\left(\omega_d\Delta T\right)}{\omega_d}\right), & \zeta < 1 \\ 1 + \dfrac{1}{2\zeta\omega_n \cdot \Delta T} + \dfrac{e^{-a\Delta T}}{\Delta T}\left(\dfrac{2\alpha}{a} - \dfrac{2\alpha\beta}{a+b} - \dfrac{\alpha^2}{a}\right) + \dfrac{e^{-b\Delta T}}{\Delta T}\left(\dfrac{2\beta}{b} - \dfrac{2\alpha\beta}{a+b} - \dfrac{\beta^2}{b}\right) & \zeta \geq 1 \end{cases} \tag{15}$$

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