A 0.6 mW/Gb/s, 6.4–7.2 Gb/s Serial Link Receiver Using Local Injection-Locked Ring Oscillators in 90 nm CMOS

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***Abstract*—This paper describes a quad-lane, 6.4–7.2 Gb/s serial link receiver prototype using a forwarded clock architecture. A novel phase deskew scheme using injection-locked ring oscillators (ILRO) is proposed that achieves greater than one UI of phase shift for multiple clock phases, eliminating phase rotation and interpolation required in conventional architectures. Each receiver, optimized for power efficiency, consists of a low-power linear equalizer, four offset-cancelled quantizers for 1:4 demultiplexing, and an injection-locked ring oscillator coupled to a low-voltage swing, global clock distribution. Measurement results show a 6.4–7.2 Gb/s data rate with BER $< 10^{-12}$ across 14 cm of PCB, and also an 8.0 Gb/s data rate through 4 cm of PCB. Designed in a 1.2 V, 90 nm CMOS process, the ILRO achieves a wide tuning range from 1.6–2.6 GHz. The total area of each receiver is 0.0174 mm^2, resulting in a measured power efficiency of 0.6 mW/Gb/s.**

***Index Terms*—Injection-locked oscillator, receiver, serial link.**

I. Introduction

THE demand for massively parallel, high speed serial links has recently intensified due to the large amount of off-chip bandwidth required for future multi-core processing and networking applications [1]–[3]. For example, microprocessor industry standards such as Hyper Transport [4] and Quick Path [5] require tens of high-speed serial links with a combined bandwidth greater than 200 Gb/s. In addition, recent chipsets for networking switches require off-chip I/O bandwidths of 2.4 Tb/s [3]. Due to the continual scaling of transistors in future CMOS processes, today's state-of-the art serial links can achieve tens of Gb/s per pin [6]–[8]. While such bandwidth/pin is an important consideration for these next generation applications, energy efficiency per link is the critical metric as there may exist tens to hundreds of these links on a single chip [1], [10].

In contrast to legacy backplane applications that exhibit channel losses greater than 20 dB at Nyquist frequencies [11], these future applications may optimize transmission line characteristics for better signal integrity (i.e. better connectors and shorter distances), such that channel losses are moderate and therefore do not require complex equalization [9]. Therefore, the goal for these short-haul, highly parallelized, chip-to-chip signaling is to achieve high power efficiency (mW/Gb/s) while requiring only minimal equalization power.

Recent serial link receivers have shown significant improvements in power efficiency by focusing on reducing dynamic clock power using resonantly-tuned LC oscillators, both in global clock distribution [9], [12] and local clock demultiplexing [8], [13]. In this paper, we present a multi-channel serial link receiver architecture that exhibits further improvements in dynamic clock power consumption by implementing a low-voltage swing, global clock distribution to multiple link locations, where locally-tapped, injection-locked ring oscillators (ILRO) are used to generate tunable quadrature sampling clocks for receiver demultiplexing [14].

The overview of this paper is as follows. Section II describes the architectural considerations for receiver clocking and data recovery (CDR). Next, in Section III, while most previous analyses of injection-locked oscillator are only applicable to LC oscillators [15]–[18], we propose new analytical equations that enable the understanding of injection-locked, nonharmonic ring oscillators, including the locking range, phase deskew ability, and jitter performance. Details of the receiver circuit implementation are described in Section IV. Section V provides the measurement results of the test chip, ending with the conclusion in Section VI.

II. Receiver Architecture Overview

Embedded clock and forwarded clock architectures are the two major CDR architectures for multi-Gb/s transceivers. In embedded clock architecture, the clock is directly recovered from the incoming data such that no extra clocking channel is required. Therefore, the jitter of the recovered clock will track that of the data within the CDR loop bandwidth. If there are multiple embedded clock serial links, each can work independently from separate frequency references. However, recovering clock from the data typically requires 2× oversampling, resulting in considerable overhead in power consumption [19].

Compared with the embedded clock architecture, forwarded clock architectures [20] reduce the power of clock recovery at the expense of an additional forwarded link to deliver the transmitted mesochronous clock. However, if the chip I/O interface

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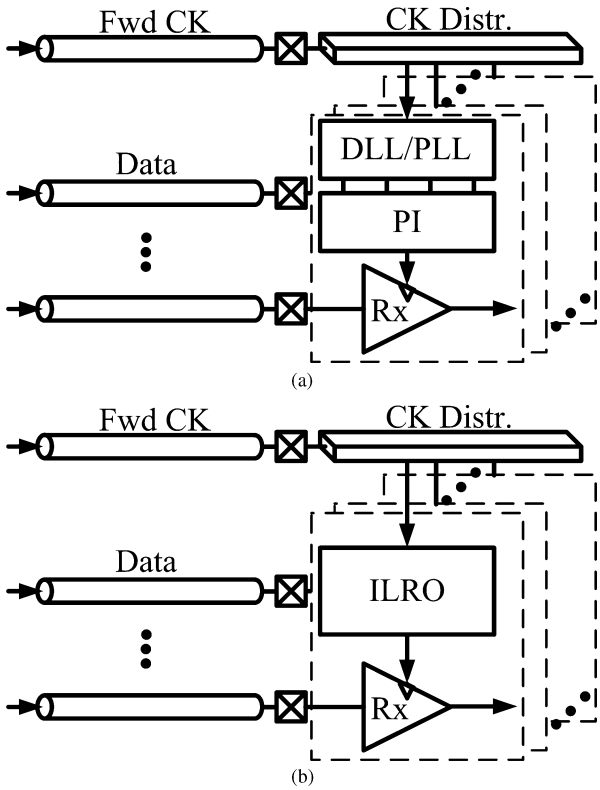


Fig. 1. (a) Conventional forwarded clock receiver architecture and (b) proposed architecture using ILRO for multiple serial links.

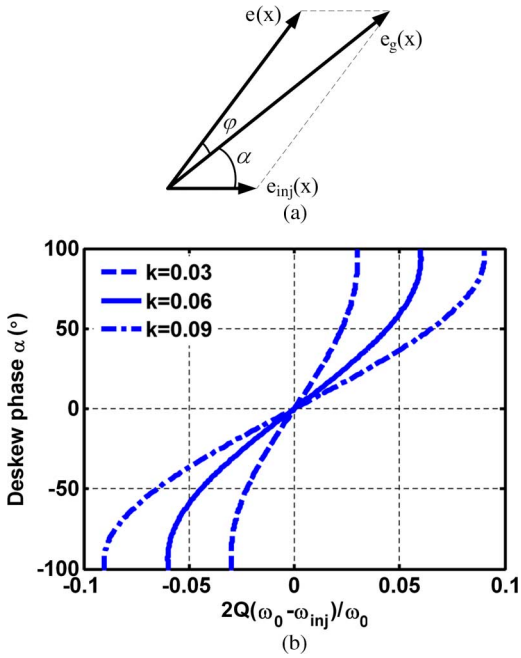


Fig. 2. (a) Phase vector diagram (injection signal $e_{inj}(x)$, free-running tank signal e(x) and resultant output $e_g(x)$). (b) Deskew with different injection strength k, based on Adler's equation.

requires many parallel serial lanes, the power and pin overhead of the additional forwarded clock can be amortized among all the data links.

A conventional, forwarded clock receiver architecture [21] is shown in Fig. 1(a), which consists of the global clock distribution, as well as the local delay/phase locked loop (DLL/PLL) to generate multiple time-interleaved phases. The proceeding phase rotator use these phases to interpolate the appropriate phase position for the receiver to sample the incoming data. In this architecture, significant power is spent in the receiver clocking and phase generation as each link needs a local, phase rotator-based PLL to deskew the clock phase for recovery of the data [22]. For example, phase rotation alone occupies almost half the total receiver power in [9].

As an alternative to the phase rotator, injection-locked LC oscillators (IL-LCO) can enable clock deskew ability with less power and a lower voltage swing for the global clock. Hence, injection-locking has recently been proposed for both clock distribution [12], [23] and serial link receivers [8], [24]. As shown from the phase vector diagram in Fig. 2(a), when the frequency of the injection signal $e_{inj}(x)$ is different from the free-running frequency of the signal in the LC tank, e(x), a phase deskew α will be generated between the resulting outputs $e_g(x)$ and $e_{inj}(x)$. The value α depends on the frequency difference and locking range, given by Alder's equation [15]:

$$\frac{d\alpha}{dt} = -\omega_{SL}\sin\alpha + \Delta\omega_0, \quad \omega_{SL} = k/\frac{d\varphi}{d\omega} = k\frac{\omega_0}{2Q} \qquad (1)$$

where α is the phase difference between the resultant output clock and the injection input clock, φ is the phase difference between the free-running frequency ω_0 and the resultant output, ω_{SL} is the single-sided locking range, k is the injection strength defined as the ratio of the injection current and the oscillator current, and $\Delta\omega_0$ is the frequency difference between ω_0 and the injection clock. Fig. 2(b) plots an example of the deskew phase shift along the normalized frequency difference under three injection strength values.

Monolithic LC oscillators typically have better phase noise and jitter performance than their ring oscillator counterparts due to the band-pass nature of LC tank resonators, rejecting out-of-band frequencies and filtering power supply induced noise [25]. However, for highly-parallel serial link applications, per-channel, injection-locked LC oscillators are not desirable, as each receiver would require an individual on-chip inductor, resulting in significant area penalty. In addition, LC-based oscillators exhibit very limited tuning range, may exhibit oscillator pulling due to magnetic coupling from adjacent LC oscillators [26], and do not scale well with continued technology scaling.

Although the jitter performance of free-running ring oscillators is typically worse than LC oscillators, the large jitter transfer bandwidth of injection locking can suppress and high-pass filter a large amount of oscillator phase noise, as will be described in Section III. Therefore, this work proposes a new forwarded clock receiver architecture using injection-locked ring oscillators (ILRO), as shown in Fig. 1(b), to deskew the clock used to sample the incoming data.

Compared with the conventional receiver architecture, the ILRO can achieve large phase deskew ability without the power overhead required for the combined DLL, PLL and phase interpolation. Second, it can lock to relatively small voltage swings of the injected global clock, saving power in the clock distribution. Third, the ILRO can achieve faster phase locking than a

conventional PLL because while the loop bandwidth of a PLL is limited to approximately 1/10 of the reference clock [26], injection-locking exhibits non-linear loop bandwidth characteristics.

Unfortunately, as shown in Fig. 2(b), nonlinearity can be observed in the deskew steps at the edge of locking range, when α reaches around $\pm 100^\circ$. However, the linear deskew region can be increased as the injection strength k increases. To further avoid the use of the nonlinear deskew region, each receiver uses 1:4 demultiplexing, implemented with four quantizers clocked by quadrature sampling. Therefore, only $\pm 45^\circ$ phase deskew range of the ring oscillator is required to enable each quadrature phase to achieve full UI range, limiting the deskew to only the linear region.

Compared with the IL-LCO, ILRO consumes less silicon area, larger tuning range, inherent multi-phase generation, and scalability to future CMOS processes. However, because previous analysis on the injection-locking phenomenon is applicable only to tank-based oscillators, new analysis is needed to further understand the behavior of the proposed ILRO.

III. Analysis on Injection-Locking Ring Oscillators

A. Previous Approaches

Several methods have been proposed in previous works to analyze injection locking in oscillators including: the phasor-based Adler's equation, the perturbation-based projection vector (PPV) method, and the waveform-based time-domain derivation.

The classic Adler's equation [15] expresses the oscillator behavior under injection locking by using a phasor vector diagram, as shown in (1) and Fig. 2. Various time-domain solutions to Adler's equation are discussed in [16]–[18]. However, two main factors prevent this approach from being applicable to ring oscillators. First, the output waveform of ring oscillators usually does not exhibit sine wave behavior; however, the adoption of a vector-based analysis relies on the assumption that there exists only a single dominant frequency component [28]. Second, it is required to know the quality factor Q in order to solve $\mathrm{d}\varphi/\mathrm{d}\omega$ in (1), which is not well defined for nonharmonic ring oscillators.

The PPV [27] and the transient waveform-based methods [28] are capable of analyzing both LC and ring oscillators. However, the PPV method requires a full circuit description at both the transistor and numerical levels, and only the expression for locking range is derived [27]. The analysis in [28] provides good insight into analyzing injection locking in the time domain. However, neither of these two methods gives an analytical expression for evaluating the jitter performance of injection-locked oscillators.

B. Proposed Approach for ILRO Analysis

Since Adler's equation is still quite simple and is proven useful for capturing the LC oscillator behavior in both the frequency and time domains, this work presents an expansion to Adler's equation that overcomes the two limitations mentioned above, making it suitable for injection-locked ring oscillators.

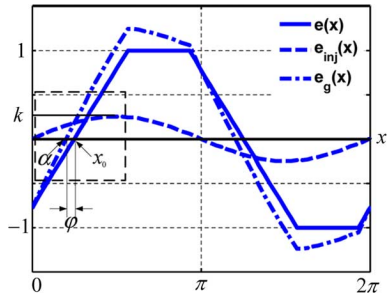


Fig. 3. Superposition of waveforms.

By revisiting the process of Adler's derivation [15], it can be observed:

$$\frac{d\alpha}{dt} = \varphi / \frac{d\varphi}{d\omega} + \Delta\omega_0. \tag{2}$$

Note that (2) is held for both LC and ring oscillators, as neither the assumption of Q nor a vector diagram approach has been applied yet. Next, alternative methods for finding $\mathrm{d}\varphi/\mathrm{d}\omega$ as well as the relationship between φ and α are presented.

First, $\mathrm{d}\varphi/\mathrm{d}\omega$ can be solved directly from the small signal model of each delay cell. Assuming each delay cell contributes one dominant 3 dB pole, the loop transfer function H of an N-stage ring oscillator is

$$H(j\omega) = -\left(\frac{A_0}{1 + j\omega/\omega_{3\ \mathrm{dB}}}\right)^N \tag{3}$$

such that its phase and derivative are

$$\varphi(j\omega) = N \tan^{-1}(\omega/\omega_{3\ \mathrm{dB}}) \tag{4}$$

$$\left.\frac{d\varphi}{d\omega}\right|_{\omega=\omega_0} = \frac{N}{2\omega_0} \sin\frac{2\pi}{N}. \tag{5}$$

Equation (5) is obtained by noting that each delay stage exhibits a phase shift equal to $\tan^{-1}(\omega_0/\omega_{3\ \mathrm{dB}}) = \pi/\mathrm{N}$. Similar analysis can lead to an equivalent definition of Q for ring oscillators as shown in [29].

Second, the phase relationship can be obtained by superposition of waveforms in the time-domain rather than using a vector diagram; this enables a general analysis for any arbitrary waveform. As shown in Fig. 3, the proposed derivation assumes that the small-swing injection clock $\mathrm{e_{inj}(x)}$ remains like a sine-wave, but the waveform shape of the free-running ring oscillator e(x) resembles a trapezoid. Hence, this trapezoidal model reflects the actual waveform of a nonharmonic ring oscillator with equal rise and fall times, where the slope is $\mathrm{k_f}$. Signal $\mathrm{e_g(x)}$ is the resulting superposition waveform of both the injection and the ring oscillator signals, and $\mathrm{x_0}$ is the phase difference between $\mathrm{e_{inj}(x)}$ and e(x), which is equal to $\alpha+\varphi$. Other symbols remain unchanged. The amplitude is normalized to the amplitude of the free-running oscillator, and the time axis x is normalized to 2π. During the rising edge of the oscillator waveform (in the dashed box of Fig. 3), it is observed that due to superposition:

$$e_g(x) = e_{inj}(x) + e(x) = k \sin x + k_f(x - x_0) \tag{6}$$

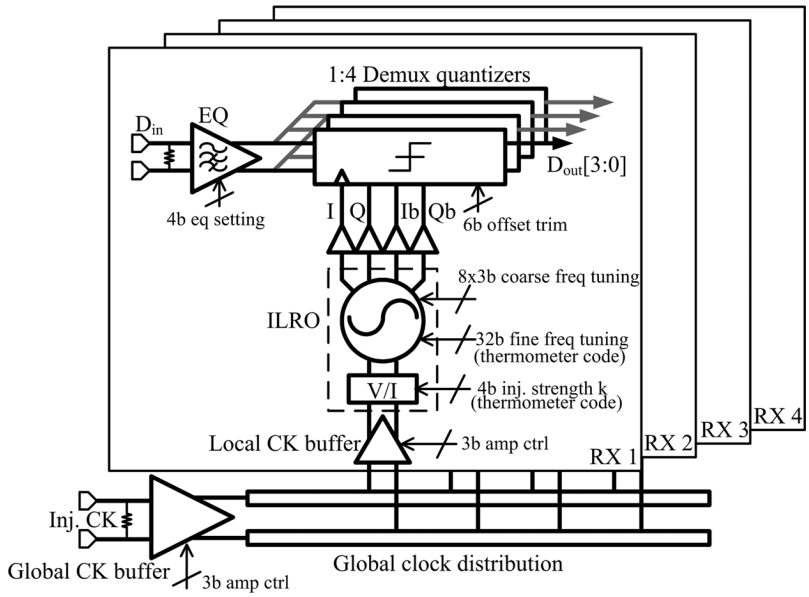


Fig. 4. Block diagram of proposed receiver.

Let (6) equal to 0, and noting that $\sin(\mathrm{x})$ can be approximated as $\sin \mathrm{x}_0 + (\mathrm{x} - \mathrm{x}_0)\cos(\mathrm{x}_0)$ using Taylor series expansion near x_0, it is obtained:

$$\varphi = -\frac{k \sin x_0}{k_f - k \cos x_0} \approx -\frac{k \sin \alpha}{k_f - k \cos \alpha} \tag{7}$$

The relationship between $\mathrm{k_f}$ and N for ring oscillators is

$$k_f = N\eta/\pi \tag{8}$$

where η is a proportionality constant, close to the value of one [30].

Substituting (5), (7) and (8) into (2), we observe:

$$\frac{d\alpha}{dt} = -\frac{k}{N\eta/\pi - k\cos\alpha} \frac{2\omega_0}{N \sin(2\pi/N)} \sin\alpha + \Delta\omega_0 \tag{9}$$

Hence, the new expression for single-sided locking range ω_{SL} becomes

$$\omega_{SL} = \frac{k}{N\eta/\pi - k\cos\alpha} \frac{2\omega_0}{N \sin(2\pi/N)} \tag{10}$$

Thus, we have derived new equations for analyzing the behavior of injection-locked ring oscillators (with no requirement for Q) by applying small signal and time-domain waveform analysis to Adler's derivation.

Further, by analogy between injection-locked oscillators and a 1st order PLL [31], jitter transfer and jitter generation functions can be derived as follows:

$$\left|\frac{\phi_{out}}{\phi_{inj}}\right| = \frac{1}{\sqrt{1 + (\omega/\omega_{SL})^2}}, \quad \left|\frac{\phi_{out}}{\phi_{vco}}\right| = \frac{1}{\sqrt{1 + (\omega_{SL}/\omega)^2}} \tag{11}$$

Therefore, ILRO will low-pass filter the noise from injection clock, while high-pass filter the noise from itself. Since the jitter of the injection clock (σ_{inj}) and that of oscillator (σ_{vco}) are usually uncorrelated, the total jitter can be expressed as

$$\sigma_{out}^2 = \left|\frac{\phi_{out}}{\phi_{inj}}\right|^2 \sigma_{inj}^2 + \left|\frac{\phi_{out}}{\phi_{vco}}\right|^2 \sigma_{vco}^2 \tag{12}$$

The results here will be verified with measurements in Section V.

IV. Circuit Implementation

Fig. 4 shows the block diagram of the major sections of the test chip. Four links are integrated for the experimental demonstration of a multiple serial link architecture using ILROs. The forwarded quarter-rate clock is first buffered by a global CML clock buffer driving a 600 um-long, ground-shielded, differential RC line to all four receivers with a 250 mV clock signal. The clock input is then coupled to each receiver through a local CML buffer that injects into the injection-locked ring oscillator. The ILRO generates tunable quadrature phases for the quantizers to recover and demultiplex the data.

A. ILRO

Each injection-locked oscillator consists of a voltage-to-current (V/I) converter and a four-stage, cross-coupled, pseudo-differential current-starved ring oscillator. Simple NMOS-only differential V/I converters without resistive loading are used here to mitigate the interaction with the DC bias at the injection point. The sizes of the NMOS differential pair are carefully chosen to reduce the parasitic loading while fully steering the current source.

All the delay cells in the ring oscillator share a single current source, implemented as a 32b thermometer-encoded DAC. The minimum DAC current step is 30 μA, enabling fine tuning of the free-running frequency of the oscillator. For coarse tuning of the

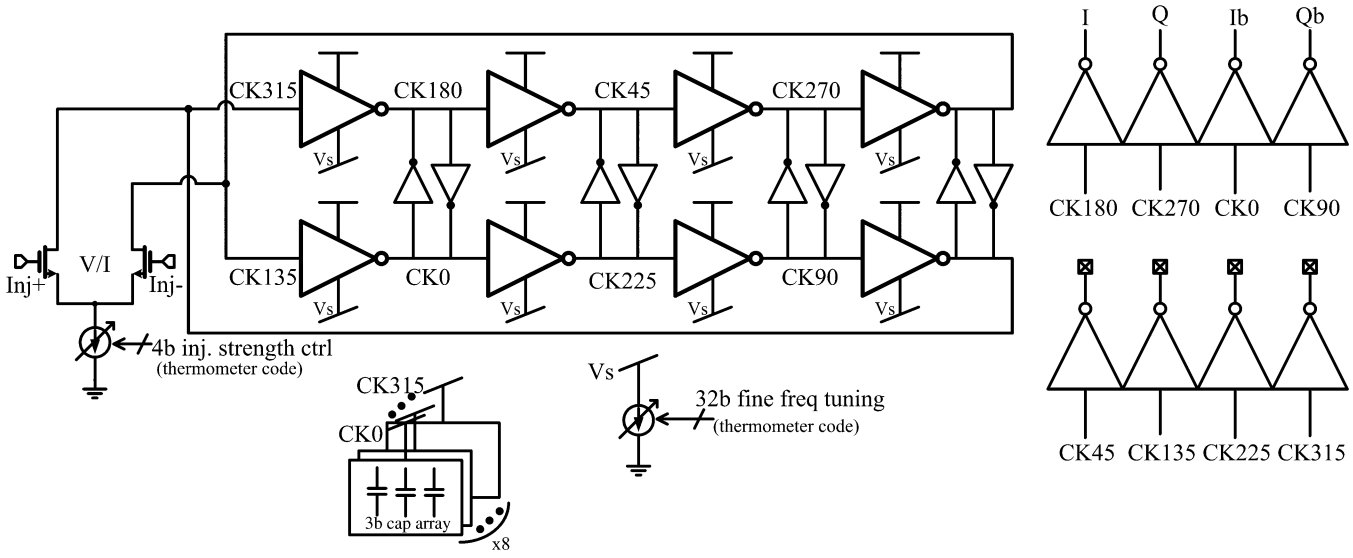


Fig. 5. Schematic of ILRO.

free-running VCO frequency, either the supply can be reduced or a 3b switched capacitor array can be utilized.

Injection-locking will cause adjacent time-interleaved phases of the oscillator to be unevenly spaced. For example, the injection nodes CK135 and CK315 exhibit significant phase asymmetry from the other six phases, as these nodes are the summing nodes from the injection-locking interpolation. However, once the differential clocks are propagated to CK0 and CK180, they are decoupled from the injection-point phase asymmetry, and now exhibit conventional inverter loading and delay. Hence, the four alternating phases (every two inverter stages) CK180, CK270, CK0, CK90 maintain adequate quadrature accuracy (less than 4.5°), both in the simulated as well as in the experimental results. Each of the eight multi-phases is loaded with the same inverter buffering, to maintain the same capacitive loading. Further phase symmetry is obtained by using small cross-coupled inverters between complementary phases, as well as using a 3b binary capacitor bank on each output clock phase to individually trim the phase imbalances that arise due to process variations or layout mismatch. In addition, for a typical application (not implemented here), an offline, static phase calibration of multiple, time-interleaved phases at reset time would be included to resolve maximum phase mismatch to several picoseconds [32], [33].

B. Linear Equalizer

The front-end receiver equalizer is the analog component that works at the highest frequency of all the receiver blocks. A source-degenerated, linear equalizer similar to [9] is implemented, as shown in Fig. 6(a). Its voltage gain can be written as

$$A_v = G_m R_{out} \approx \frac{g_m}{1 + g_m\left(R_s // \frac{1}{sC}\right)}\left(R_D // \frac{1}{sC_L}\right) = \frac{g_m R_D}{1 + g_m R_s}\frac{1 + s/\omega_z}{(1 + s/\omega_p)(1 + s/\omega_{p,out})} \quad (13)$$

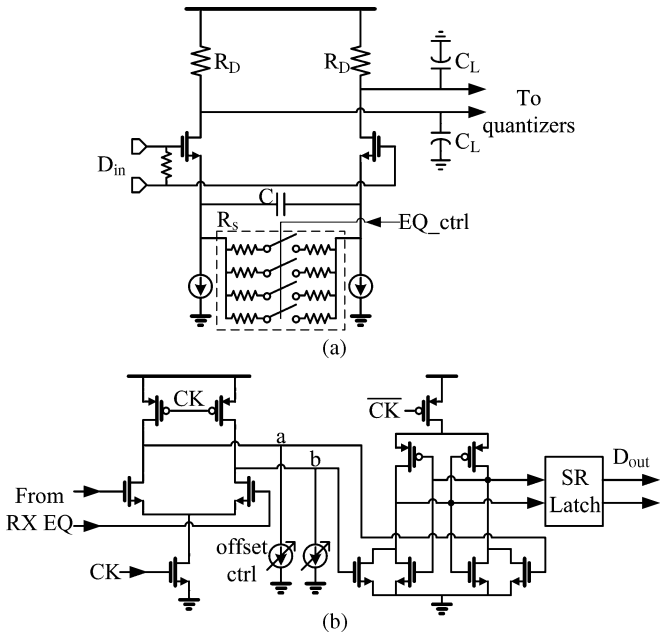


Fig. 6. (a) Schematic of RX EQ. (b) quantizer with offset control.

where $\omega_z = 1/R_s C, \omega_p = (1+g_m R_s)/R_s C = (1+g_m R_s)\omega_z$, and output pole $\omega_{p,out} = 1/R_D C_L$. Therefore, $\mathrm{R_s}$ and C introduce a zero ω_z before the pole ω_p. If the output pole $\omega_{p,out}$ is also designed to be larger than the zero, gain will be boosted between ω_z and the smaller one of ω_p and $\omega_{p,out}$. By switching the value of the degenerated resistor $\mathrm{R_s}$, the DC gain will change as shown in Fig. 7, resulting in an effective high-pass filtering effect.

C. Other Building Blocks

Each quantizer of the 1:4 demuxplexing is implemented using a two-stage sense amplifier [34] and SR latch, as shown in Fig. 6(b). A 6b binary current source can be injected to nodes ***a*** and ***b*** in order to cancel the quantizer offset by current-imbalancing.

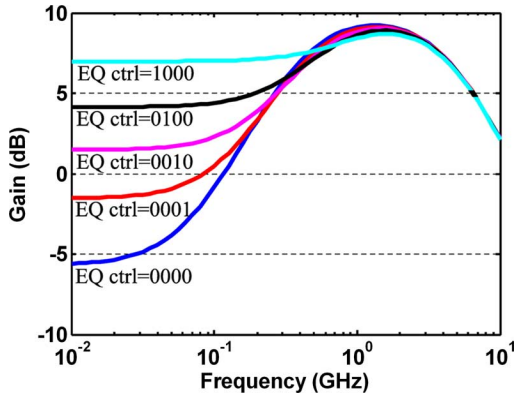


Fig. 7. Simulated AC response of RX EQ under different settings.

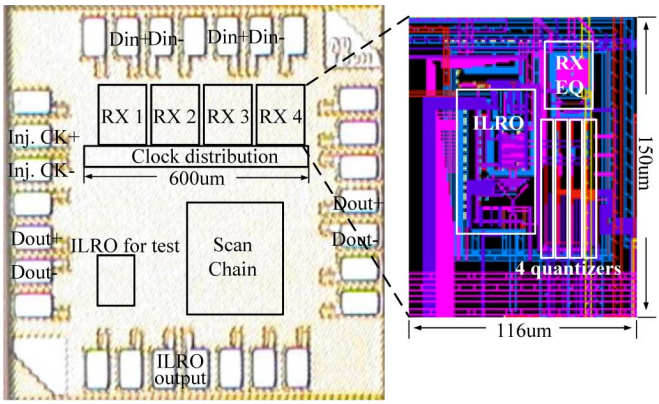


Fig. 8. Die photo and layout screen capture.

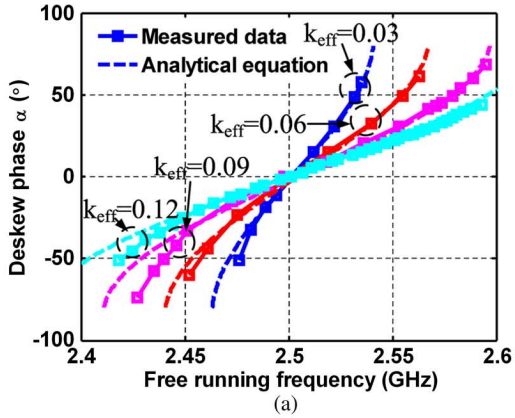
V. Experimental Results

The 1 mm^2 test chip has been fabricated in a 90 nm, 1.2 V CMOS process and tested in a chip-on-board assembly. As shown in Fig. 8, it integrates four receivers, the global clock distribution network, a digital scan chain, test output buffers and a stand-alone ILRO for test purposes. Each receiver occupies 0.0174 mm^2. Due to the limitation in pad area, only near-end (RX1) and far-end (RX4) I/Os are measured. In each receiver, the four-way, demultiplexed output data can be individually selected to drive the output pads.

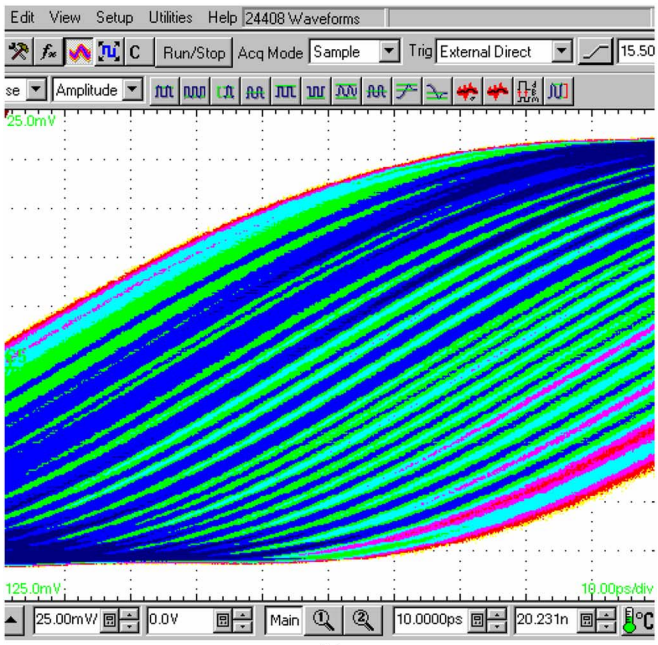
A. ILRO

In this subsection, the analytical equations derived in Section III will be examined and compared with measurement data. Note that the stage number $N = 4$ and assumes $\eta = 1$. The ILRO can tune from 1.6 GHz to 2.6 GHz by coarse tuning its supply, while turning on all switches in the digital switch capacitor bank can provide an additional 250–300 MHz frequency range. Hence, this large and fine tuning range can be used to compensate possible variations. Note that a shared, frequency-locked loop (not implemented in this work) initiated at reset time, can be used at startup to calibrate and compensate for initial oscillation frequency variations [35].

Fig. 9(a) shows both the measured deskew under different injection strength k_{eff} and the analytical model predicted from (9). In this measurement, the injection clock was kept constant at 2.5 GHz and the current-DAC, fine tuning control was swept



(a)



(b)

Fig. 9. (a) Deskew of ILRO; (b) overlaid waveforms by sweeping phase settings (vertical scale = 25 mV/div, horizontal scale = 10 ps/div).

until the oscillator operated beyond its locking range. The measured phase shift confirms the same deskew characteristics as the simulated ILRO shown previously in Fig. 2(b). The measured results also show that the ILRO can achieve greater than $\pm 45°$ linear deskew range. Fig. 9(b) plots the corresponding output waveforms of the ILRO, overlaid on oscilloscope, giving an intuitive viewpoint of the fine interpolation steps of ILRO. The measured injection-locking ranges for injection strength $k_{eff} = 0.03, 0.06, 0.09$, and 0.12 are 65, 115, 167, and 203 MHz, respectively.

The jitter performance was measured by keeping the free-running frequency fixed at round 2.5 GHz and sweeping the frequency of the injection clock. Fig. 10 shows that the jitter of ILRO will first get slightly worse as the frequency of injection clock moves away from the free-running frequency, and then get dramatically worse at the edge of locking range. By substituting measured RMS jitters of injection clock and free-running ring oscillator into (12), we can successfully predict the jitter degradation when the injection clock is near the free-running frequency. This is because ω_{SL} will reduce slightly due to

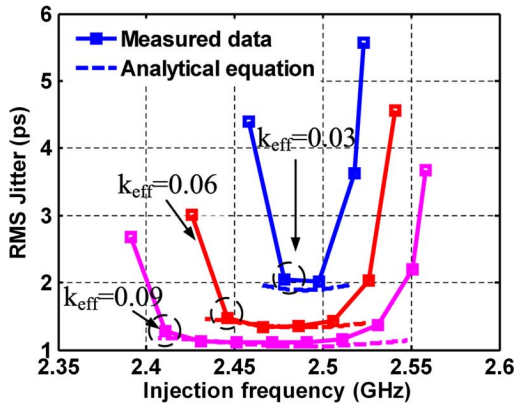


Fig. 10. Jitter performance of ILRO.

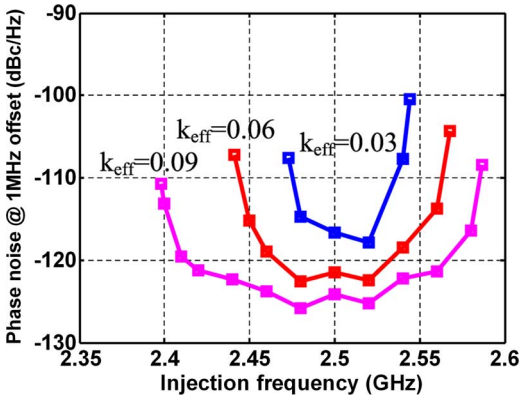


Fig. 11. Measured phase noise performance of ILRO.

the change of α from (10), such that more noise of the oscillator will pass through to the output. At the edge of the locking range, the jitter worsens because the oscillator is on the cusp of losing phase lock. However, across the linear deskew range, the jitter stays sufficiently low (below 1.5 ps RMS jitter when $k_{eff} = 0.09$) such that the jitter degradation will not affect the normal operation of the ILRO. Corresponding measurements of the phase noise shows a similar tendency in the performance degradation, as shown in Fig. 11.

The -3 dB bandwidth at $k_{eff} = 0.03$, 0.06, 0.09, and 0.12 are 31, 55, 80, and 100 MHz, respectively, as shown in Fig. 12. This measurement is done directly by injecting a stressed input clock with 5% UI of sine jitter generated by a BertScope 12500B. To verify the phase symmetry, quadrature output waveforms of the ILRO are overlaid in Fig. 13. Measurement across the linear deskew range shows a maximum I/Q phase and amplitude imbalance of 4.5° and 7 mV, respectively.

B. Entire Receiver

Experimental measurements are obtained from testing the far-end receiver (RX4). RX4 exhibits the longest clock distribution distance among the four receivers, and therefore shows the worse case performance of the four lanes. The results are measured from 6.4 Gb/s to 8 Gb/s with a 400 mV swing PRBS 7 data sequence generated by the BertScope under two channel conditions: 1) chip-on-board bond-wire with a 4 cm PCB trace on the test board plus two SMA connectors and cables, and

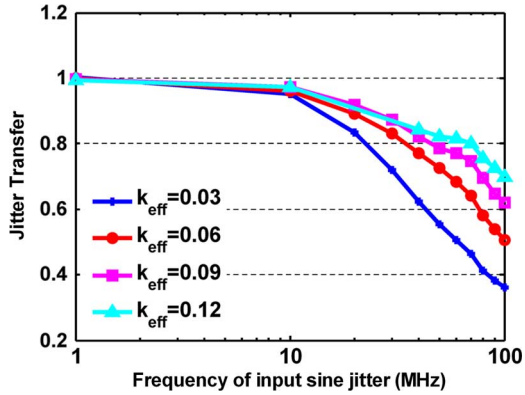
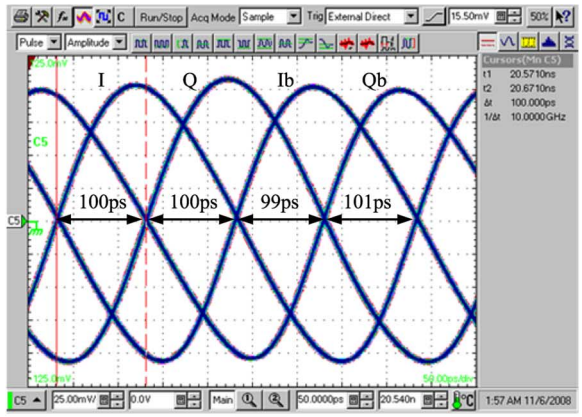
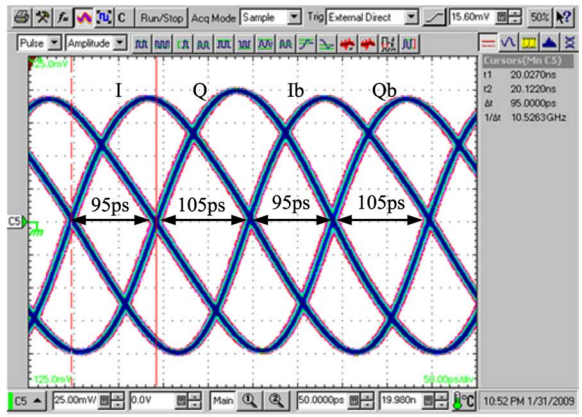


Fig. 12. Measured jitter transfer of ILRO.



(a)



(b)

Fig. 13. Phase spacing when injecting 2.5 GHz clock: (a) $f_0 = 2.49$ GHz, (b) $f_0 = 2.58$ GHz (vertical scale = 25 mV/div, horizontal scale = 50 ps/div).

2) uses both 1) and an additional 10 cm of FR4 PCB trace. They are denoted as 4 cm trace and 14 cm trace in this paper, and exhibit approximately 1 dB and 5 dB loss at 4 GHz, respectively.

The receiver consumes 3.84 mW, 4.3 mW and 4.8 mW[1] at input data rates of 6.4 Gb/s, 7.2 Gb/s, and 8 Gb/s, respectively. Fig. 14 shows the breakdown of the power for the receiver. The ILRO occupies 23% of the total power consumption, which is

[1]We do not implement an on-chip regulator in this design. Supply noise was mitigated by using large decoupling capacitors both on-chip and off-chip and testing with an off-chip, precision digital voltage generator. Power of test buffers is not included.

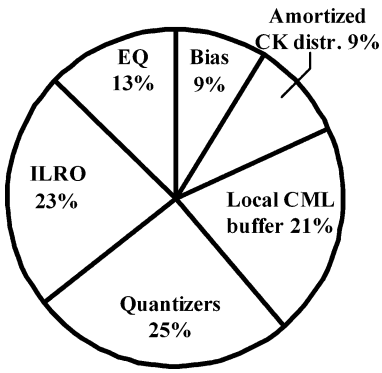
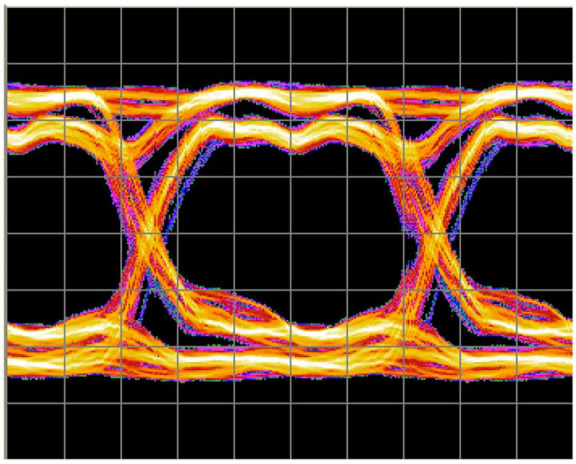
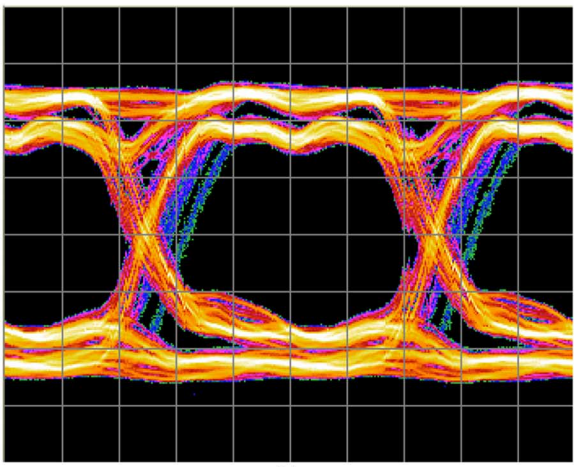


Fig. 14. Receiver power breakdown.

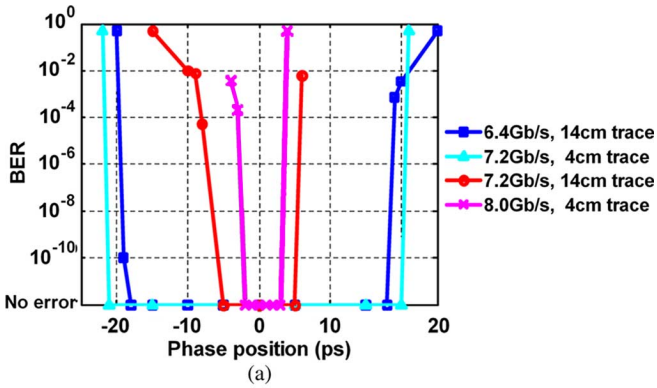


(a)

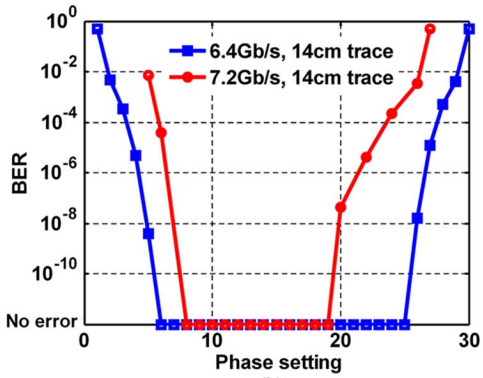


(b)

Fig. 15. Eye diagrams of recovered data under (a) 4 cm trace and (b) 14 cm trace (input data rate = 7.2 Gb/s, vertical scale = 155 mV/div, horizontal scale = 111 ps/div).



(a)



(b)

Fig. 16. BER measurements (a) by sweeping the delay in BERT and (b) by sweeping the phase setting of ILRO.

TABLE I
PERFORMANCE SUMMARY

Technology	1.2V 90nm CMOS		
ILRO tuning range	1.6-2.6GHz		
ILRO locking range (k_{eff}=0.12)	203MHz		
Phase deskew resolution(k_{eff}=0.12)	1.8°-3.6°		
ILRO power	0.88mW @1.6GHz	1.08mW @1.8GHz	1.3mW @2GHz
Total RX Power (including amortized power of clock distr.)	3.84mW @6.4Gb/s	4.3mW @7.2Gb/s	4.8mW @8Gb/s

about half the ratio of a phase rotator within a conventional link receiver, as in [9]. Therefore the clock related power is reduced to about 53% of the total receiver power.

Eye diagrams of one stream of recovered 1.8 Gb/s data from the 7.2 Gb/s input are shown in Fig. 15. There exists a slightly bimodal eye diagram when the 14 cm PCB trace is used. Due to a sub-optimal design of the equalizer where the peak is placed 2× lower than desired for this PCB Nyquist bandwidth, the channel plus component assembly results in more loss and reflection than expected, such that the equalization is not enough to compensate for the channel losses at higher data rate. Fig. 16 plots the measured BER bathtub curves for the two channel conditions, with the measured performance summarized in Table I. Table II compares the performance with prior state-of-the-art, energy-efficient serial links.

VI. CONCLUSION

A four-lane, 6.4–7.2 Gb/s per link, parallel serial link receiver design has been presented. The proposed forwarded clock ar-

TABLE II
COMPARISON WITH RECENT DESIGNS

	[9]	[8]	This work
Data rate	6.25Gb/s	27Gb/s	7.2Gb/s
Architecture	Software CDR	Forwarded CK	Forwarded CK
Phase tuning method	Ring-VCO PLL with PI	IL-LCO	ILRO
RX power	8.22mW	43mW	4.3mW
Power efficiency	1.31 mW/Gb/s	1.6 mW/Gb/s	0.6 mW/Gb/s
RX area	~0.15mm^2	0.015mm^2	0.0174mm^2
Technology	90nm CMOS	45nm CMOS	90nm CMOS

chitecture using ILROs allows the test chip to obtain full UI deskew while achieving only 0.6 mW/Gb/s under moderate channel losses. The use of ILROs also exhibits other benefits including inherent multiphase generation and large jitter transfer bandwidth. Methods to avoid the nonlinearity of ILROs are also discussed. Simple analytical equations are derived to understand both the injection locking and jitter performance of ILROs and are verified with experimental measurements. The methods presented provide new insights into low power serial link design for future multi-Gb/s I/O interfaces.

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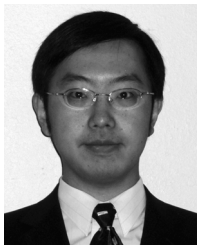

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