

Strong Injection Locking in Low- Q LC Oscillators: Modeling and Application in a Forwarded-Clock I/O Receiver

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Abstract—A general model for injection-locked LC oscillators (LC-ILOs) is presented that is valid for any tank quality factor and injection strength. Important properties of an ILO such as lock-range, phase shift, bandwidth and response to input jitter are described. An LC-ILO together with a half-rate data sampler is implemented as a forwarded-clock I/O receiver in 45-nm CMOS. A strongly-injected low- Q LC oscillator enables clock deskew across 1UI and rejects high-frequency clock jitter. The complete 27 Gb/s ILO-based data receiver has an overall power efficiency of 1.6 mW/Gb/s.

Index Terms—Clocks, high-speed input/output (I/O), jitter, receivers, voltage-controlled oscillator (VCO).

I. INTRODUCTION

THE TECHNIQUE of injection locking has recently gained substantial attention in CMOS communication circuits. Recent applications include quadrature voltage-controlled oscillators (VCOs) [1], frequency dividers [2], [3], frequency multipliers [4], interference cancellation [5], clock recovery [6], and jitter filtering and phase deskew [7]–[10]. LC oscillators are widely used due to their superior noise performance compared with CMOS ring VCOs. The prior-state-of-the-art has extensively studied and modeled the behavior of an injection-locked LC oscillator (LC-ILO). Adler explained the phenomena of injection locking in LC oscillators for weak injection strength (amplitude ratio of the injecting signal to that of free running oscillator = $A_{inj}/A_{osc} \ll 1$) (see Fig. 1) [11]. The behavior of an LC-ILO for higher injection strength was explained later by Paciorek [12].

The quality factor Q of the LC oscillators when implemented in fine line digital CMOS technology tends to be poor relative to discrete and integrated inductors on processes that are optimized for analog and RF applications. Series resistance and substrate loss typically limit the inductor quality factor to around 4–5, whereas the tank itself may have a quality factor of 2–3

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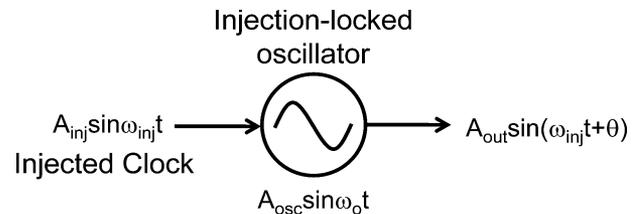


Fig. 1. Injecting an oscillator with an external clock.

when other tank losses are also taken into consideration. Prior analysis of LC-ILOs modeled the tank as an equivalent parallel RLC network. However, for the range of inductor quality factor achievable within a typical digital CMOS process, this tank approximation fails to accurately model the behavior of an ILO. In this paper, we present an ILO model that uses a series-RL parallel-C network for the LC tank. It is shown that the proposed model correctly predicts the behavior of ILOs for any tank Q , including low- Q tanks. The advantages of strong injection strength in injection locking oscillators (ILOs) are explained. It is also shown that the proposed model accurately models the injection locking behavior for all injection strengths.

An application of high injection strength, low- Q ILOs is then presented in a forwarded-clock data receiver. In forwarded-clock parallel I/Os, multiple data channels are accompanied by a dedicated clock channel. They provide the high data rates needed to support the aggregate bandwidth (BW) of microprocessors in a dense, low-power form factor. Fig. 2 shows a simplified block diagram of a forwarded clock I/O transceiver. The clock pattern, sent on a separate but similar channel, is used in the receiver to sample the data pattern at the optimum point. Source synchronous forwarded-clock I/Os benefit from the tracking of transmit jitter that is modulated on both the data and clock patterns. However, as there is usually a delay mismatch between the clock and the data channel, the effective tracking is limited. Tracking high-frequency jitter that is beyond the tracking BW can degrade link performance. In addition, data-dependent amplification of high-frequency jitter across lossy channels can further degrade clock-data jitter tracking [13]. To account for latency mismatch and sample the data pattern at the optimum point, a clock deskew mechanism is used to optimally shift the forwarded clock. Delay locked loops (DLLs) in conjunction with phase interpolators (PIs) are commonly used to deskew the clock phase (see Fig. 2). However, due to an all-pass jitter transfer characteristic, a DLL

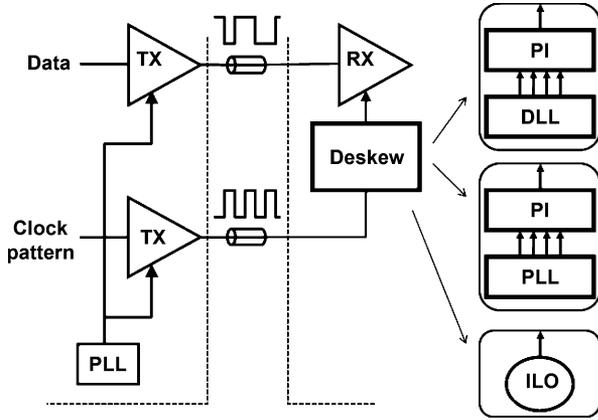


Fig. 2. Forwarded clock I/O transceiver with different receiver phase-deskew options.

cannot filter the amplified high frequency jitter [14]. High-frequency clock jitter can be filtered by using a phase locked loop (PLL) in conjunction with PIs, owing to the inherent low-pass jitter transfer characteristic of a PLL [15]. However, low-power high-BW PLLs are difficult to design, and the loop filter and supply decoupling capacitor can consume a large amount of silicon area. They also usually suffer from deterministic jitter due to device mismatch such as charge-pump asymmetry leading to control voltage ripple. Both DLLs and PLLs require a high-speed control loop, whose design typically entails stability concerns and higher power consumption. In order to overcome the above limitations, this paper presents a differential LC-ILO that deskews and filters the forwarded clock and simultaneously achieves low power, low area and low susceptibility to device variation. This technique is demonstrated in a 27 Gb/s forwarded-clock data receiver.

This paper is organized as follows. Section II presents the theory and modeling of an LC-ILO. Section III of the paper gives an overview of the implemented data receiver. Circuit level details of the LC oscillator and data sampler are then presented in Sections IV and V, respectively. Measurements results from a prototype chip are presented in Section VI, followed by conclusions in Section VII.

II. INJECTION LOCKING MODEL OF AN LC OSCILLATOR

Fig. 3(a) shows a conceptual injection-locked LC oscillator with a tuned tank. When the injecting signal magnitude is zero ($I_{inj} = 0$), the LC oscillator runs at its free-running frequency (ω_0) where its tuned tank contributes no phase shift ($\phi = 0$). When the oscillator is injection locked to an external signal, the oscillator frequency becomes equal to the external signal frequency (ω_{inj}). If there is a frequency difference between ω_{inj} and ω_0 , the tank impedance contributes a nonzero phase shift, $\phi \neq 0$. For instance, if ω_{inj} is greater than ω_0 , the tank impedance has a negative phase shift, $-\phi_1$ [see Fig. 3(a)]. To maintain oscillation at ω_{inj} , the total tank current (I_T) must have the same phase angle with the opposite polarity of the tank impedance. As a result, the ILO introduces a phase shift (θ) between the injected clock and its output signal [see Fig. 3(b)].

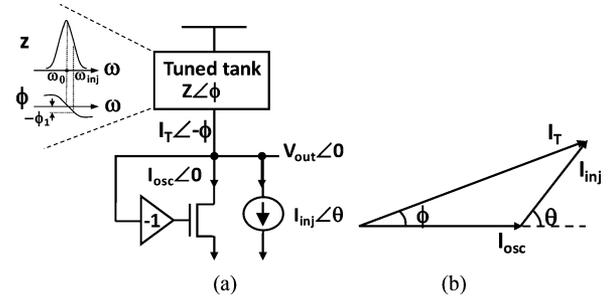


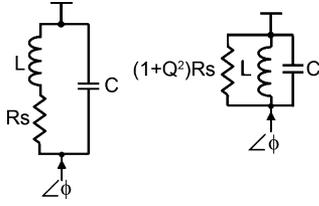
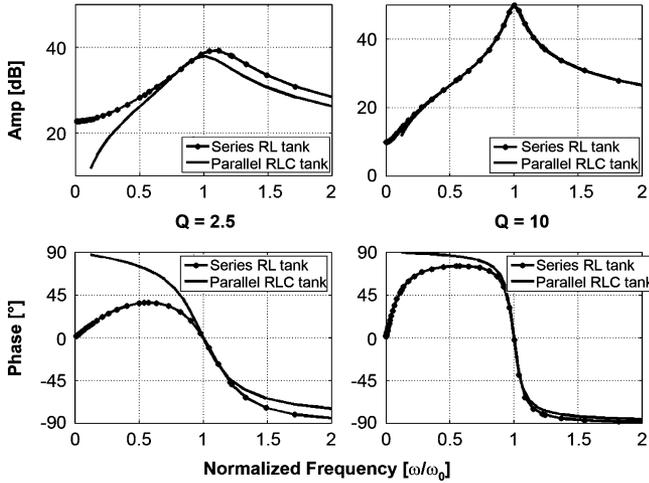
Fig. 3. Injection-locked LC oscillator and its vector diagram.

From Fig. 3(b), the relationship between θ and ϕ is given below where K represents the injection strength

$$\tan \phi = \frac{I_{inj} \cdot \sin \theta}{I_{osc} + I_{inj} \cdot \cos \theta} = \frac{K \cdot \sin \theta}{1 + K \cdot \cos \theta}, \quad K = \frac{I_{inj}}{I_{osc}}. \quad (1)$$

To the best of our knowledge, all previous analyses of electrical LC-ILO behavior are based on a parallel RLC equivalent circuit. However, this model can be inaccurate for tanks with significant series loss. Fig. 4 shows two models for a lossy LC tank, one with a series RL in parallel with C and one with its equivalent parallel RLC circuit. The calculated amplitude and phase of both tuned tanks as a function of normalized frequency are plotted in Fig. 5. At higher $Q = 10$, the parallel RLC tank closely approximates the amplitude of series RL tank. As Q is reduced to 2.5, however, the amplitude predicted by the equivalent RLC tank deviates from the real amplitude of a series RL tank. Unlike the equivalent parallel tank, the phase of a series RL tank is not symmetric with respect to the oscillator free-running frequency, ω_0 . As shown by Fig. 5, the phase asymmetry becomes worse as Q is reduced. As Q reduces and/or the injection strength of an ILO increases, the frequency range over which the ILO can lock increases. Thus, the phase asymmetry across the lock range becomes more pronounced for a low- Q and/or high- K ILO. Fig. 6 qualitatively plots the range of Q and K values at which the previously derived ILO equation based on an equivalent parallel RLC tank is inadequate to correctly model the ILO. To analytically demonstrate the ranges of K and Q values at which an ILO model based on an equivalent parallel RLC tank fails, we first derive the locking equation for a series RL tank, similar to the methodology used in [12]. Both phase and amplitude of the tank impact the ILO behavior. However, the oscillation amplitude is typically kept constant with an amplitude tracking mechanism [16]. Thus, similar to [12], we only consider the tank phase and assume the oscillation amplitude is constant. The phase of a series RL tank and its equivalent parallel RLC tank for a frequency ω is given by (2) and (3), respectively

$$\text{Series RL : } \phi = \arctan \left[\frac{-2Q(\omega - \omega_0)}{\omega_0} \left(\frac{1}{2} \cdot \left(1 - \frac{1}{Q^2} \right)^{1.5} \cdot \left(\frac{\omega + \omega_0}{\omega_0^2} \cdot \omega \right) \right) \right] \quad (2)$$

Fig. 4. Tuned series RL in parallel with C tank and its equivalent RLC tank.Fig. 5. Amplitude and phase of series versus parallel tank for $Q = 2.5$ and 10 .

$$\text{Parallel RLC} : \phi = \arctan \left[\frac{-2Q(\omega - \omega_0)}{\omega_0} \right]. \quad (3)$$

Substituting these phase equations into (1) results in

$$\begin{aligned} \text{Series RL} : \frac{2Q(\omega - \omega_0)}{\omega_0} \left(\frac{1}{2} \cdot \left(1 - \frac{1}{Q^2}\right)^{1.5} \cdot \left(\frac{\omega + \omega_0}{\omega_0^2} \cdot \omega\right) \right) \\ = \frac{-K \cdot \sin \theta}{1 + K \cdot \cos \theta} \end{aligned} \quad (4)$$

$$\text{Parallel RLC} : \frac{2Q(\omega - \omega_0)}{\omega_0} = \frac{-K \cdot \sin \theta}{1 + K \cdot \cos \theta} \quad (5)$$

where ω is the oscillator instantaneous frequency and is equal to $\omega_{inj} + d\theta/dt$. By replacing ω in (4) and (5), the locking equations for the two tanks are obtained

$$\begin{aligned} \text{Series RL} : \frac{\left(\frac{d\theta}{dt} + \omega_{inj}\right)^3}{\omega_0^2} - \frac{d\theta}{dt} = \omega_{inj} - \left(\frac{\omega_0}{Q \cdot \left(1 - \frac{1}{Q^2}\right)^{1.5}} \right) \\ \cdot \frac{K \cdot \sin \theta}{1 + K \cdot \cos \theta} \end{aligned} \quad (6)$$

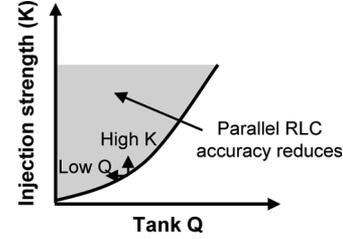


Fig. 6. Limitation of an ILO model based on a parallel RLC tank approximation.

$$\text{Parallel RLC} : \frac{d\theta}{dt} = \omega_0 - \omega_{inj} - \left(\frac{\omega_0}{2Q} \right) \cdot \frac{K \cdot \sin \theta}{1 + K \cdot \cos \theta}. \quad (7)$$

With the injection locking equation now developed for a series RL tank, we next calculate and compare the ILO properties of lock range, phase shift and bandwidth for both tank models and for different K and Q values.

A. Lock Range

The lock range of an ILO is defined to be the maximum frequency difference between the injection signal and oscillator for which locking occurs. At lock, there is a constant phase shift θ_{ss} between the oscillator and injected signal. To calculate the lock range, we first set $d\theta/dt = 0$ and $\theta = \theta_{ss}$ in (6) and (7)

$$\text{Series RL} : \frac{Q}{\omega_0} \cdot \left(1 - \frac{1}{Q^2}\right)^{1.5} \cdot \left(\omega_{inj} - \frac{\omega_{inj}^3}{\omega_0^2}\right) = \frac{K \cdot \sin \theta_{ss}}{1 + K \cdot \cos \theta_{ss}} \quad (8)$$

$$\text{Parallel RLC} : \omega_0 - \omega_{inj} = \left(\frac{\omega_0}{2Q} \right) \cdot \frac{K \cdot \sin \theta_{ss}}{1 + K \cdot \cos \theta_{ss}}. \quad (9)$$

Then, we differentiate ω_{inj} with respect to θ_{ss} and solve for the maximum constant phase shift $\theta_{ss \max}$. Interestingly, the maximum phase shift calculated for series tank is equal to the result shown in [12] for a parallel tank

$$\theta_{ss \max} = 180^\circ - \arccos(K). \quad (10)$$

By substituting $\theta_{ss \max}$ into (8) and (9), the lock range for both tank models is calculated in (11) and (12), shown at the bottom of the page. Equation (11) is composed of two sets of equations for the negative lock range, ω_{L-} , (i.e., $\omega_{inj \max} - \omega_0 < 0$), and positive lock range, ω_{L+} , (i.e., $\omega_{inj \max} - \omega_0 > 0$). Therefore, unlike a parallel RLC tank, the lock range for a series RL tank is not symmetric around the oscillator free-running frequency

$$\text{Series RL} : \begin{cases} (\omega_0 + \omega_{L+})^3 - (\omega_0 + \omega_{L+}) \cdot \omega_0^2 = \frac{\omega_0^3}{Q \cdot \left(1 - \frac{1}{Q^2}\right)^{1.5}} \cdot \frac{K}{\sqrt{1-K^2}}, \omega_{L+} = \omega_{inj \max} - \omega_0 \\ (\omega_0 - \omega_{L-})^3 - (\omega_0 - \omega_{L-}) \cdot \omega_0^2 = \frac{-\omega_0^3}{Q \cdot \left(1 - \frac{1}{Q^2}\right)^{1.5}} \cdot \frac{K}{\sqrt{1-K^2}}, \omega_{L-} = \omega_0 - \omega_{inj \max} \end{cases} \quad (11)$$

$$\text{Parallel RLC} : \omega_{L \max} = |\omega_{inj \max} - \omega_0| = \frac{\omega_0}{2Q} \cdot \frac{K}{\sqrt{1-K^2}} \quad (12)$$

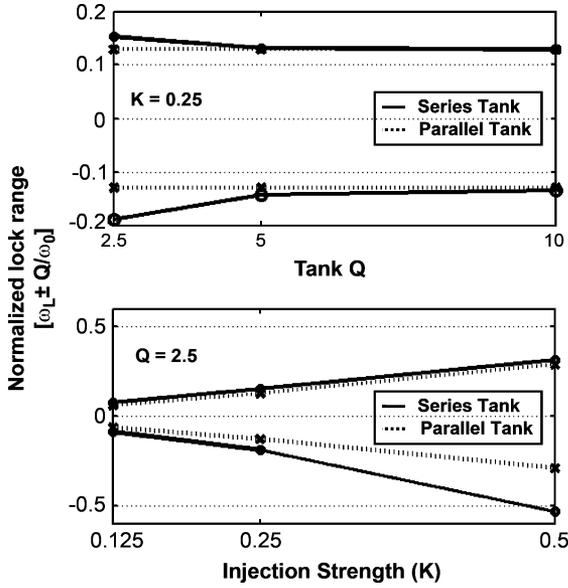


Fig. 7. Calculated lock range for series and parallel tank.

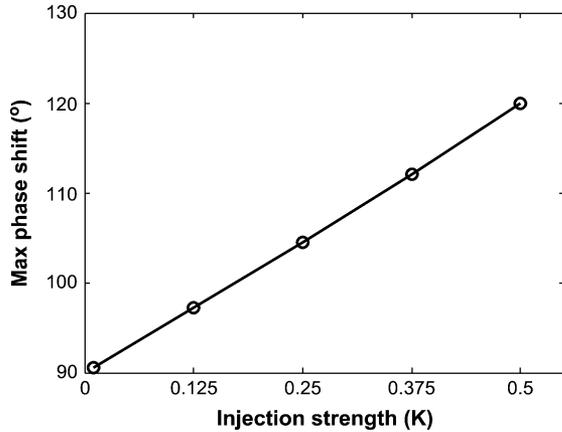


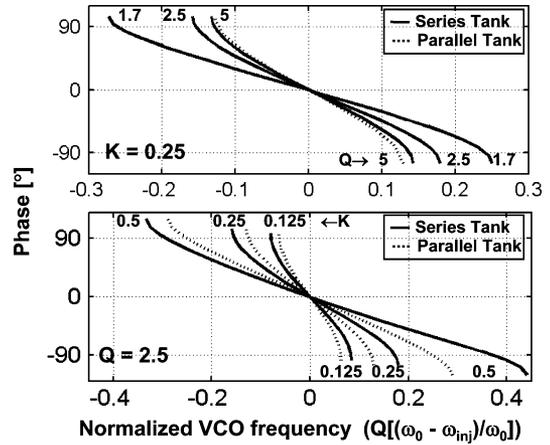
Fig. 8. Calculated maximum phase shift as a function of injection strength.

(ω_0). Fig. 7 plots the lock range calculated by (11) and (12) for different Q and K values. For a constant K ($= 0.25$), as Q reduces, the parallel tank model underestimates the lock range and also fails to predict the asymmetry between positive and negative lock range. Increasing K with a constant low Q ($= 2.5$) also results in more asymmetric lock range using the series tank model, while a parallel tank model fails to predict it.

B. Phase Shift

At lock, there is a constant phase shift between the oscillator and injected clock signal. Due to this interesting property, one application of an ILO is to shift/deskew the phase of the injected clock [8], [9]. The maximum phase shift achievable by an LC-ILO only depends on K and is calculated from (10). Shown in Fig. 8, the maximum phase shift of $\pm 90^\circ$ for weak injection ($K \ll 1$) increases to $\pm 120^\circ$ for $K = 0.5$. In other words, high injection strength ILOs are desirable as they provide larger phase shift range.

For a given injected clock frequency (ω_{inj}), the phase shift, calculated by (8) and (9), is a function of Q , K and the oscillator free-running frequency (ω_0). Fig. 9 plots the calculated θ_{ss} for


 Fig. 9. Calculated phase shift for series RL versus parallel RLC tank.

a series tank versus its equivalent parallel tank for different Q and K values. By rearranging (9), it can be shown that the phase shift for a parallel tank, plotted as a function of $Q(\omega_0 - \omega_{inj})/\omega_0$, is independent of Q and only dependent on K . For a constant K ($= 0.25$) and for high Q (> 5), θ_{ss} approximated by the equivalent parallel tank closely matches θ_{ss} calculated by the series RL tank model. However, as Q reduces, the error in θ_{ss} calculated from the equivalent parallel tank model increases relative to the series RL tank model. Therefore, at low Q (< 5), the ILO equation for a parallel tank fails to predict the correct θ_{ss} (see Fig. 9). For a constant low Q ($= 2.5$), the parallel tank model overestimates the phase shift for a given frequency offset from ω_0 and underestimates the oscillator frequency range required to provide $-90^\circ \leq \theta_{ss} \leq 90^\circ$. As K increases, the error in approximating θ_{ss} using a parallel tank increases (see Fig. 9). To design an ILO that provides 1UI phase shift, increasing K extends the phase shift beyond $\pm 90^\circ$ and consequently, it improves the phase linearity and resolution for $-90^\circ \leq \theta_{ss} \leq 90^\circ$. However, there is a tradeoff between K and the required frequency range of oscillator. The tradeoff becomes more critical at higher K where the required frequency range increases asymmetrically with respect to ω_{inj} .

C. ILO Bandwidth

Similar to a PLL, an ILO tracks the input jitter within its BW and rejects it outside the BW. The BW for an ILO with a parallel RLC tank has previously been calculated [1], [12]. To calculate the BW of an ILO with series RL tank, we apply small phase perturbation technique to an ILO steady-state phase, similar to [1]

$$\theta = \theta_{ss} + \hat{\theta}, \quad \hat{\theta} \ll 1. \quad (13)$$

To calculate the BW, we first replace θ in (6) with (13)

$$\frac{\left(\frac{d\hat{\theta}}{dt} + \omega_{inj}\right)^3}{\omega_0^2} - \frac{d\hat{\theta}}{dt} = \omega_{inj} - \left(\frac{\omega_0}{Q \cdot \left(1 - \frac{1}{Q^2}\right)^{1.5}}\right) \cdot \frac{K \cdot \sin(\hat{\theta} + \theta_{ss})}{1 + K \cdot \cos(\hat{\theta} + \theta_{ss})}. \quad (14)$$

Using Taylor expansion, the following simplification can be made

$$\frac{K \cdot \sin(\hat{\theta} + \theta_{ss})}{1 + K \cdot \cos(\hat{\theta} + \theta_{ss})} = \frac{\hat{\theta} \cdot (K + \cos \theta_{ss})}{(1 + K \cdot \cos \theta_{ss})^2} + \frac{\sin \theta_{ss}}{1 + K \cdot \cos \theta_{ss}}. \quad (15)$$

By replacing (15) in (14) and ignoring second and higher order terms of $d\theta/dt$, (14) is simplified to

$$\frac{d\hat{\theta}}{dt} = \frac{-\omega_0}{2Q} \cdot K \cdot \frac{K + \cos \theta_{ss}}{(1 + K \cdot \cos \theta_{ss})^2} \times \left(\frac{2}{\left(1 - \frac{1}{Q^2}\right)^{1.5}} \cdot \frac{1}{\frac{3\omega_{inj}^2}{\omega_0^2} - 1} \right) \cdot \hat{\theta}. \quad (16)$$

From (16), the BW of an ILO with series RL is calculated

$$\text{Series RL : } BW_s = BW_P \cdot \left(\frac{2}{\left(1 - \frac{1}{Q^2}\right)^{1.5}} \cdot \frac{1}{\frac{3\omega_{inj}^2}{\omega_0^2} - 1} \right) \quad (17)$$

$$\text{Parallel RLC : } BW_P = \frac{\omega_0}{2Q} \cdot K \cdot \frac{K + \cos \theta_{ss}}{(1 + K \cdot \cos \theta_{ss})^2}. \quad (18)$$

As shown by (17), the BW of an ILO using a parallel tank model is inversely proportional to Q . Thus, the product of normalized bandwidth ($= BW/\omega_{inj}$) and Q for a parallel tank is only dependent on K and θ_{ss} . Fig. 10 compares the calculated ILO BW for the two tank models for different Q and K values. For a constant K and higher $Q (> 5)$, the BW estimated from parallel tank model matches well with series tank model. However, as Q reduces, the parallel tank model underestimates the BW and fails to predict the asymmetry in BW around zero phase shift [see Fig. 10(a)]. For a constant low $Q (= 2.5)$, the parallel tank model again underestimates the BW and fails to predict the asymmetry. As K increases, the error in approximating ILO BW, using a parallel tank model, increases [see Fig. 10(b)]. At the lock boundary, the ILO BW significantly drops due to quasi-lock effects [17]. By increasing K , quasi-lock effects are pushed out to $|\theta_{ss}| > 90^\circ$ which significantly reduces the ILO BW variation to $< 2x$ for 180° phase shift. In summary, an LC-ILO with high injection strength is desirable for forwarded-clock data receiver as it successfully deskews the clock within 1UI without its BW significantly degrading at $\pm 90^\circ$ with respect to the BW at zero phase shift.

III. RECEIVER OVERVIEW

To evaluate an ILO-based phase shifter in a data link, the forwarded-clock data receiver, shown in Fig. 11, is implemented. It consists of an injection-locked LC oscillator, clock buffering, and a half-rate interleaved data sampler. The ILO locks to the differential injection clock, clk_{inj} , within the lock range of the ILO. The ILO phase shifts the injection clock

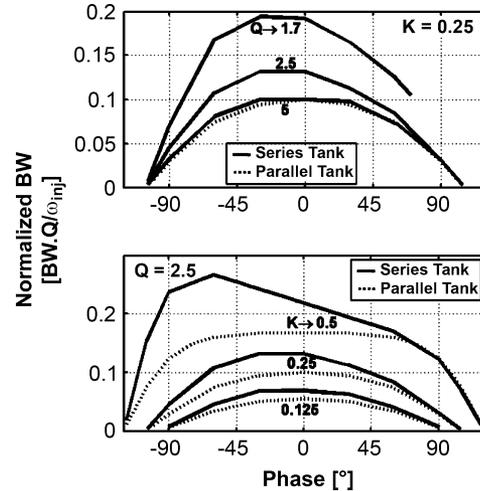


Fig. 10. Calculated ILO BW for series RL versus parallel RLC tank for constant $K = 0.25$ and varying Q , and constant $Q = 2.5$ and varying K , respectively.

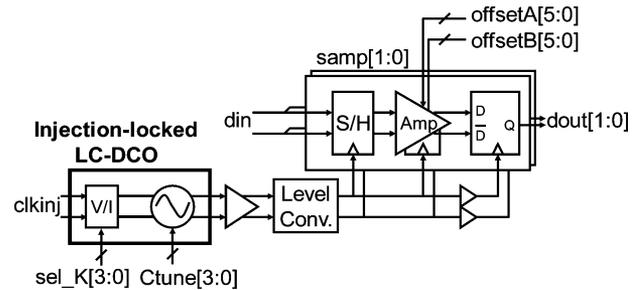


Fig. 11. Proposed ILO-based clock deskew and data sampler for a forwarded-clock link.

in excess of 180° (1UI), by digitally tuning the free-running oscillator frequency away from the injection clock frequency as described in Section II. The free-running frequency of the digitally-controlled oscillator (DCO) is tuned with a 4-b binary control word, $Ctune$. The ILO also acts as a low-pass jitter filter for the injected clock signal. The injection strength is controlled with a 4-b thermometer control word, sel_K , which tunes both the BW and phase shift resolution of the ILO. The phase-shifted clock is driven to the data samplers through a level converter that amplifies the oscillator output to full CMOS levels. The half-rate data samplers have a sample-amplify-regenerate architecture and serve as a 1:2 data demultiplexer. The amplifier within each sampler has 6-b digital offset control, $offsetA$ and $offsetB$, to compensate for input-referred sampler offset and to enable measurement of data eye voltage margins.

An interesting and unique feature of the ILO-based architecture is that a single digital word controls the oscillator tuned frequency and phase shift simultaneously. As such, there is no need for an explicit frequency detector or to characterize the lock range of the ILO. The optimal phase-tuning code can be determined during link training by sweeping through all the tuning codes and choosing the setting with the largest eye margins. Codes that are outside of the locking range will be evident by their poor BER. This method is used later to measure the receiver timing margins in Section VI.

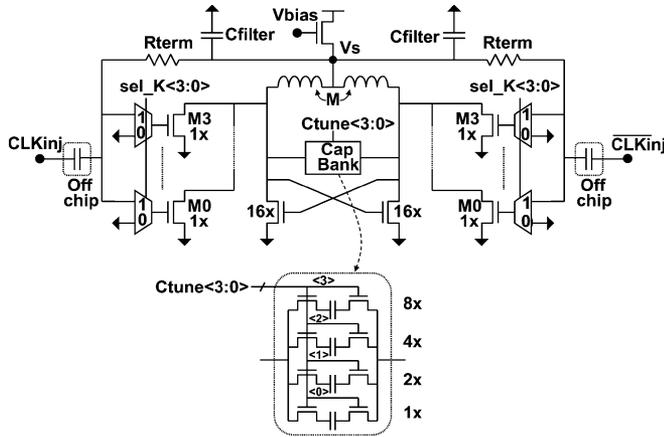


Fig. 12. Schematic of the injection-locked LC-DCO.

The primary goal of the prototype is to demonstrate the ILO phase tuning technique in a receiver that is optimized for high per-pin data rate and good power efficiency. The performance target for this prototype is limited not by the 45-nm CMOS process speed, but by our ability to test the data receiver only up to 27 Gb/s using the available BERT equipment. As such, we designed for a data rate target of 27 Gb/s. Simulations indicate that both the ILO and data sampler could operate beyond 27 Gb/s.

IV. INJECTION-LOCKED LC-DCO DESIGN

The ILO, shown in Fig. 12, is based on a differential LC-DCO. The key features of the ILO design are that both the oscillator free-running frequency and injection strength are digitally controlled, and injection devices use replica-biasing to reduce susceptibility of injection strength to PVT and biasing variations. The DCO is implemented as a differential cross-coupled LC oscillator with a center frequency of 13.5 GHz. The inductor is a differential interleaved design with differential inductance of 2×0.38 nH and a Q of 3 to 4 over a low-resistivity substrate. The overall tank Q is ~ 2.5 when accounting for other tank loss such as shunt loss of the capacitor bank and current-injecting devices. A 4-bit thermometer code adjusts the injection strength from 0 (no injection) to 0.25 in four equal steps by switching on or off segments of the V/I converter. The network formed by the on-chip termination resistor (R_{term}) and filtering capacitor (C_{filter}) copies the gate bias of cross-coupled devices, which is approximately equal to V_s , onto the gate of current-injecting devices, M3-M0. Because the cross-coupled and current-injecting devices have nearly identical biasing conditions, their transconductance (g_m) ratio is independent of PVT and biasing. It should be noted that the voltage drop across the inductor due to series resistance will cause a slightly higher V_{gs} for the injection devices. For this design, the discrepancy is in the range of 25 mV. By setting the amplitude of the injection clock to match the oscillator amplitude, the injection strength is primarily determined by the ratio of the injection and cross-coupled devices. For example, a variable gain amplifier (VGA) in the injection path could be adapted to balance the amplitudes of the oscillator output and injection. The control loop would increment or decrement the

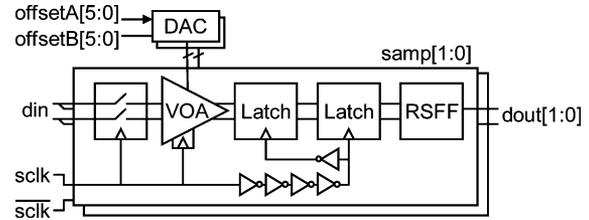


Fig. 13. Half-rate interleaved data sampler with per-sampler programmable offset.

VGA gain based on a relative comparison of the two voltages using peak detectors. However, for design simplicity, the amplitude control loop has not been implemented in this prototype.

The digitally controlled switch-capacitor bank tunes the free-running frequency of DCO to adjust the phase of the 13.5 GHz forwarded clock and also compensate for PVT. From (8), the required DCO frequency range to achieve -90° to 90° of phase tuning for $K = 0.25$ is calculated to be 12.7–14.6 GHz. The DCO was designed to tune from 11.75 to 15.25 GHz which compensates for $\leq \pm 5\%$ frequency shift due to PVT. The frequency steps are 200 to 300 MHz which result in relatively coarse phase tuning of $15\text{--}30^\circ$ for $K = 0.25$. Finer phase tuning can be easily accomplished by reducing the incremental capacitance value. From (17), the ILO provides a simulated filtering bandwidth of 390 and 700 MHz at zero phase shift for $K = 0.125$ and $K = 0.25$, respectively.

V. DATA SAMPLER DESIGN

The data sampler design is shown in Fig. 13. A full-rate data pattern is sampled and resolved by two differential half-rate sampling paths. The sampler paths use a sample-amplify-regenerate architecture that is popular for data links and ADCs. The receiver sampling aperture is set by fast NMOS sampling switches at its input. This is followed by a variable offset amplifier (VOA). Each VOA has its own independent 6-b offset control for link voltage margining and to independently calibrate the offset in each path. The VOA schematic is shown in Fig. 14 and is similar to the design described in [18]. Voltage offset is achieved by steering bias current through two differential pairs with intentional 2:1 device width offset. The bias currents are generated using 6-b differential current steering DACs. The VOA design further partitions the pMOS current source for each differential pair into two devices to enable coarse and fine offset adjustment. The voltage control for the smaller of the two devices can be connected to either the same bias voltage as the larger device (for coarse resolution) or the bias for the other differential pair (for fine resolution). The simulated 6-b offset resolution near zero offset in coarse and fine modes are 2.5 and 1.2 mV, respectively. The simulated gain and BW are 8.9 dB and 10.9 GHz near the zero offset setting. A precharge switch across the outputs of the amplifier reduces sampler hysteresis by partially resetting the output between samples. This effectively relaxes the amplifier BW requirement for a fixed sensitivity target.

The VOA is followed by two clocked, regenerative latches and an asynchronous flip-flop, similar to [19]. The cascaded latches are used to improve sensitivity at this fast sampling rate.

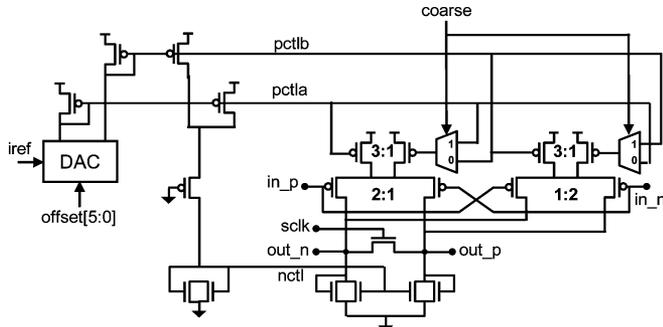


Fig. 14. VOA with coarse/fine resolution.

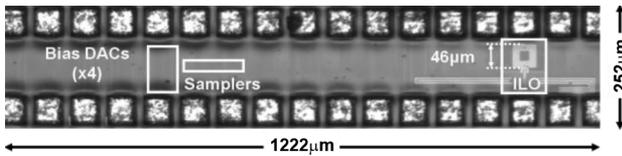


Fig. 15. Die micrograph.

The clock is buffered in the same direction as the data starting at the input data sampling switches. Starting the clock at the sampling switches rather than running it in the opposite direction minimizes the impact of supply-noise-induced jitter in the clock path. Since the sampling jitter is primarily set by the clock at the sampling switches, minimizing the depth of the clock buffer chain to this point minimizes the sampler timing uncertainty. The disadvantage of this approach is that it relies on unregulated inverter delay to set the time allowed for the VOA to settle. This time does not increase at lower sampling rates, although it will track process. For this design, the optimal delay between the sampler clock and latch clock is ~ 20 ps at 13.5 GHz, which corresponds to about 1.5 time constants for the VOA.

The simulated input-referred noise for the complete sampler path is 1.0 mV-rms. The sampler input-referred metastable range is less than 2 mV.

VI. MEASUREMENT RESULTS

A prototype chip for the ILO-based data receiver is implemented in a 45 nm 1.1 V 9M digital CMOS process. The die micrograph is shown in Fig. 15. The injection-locked LC-DCO and 2-way interleaved data samplers occupy an area of 0.01 mm² and 0.005 mm², respectively, and consume 15 and 28 mW, respectively. The chip is microprobed and controlled through a PC using scan chain registers. The reference current for the DACs is generated from a differential off-chip reference voltage. The ILO output is buffered off chip using an open-drain buffer to minimize jitter caused by buffering. The clock and data sequences from the data samplers are driven off chip using large inverter buffers.

The measurements in this section characterize the ILO in terms of lock range, phase tuning, jitter transfer function, and power supply sensitivity. Where applicable, the measured results are compared with the models described in Section II. Excellent correlation between the model and measurements confirm that the validity of the series-RL model for low- Q , high- K ILOs.

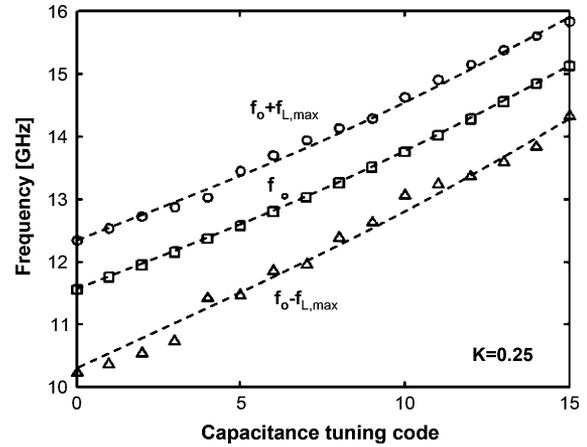
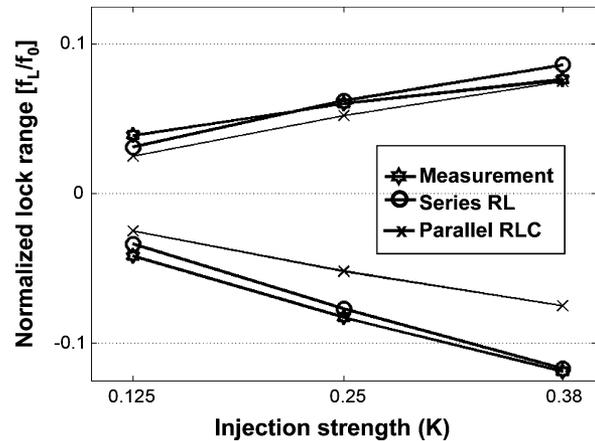


Fig. 16. Injection-locked LC-DCO tuning range and lock range plot.

Fig. 17. Measured and calculated lock range (normalized) of injection-locked LC-DCO at $f_o = 12.4$ GHz.

A. Lock Range

Fig. 16 shows the tuning range of the free-running DCO as the capacitor bank is scanned through all 16 codes. The DCO operates from 11.6 to 15.1 GHz with frequency steps of 200–300 MHz. On the same plot, the injection locking range of the DCO is also shown as f_{inj} is swept about a given f_o of the DCO. The measurement results for $K = 0.25$ shows asymmetric lock range at lower values of f_o where the tank- Q is the lowest. This asymmetric behavior at lower tank- Q is qualitatively consistent with the series-RL model results described in Section II-A. Fig. 17 compares the measured frequency lock range at $f_0 = 12.4$ GHz for three different K values with the series and parallel tank models, assuming Q of 2.5. K is set to 0.125 and 0.25, using the digital injection strength control with the same injection voltage amplitude. The measurement at $K \sim 0.38$ is obtained by setting the injection strength code to its maximum value ($K = 0.25$) and then increasing the injection voltage amplitude. The measured locking range correlate well with the proposed series-RL model, while the parallel-RLC model underestimates the lower end of the frequency locking range by up to 35%.

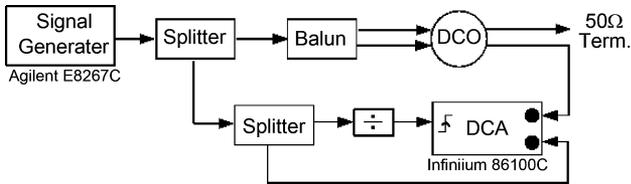


Fig. 18. Test setup for measuring the phase deskew of the ILO.

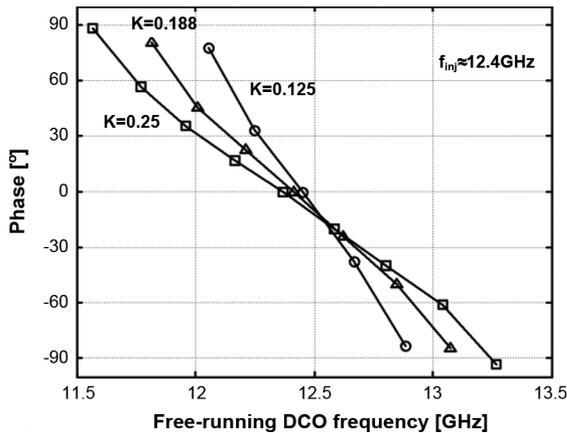


Fig. 19. Measured phase deskew of the injected clock through the ILO.

B. Phase Shift

The phase shift between the injected clock and oscillator output clock is measured using the test setup shown in Fig. 18. In this setup, the DCO output phase is shifted by digitally tuning the free-running frequency of the DCO. The injected clock serves as the phase reference for measuring changes in the DCO output phase. The phase tuning curves for three K values is shown in Fig. 19. These phase tuning curves are analogous to the calculated curves shown in Fig. 9 based on ILO models. Note that, unlike in Fig. 9, the measured phase steps are quantized due to the digital nature of the oscillator frequency tuning. The results shown in Fig. 19 confirm that increasing K improves both phase linearity and resolution. However, it also increases the required frequency tuning range of the DCO to achieve $\pm 90^\circ$ phase tuning. For $K = 0.25$, the injected clock is deskewed from -93° to $+88^\circ$. Fig. 20 compares the measured phase tuning range for $K = 0.125$ and $K = 0.38$ along with calculated predictions based on the series and parallel tank models, assuming Q of 2.5. As with the locking range measurements, the series model matches well with the measured results and, unlike the parallel model, it explains the observed asymmetry in the frequency-phase transfer curves for higher K of 0.38. Note that although measured at $K > 0.25$ to verify the proposed model for different K values, the ILO for this prototype is mainly designed for $K \leq 0.25$. In order to design the ILO with $K > 0.25$, the DCO frequency tuning range should be increased to compensate for PVT.

C. ILO Bandwidth

To measure the jitter transfer function from the injected clock input to the output, the ILO is injected with a clock signal whose phase is modulated at frequency f_m . Consequently, the spectrum of both injected clock and ILO output clock contain the

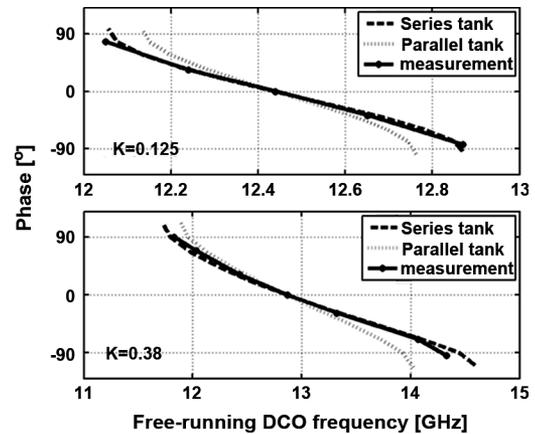
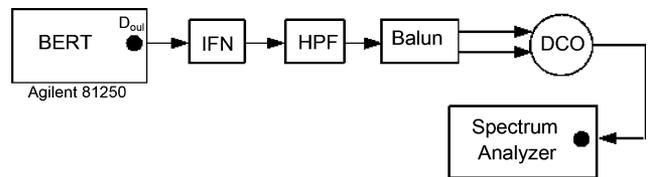
Fig. 20. Measured and calculated phase deskew with $Q = 2.5$.

Fig. 21. Test setup for measuring the jitter transfer function for the ILO.

main carrier, f_{inj} , and two sidebands that are located $\pm f_m$ away from f_{inj} . By measuring the spectrum amplitudes at the carrier and sideband frequencies and using Bessel function properties, ILO input and output jitter are calculated similar to the method described in [20]. Fig. 21 shows the test setup for measuring the ILO jitter transfer function and BW. A BERT generates an alternating data sequence that serves as the injection clock for the ILO. The BERT data output is used rather than the clock output because only the data output can be modulated. However, the maximum frequency for the alternating data pattern is limited by the BERT to be 6.75 GHz, which is well below the ILO frequency range. To bypass this equipment limitation, a one-third rate clock pattern is multiplied prior to injecting it into the DCO. To multiply the clock, the BERT output is fed into an impulse forming network (IFN), which generates the odd harmonics of the sub-rate clock. Then, the clock signal is passed through a high-pass filter to suppress the fundamental while passing the 3rd harmonic, which is at the desired injection frequency. Higher-order harmonics are not significant due to the limited pulsewidth of the IFN and the finite BW of the high-pass filter. The band-pass characteristics of this setup must be wide enough to pass the desired clock frequency as well as the modulated jitter sidebands, which can have significant spectral components in excess of 1 GHz. In our case, the BW of the clock multiplier limited the maximum frequency for the jitter-modulated clock to about 12.4 GHz. For the sake of consistency, the phase shifting measurements (see Section VI-B) are taken at this same frequency rather than at 13.5 GHz.

The ILO jitter transfer function, measured at 0° phase shift over a range of injection strengths, is shown in Fig. 22. This data demonstrates that the ILO behaves as a first-order low-pass filter that rejects high-frequency jitter and duty-cycle error present in the injected clock. Based on Fig. 22, the -3 dB jitter tracking

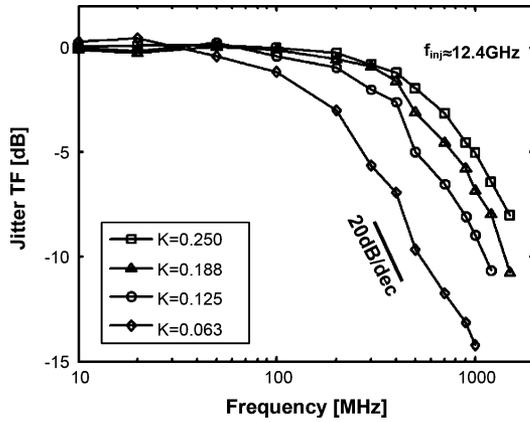


Fig. 22. Measured jitter transfer function for the ILO.

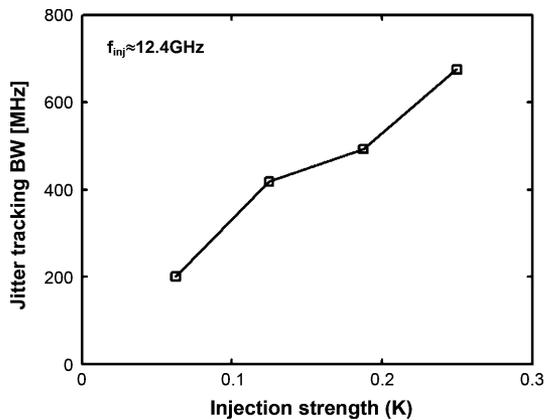


Fig. 23. Measured jitter tracking BW as a function of injection strength at 0° phase deskew.

BW is summarized for different K values in Fig. 23. The BW can be tuned through the digital control of K , which is consistent with the analytical results of (17) shown in Section II-C. The measured jitter tracking BW as a function of phase tuning is plotted in Fig. 24 for $K = 0.125$ and $K = 0.25$. For comparison, the calculated BW assuming a tank Q of 2.5 and using both the series-RL and parallel-RLC tank models is also plotted. For $K = 0.125$, the tracking BW is symmetric and shows the expected monotonic reduction as phase is tuned away from 0°; the series model tracks the measured results. For $K = 0.25$, however, the tracking BW is asymmetric, which is also predicted by the series tank model. The series tank model closely approximates the BW with deskew between $\sim -70^\circ$ and 90° , beyond which the error is attributed to K variation of the ILO across its tuning range. Since there is no amplitude tracking mechanism in this prototype, the amplitude of the VCO changes over its frequency tuning range. This amplitude variation effectively changes the values of K , predominantly at the extremes of the frequency tuning range, or phase deskew range. To verify this postulation, estimated values of K at each frequency (based on Fig. 5 and circuit simulation) is included in the model, and this reduces the error significantly, as shown in Fig. 24. Although not implemented in this prototype, the DCO with an amplitude control loop is recommended. This guarantees a predictable and constant K based on DCO digital control set and independent of the oscillator amplitude which avoids approximating K from

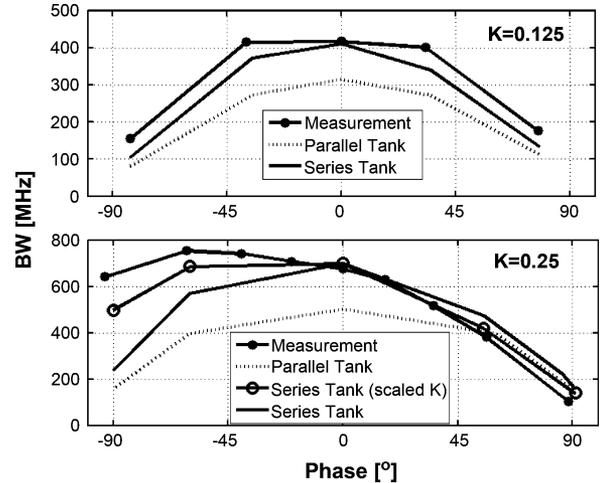


Fig. 24. Measured jitter tracking BW for the ILO.

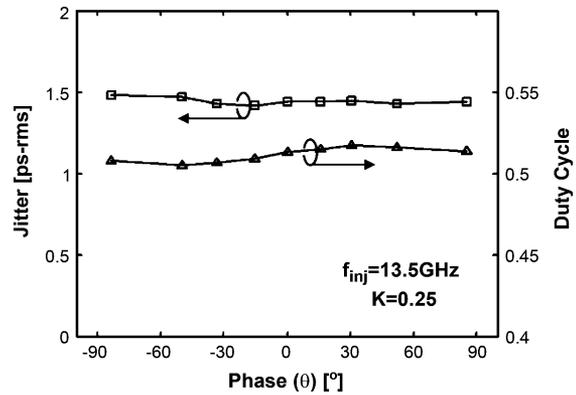


Fig. 25. Measured random jitter and duty cycle of ILO output as a function of phase deskew.

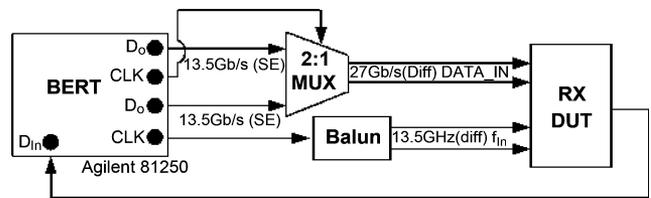


Fig. 26. Test setup for measuring BER.

the complex tank amplitude equation. Fig. 25 shows that the measured random jitter and duty cycle of the ILO as a function of the phase deskew is well behaved.

D. Power Supply Induced Jitter

The sensitivity of the ILO to power supply noise is measured for both free-running and injection-locked conditions. The measurements characterize the sensitivity to static power supply noise (rather than dynamic supply noise) due to our limited ability to inject known amounts of high frequency power supply noise in this test setup. The DC power supply sensitivity of the free-running oscillator is 1075 MHz/V near 13.5 GHz. When injection locked at 13.5 GHz with $K = 0.25$, the measured phase sensitivity of the ILO output is 16 ps/V. This jitter measurement result correlates well with the measured phase tuning data

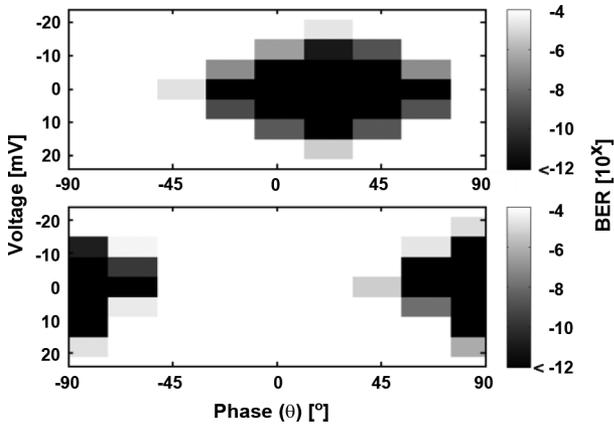


Fig. 27. Measured receiver BER eyes at 27 Gb/s for $K = 0.25$ and 95 mV-pp-diff data amplitude with $2^{15} - 1$ PRBS pattern.

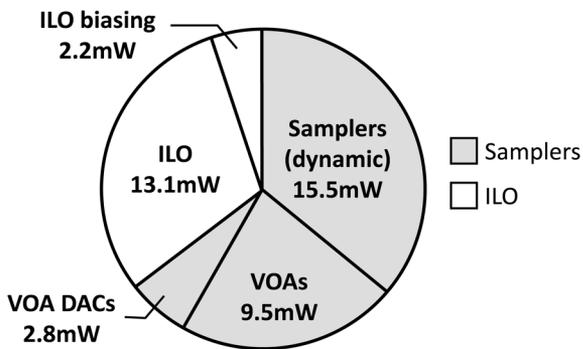


Fig. 28. Measured receiver power breakdown (27.0 Gb/s, $2^{15} - 1$ PRBS, BER $< 10^{-12}$).

in Fig. 19, which shows 90° (18.5 ps @ 13.5 GHz) phase shift for 1 GHz frequency tuning. It is also apparent from this figure that jitter sensitivity improves as the injection strength increases since, to first order, the frequency sensitivity is independent of injection strength. To get a feel for the significance of the jitter sensitivity to supply noise, it is useful to consider the UI jitter for reasonable power supply noise amplitudes. Based on the measured data, 10% power supply noise would result in 1.8 ps-pp jitter at 13.5 GHz, which corresponds to 0.05UI timing jitter at 27 Gb/s.

E. BER Eye

Fig. 26 shows the test setup for measuring the BER eye of the receiver using the ILO to sweep the sampling phase and the OA to sweep sampling voltage. Two single-ended $2^{15} - 1$ PRBS data sequences from the BERT at 13.5 Gb/s are multiplexed to produce a 27 Gb/s differential data sequence. The BERT also provides the injected clock frequency at 13.5 GHz for the receiver. The output of the receiver is fed back to the BERT pattern checker. The BER eye diagrams in Fig. 27 are generated by sweeping the voltage offset of the VOAs and phase of the ILO. As expected, the ILO phase tuning range is just adequate to cover 1UI for this half-rate data receiver. Note that the phase tuning range for this phase deskewing technique is finite, and therefore it cannot sweep across multiple UI in a continuous fashion. As a result, the center of the eye could be anywhere

TABLE I
MEASUREMENT SUMMARY ($K = 0.25$)

| | |
|--|--|
| Process technology | 45nm 9M CMOS |
| Supply voltage | 1.1V |
| DCO tuning range | 11.6 - 15.1GHz (200 - 300MHz steps) |
| Phase deskew resolution | $16^\circ - 32^\circ$ |
| Lock range, $f_{\text{osc}} = 13.5\text{GHz}$ | 12.62 - 14.29GHz |
| Power supply sensitivity (DC), $f_{\text{inj}} = 13.5\text{GHz}$ | 1075MHz/V (free-running) 16ps/V (injection locked) |
| Receiver sensitivity @ 27.0Gb/s, BER $< 10^{-12}$, $2^{15}-1$ PRBS | 46mV _{pp-diff} |
| Power @ 13.5GHz / 27.0Gb/s (including bias DACs) | ILO: 15mW Data samplers: 28mW |
| Area (including bias DACs) | ILO: 0.010mm ² Data samplers: 0.005mm ² |

TABLE II
PERFORMANCE COMPARISON

| | [21] | [15] | [22]* | This work |
|----------------------------------|-----------|---------------|---------------|-----------------|
| Data Rate [Gb/s] | 25 | 40 | 40 | 27 |
| Architecture | CDR | CDR | CDR | Forwarded-clock |
| Demux | 1:4 | 1:8 | 1:1 | 1:2 |
| Power [mW] | 98 | 72 | 32 | 43 |
| Power efficiency [mW/Gb/s] | 3.9 | 1.8 | 0.8 | 1.6 |
| Area [mm ²] | 0.07 | 0.03 | 0.06 (estim.) | 0.015 |
| Sensitivity [mV _{ppd}] | 620 | 400 (estim.) | 650 | 46 |
| Technology | 90nm CMOS | 65nm SOI CMOS | 90nm CMOS | 45nm CMOS |

*Excludes equalizer

within the finite tuning range. The two extreme cases of this are shown in Fig. 27 when the eye is at the center and edge of the phase tuning range, respectively. Regardless, the eye dimensions remain comparable.

F. Power Consumption and Measurement Summary

Operating at 27 Gb/s, the complete receiver consumes 43 mW from a 1.1 V power supply. This corresponds to a power efficiency of 1.6 mW/Gb/s. The power breakdown for the data receiver, including the ILO and data samplers, is shown in Fig. 28. Table I summarizes the complete receiver performance measured at $K = 0.25$. This work is comparable to the lowest reported power efficiency and area for CMOS data receivers above 20 Gb/s, as shown in Table II. It is worth noting that the performance specifications for [15], [21], and [22] include the power and area for CDRs, whereas the present work does not include active clock-data tracking circuitry. However, the present work is designed for an input sensitivity that is about an order of magnitude better than reported for the other receivers.

VII. CONCLUSION

A general model for injection-locked LC oscillators, based on a series-RL parallel-C tank, is proposed. Unlike the parallel RLC tank approximation used in previous ILO models, the

series RL tank is valid for any tank Q and injection strength. The proposed model, confirmed with measurement results, reveals important properties of low- Q and/or high- K ILOs such as asymmetry in the lock range, reduced phase shift, and higher BW. A 27 Gb/s forwarded clock receiver with a low- Q tunable- K injection-locked LC oscillator is implemented in CMOS digital process with low-resistivity substrate. The injection-locked DCO deskews the forwarded clock across 1UI, rejects the high-frequency forwarded clock jitter with the BW of 200–400 MHz across 1UI at $K = 0.125$. Owing to the simplicity of proposed clocking architecture, the entire receiver occupies 0.015 mm² and achieves an overall power efficiency of 1.6 mW/Gb/s.

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