March 29, 2010

ECEN 689: High-Speed Links

Homework #6

Due: 4-7-2010, 9:10AM

Homeworks will not be received after due.

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1. **TX FIR Equalization**. This problem investigates TX FIR equalization using the 12" Backplane channel from HW3, "**peters_01_0605_B12_thru.s4p**". For parts (a) and (b), use the example matlab code "**channel_data_pulse_pda.m**" and produce the following 2 graphs:
   a. **Peak-Distortion Eye Height versus FIR tap number at 5, 10, and 16Gbps** (3 lines). For the tap numbers, use 1-tap (no equalization), 2-tap (1-post), 3-tap (1-pre and 1-post), and 4-tap (1-pre, 2-post). Don't restrict the TX equalizer resolution for this graph.
   b. **10Gb/s Peak-Distortion Eye Height versus Equalizer Resolution with 2, 3, and 4-tap equalization** (3-lines). For the tap resolution sweep, use 3, 4, 5, 6, and also include the infinite resolution data.

Note: The above matlab code also requires the "**tx_eq.m**" function. Also, this matlab code is only reference code. Feel free to modify and improve upon the code as you wish.

   c. **Design a 10Gb/s TX Driver with Equalization**. Modify one of your drivers from Homework 4 to include FIR equalization.
      i. The maximum output voltage swing can be anywhere from 350mVppd (min.) to 1Vppd (max.). This gives you the flexibility to choose whichever driver you wish – from low-swing voltage-mode to current-mode.
      ii. Use the results from part (a) and (b) to justify your tap number and resolution.
      iii. **Include 2 10Gb/s PRBS eye diagrams** – one without equalization (all weight on cursor) and one with the proper equalization taps enabled. Import the s-parameter file into your Cadence simulation to produce the eye diagrams. Make sure the channel is properly terminated at both ends. Note, as you will have some additional driver capacitance, the equalization taps may change slightly.
      iv. The driver and at least one predriver stage should be full-transistor level design. The other blocks (PRBS, delay elements, etc) can be macromodeled.
      v. Report transmitter power consumption, power efficiency (mW/Gb/s), and 10Gb/s eye height and width.

2. **RX CTLE Equalization**. Design a 10Gb/s active CTLE to meet the following specifications:
   a. Min peak gain at Nyquist (5GHz) of 6dB
   b. Zero frequency tunable from a minimum range of 500MHz to 2GHz
   c. Minimum tunable peaking (magnitude difference between Nyquist and low frequency response) range of 12dB (Example: +6dB at 5GHz and -6dB at low frequency).
   d. Load capacitor = 20fF
      i. **Produce frequency response plots** showing the zero and peaking tenability.
      ii. **Produce a 10Gb/s PRBS eye diagram** with the 12" Backplane channel s-parameter channel output as the input to the CTLE. Optimize the CTLE settings for optimal eye opening.
      iii. Report CTLE power, power efficiency (mW/Gb/s), and 10Gb/s eye height and width.

3. **RX DFE Equalization**. Design a 10Gb/s 2-tap DFE.
   a. Use one of the comparators you designed in Homework 5 in your design. Note, you will probably have to speed this design up – as you will need a 5GHz clock if you implement a ½ rate design.
   b. The only thing that has to be transistor level is the comparator. The rest of the blocks (summer, feedback taps, other logic) can be macromodeled. Note for the summer model, make sure to capture the RC settling if you use a linear resistive load summer. Feel free to investigate an integrating architecture if you prefer.
   c. **Produce a 10Gb/s PRBS eye diagram at the summer output** with the 12" Backplane channel s-parameter channel output as the input to the DFE. Optimize the DFE settings for optimal eye opening at the input of the comparator (summer output).
   d. Report DFE power, power efficiency (mW/Gb/s), and 10Gb/s eye height and width.
   e. Note, you will have to synchronize the DFE with the incoming data stream. A good way to do this is with an initial "lone pulse" input pattern. Adjust your comparator clock to sample near the peak of the lone pulse. Then simulate with the PRBS data.