March 3, 2010

# ECEN 689: High-Speed Links

Homework #4

Due: 3-10-2010, 5:00PM

**Homeworks will not be received after due.**

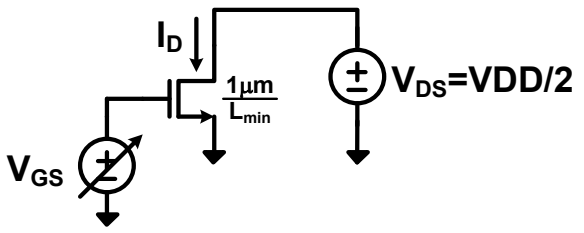
Instructor: Sam Palermo

This homework requires transistor-level circuit design. You may use any CMOS technology to solve the problem, as long as it is a 90nm or mode advanced technology node (shorter channel length). For students who do not have access to a design kit, instructions on how to access the default 90nm CMOS transistor models are posted on the website. For this 90nm technology assume a nominal 1.2V supply.

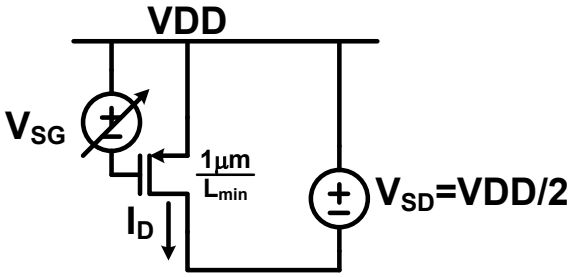
1. **CMOS Technology Characterization**. In order to estimate what level of performance is achievable with a given process technology, it is useful to run some initial characterization simulations.
   a. For both NMOS and PMOS transistors with dimensions W=1µm and L=$L_{min}$, **plot $f_T$ versus $|V_{GS}|$ and also versus $I_D$ – 4 plots total (2 per transistor)**. Use the test circuits below. The easiest way to do this is to run a DC sweep with $|V_{GS}|$ varying from 0 to VDD and plot

$$f_T = \frac{g_m}{2\pi C_{gg}}$$

   where $C_{gg}$ is the total gate capacitance. For the plot versus $|V_{GS}|$, use a linear scale for both axes. For the plot versus $I_{DS}$, use a log scale for the x-axis (current) and a linear scale for the y-axis (frequency).

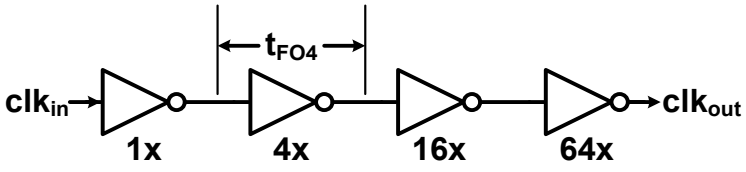



(i) NMOS $f_T$ test circuit



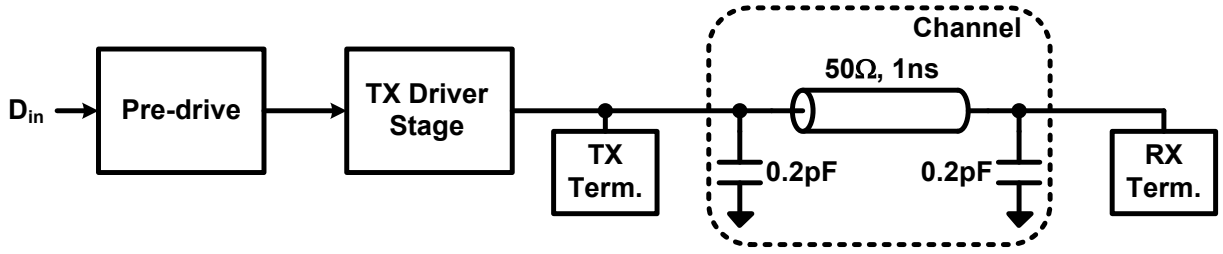

(ii) PMOS $f_T$ test circuit

   b. **Find the FO4 inverter delay**. Refer to the instructions on how to use the default 90nm CMOS technology models for more details on how to setup the test circuit. For the inverters use minimum channel length and an NMOS unit finger width of 1µm. Size the P/N ratio of the inverter for equal rise and fall delay, measured from 50% of the input to 50% of the output. However, don't exceed a P/N ratio of 3, i.e. if the simulations show that a ratio greater than 3 is required for equal delay then just use 3 and accept the slight delay difference.




FO4 test circuit

2. **10Gb/s Low-Swing Driver and Termination Design**.
   a. Design both a differential current-mode CML driver and a differential low-swing voltage-mode driver to support an output swing of $300mV_{ppd}$.
      i. For the CML driver, the output tail current source should be implemented at the transistor level, but you may use a current mirror that has an ideal current source to produce the bias for the output stage tail current source.
      ii. For the voltage-mode driver, any regulator voltage can be implemented with an ideal voltage source, i.e. you don't have to design the regulator.
   b. Include one pre-driver stage before the driver output stage. This may be a simple inverter pre-driver or something more fancy if you want.
   c. The driver should be terminated on-chip both at the transmitter and the receiver. The termination should be designed to handle a temperature variation from 0 to 100C **OR a variation of ±15% from the nominal 25C value if the temperature variation simulation doesn't work**. Passive termination may be used, however a realistic model including parasitic capacitance must be used, i.e. from a design kit or taken from the table in lecture 10. Choose whichever termination scheme you think is most appropriate (AC vs DC-coupled, Single-ended vs Differential) and explain your choice.
   d. Since the emphasis of this problem is the driver design, in your simulations use a simple channel consisting of TX output cap = RX input cap = 200fF and an ideal 50Ω, 1ns transmission line.




Block diagram for Problems 2 &3.

   e. **Turn-in the following for your design**
      i. Schematics with details of transistor sizing.
      ii. A 10Gb/s eye diagram at the RX. Use a pseudo-random input sequence of $2^7$-1 or higher to produce the eye diagram.
      **iii.** Plot the return loss versus frequency looking back into the transmitter at 0, 25, and 100C. For this, program the termination to yield the best performance at each temperature. **Note: if your temperature variation simulations don't work, then just turn in one plot at 25C and data showing that your termination can tune ±15%.**[1]
      iv. Compare the power consumption of the two drivers. Break down the power into pre-driver and output stage power.

For the Low-Swing Voltage-Mode Driver, refer to the 2 low-swing voltage-mode papers posted on the website for reference.

[1] Note: ±15% is probably sufficient for only temperature variations. To handle process, voltage, and temperature variations, you would probably need to increase this range to ±30%.

3. **10Gb/s High-Swing Driver and Termination Design**.
   a. Repeat the steps of problem 2 for both a differential current-mode CML driver and a differential high-swing voltage-mode driver to support an output swing of $1V_{ppd}$.
   b. For the current-mode driver, you can probably use the same driver. You will probably just need to increase the output stage and perhaps the pre-driver sizing.
   c. For the voltage-mode driver, a high-swing architecture will need to be used. Refer to the 2 high-swing voltage-mode papers posted on the website for reference.