January 20, 2021

# ECEN 720: High-Speed Links

Homework #1

Due: 1-27-2021, 11:59PM
**Homeworks will not be received after due.**
Instructor: Sam Palermo

Read the following high-speed link overview material and recent design papers which are posted on the website.

## Link Overview Material

1. S. Palermo, "CMOS Nanoelectronics Analog and RF VLSI Circuits. Chapter 9: High-Speed Serial I/O Design for Channel-Limited and Power-Constrained Systems," McGraw-Hill, 2011.
2. M. Horowitz *et al*., "High-speed electrical signaling: overview and limitations," *IEEE Micro*, vol. 18, no. 1, Jan./Feb. 1998, pp. 12-24.

## Recent Design Papers

### State-Of-The-Art Backplane Link (Non-ADC-based)

3. J. Bulzacchelli *et al*., "A 28-Gb/s 4-tap FFE/15-tap DFE serial link transceiver in 32-nm SOI CMOS technology," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, Dec. 2012, pp. 3232-3248.

### Low-Power Source-Synchronous Link

4. M. Mansuri *et al*., "A scalable 0.128–1 Tb/s, 0.8–2.6 pJ/bit, 64-lane parallel I/O in 32-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, Dec. 2013, pp. 3229-3242.

### ADC-Based Backplane Link

5. E.-H. Chen, R. Yousry, and C.-K. Yang, "Power optimized ADC-based serial link receiver," *IEEE J. Solid-State Circuits*, vol. 47, no. 4, Apr. 2012, pp. 938-951.

### Optical Interconnect Link

6. S. Palermo *et al*., "A 90nm CMOS 16Gb/s transceiver for optical interconnects," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, May 2008, pp. 1235-1246.

**Write a one-page summary report on one of the above recent design papers (3-6).**