Texas A&M University
Department of Electrical and Computer Engineering

ECEN 720 – High-Speed Links

Spring 2023

Exam #2

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- Please write your name in the space provided below
- Please verify that there are **7** pages in your exam
- Good Luck!

Problem	Score	Max Score
1		35
2		30
3		35
Total		**100**

Name: SAM PALERMO

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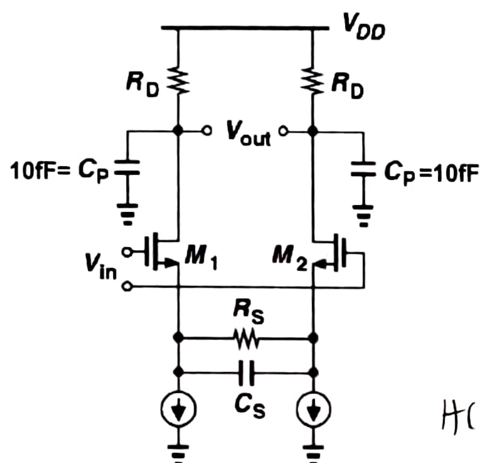
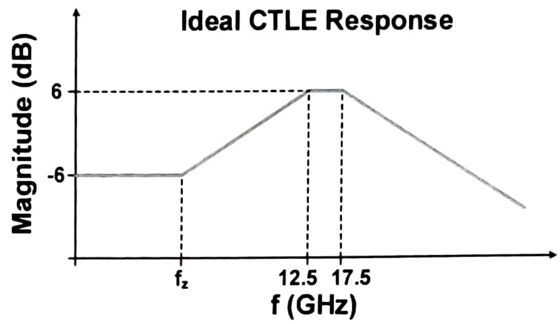
TABLE 13-1. Q_{BER} as a Function of the Bit Error Rate

BER	Q_{BER}	BER	Q_{BER}	BER	Q_{BER}
1×10^{-3}	6.180	1×10^{-10}	12.723	1×10^{-17}	16.987
1×10^{-4}	7.438	1×10^{-11}	13.412	1×10^{-18}	17.514
1×10^{-5}	8.530	1×10^{-12}	14.069	1×10^{-19}	18.026
1×10^{-6}	9.507	1×10^{-13}	14.698	1×10^{-20}	18.524
1×10^{-7}	10.399	1×10^{-14}	15.301	1×10^{-21}	19.010
1×10^{-8}	11.224	1×10^{-15}	15.882	1×10^{-22}	19.484
1×10^{-9}	11.996	1×10^{-16}	16.444	7.7×10^{-24}	20.000

Problem 1 (35 points)

This problem involves the design of an active continuous-time linear equalizer (CTLE) for a 25Gb/s system. The CTLE should have a bandwidth of 17.5GHz, an ideal peaking at 12.5GHz that is 12dB higher than the low-frequency gain of -6dB. **Assuming the maximum zero frequency**, give the input transistor's g_m and the values for R_D, R_S, and C_S. You can neglect all of the transistor capacitors, i.e. only consider capacitors that are explicitly drawn in your analysis. Also assume that all transistors operate in the saturation region and have infinite output resistance.





$$H(s) = \left(\frac{g_m}{C_p}\right) \frac{s + \frac{1}{R_S C_S}}{\left(s + \frac{1 + g_m R_S/2}{R_S C_S}\right)\left(s + \frac{1}{R_D C_p}\right)}$$

$$\omega_{p2} = 2\pi f_{p2} = \frac{1}{R_D C_p} \Rightarrow R_D = \frac{1}{2\pi f_{p2} C_p} = \frac{1}{2\pi (17.5GHz)(10fF)} = 910\Omega$$

$$\text{Ideal Peaking} = \frac{\omega_{p1}}{\omega_z} = 12dB = 4 \Rightarrow \omega_z = \frac{\omega_{p1}}{4} = \frac{2\pi(12.5GHz)}{4} = 2\pi(3.125GHz)$$

$$\text{Gain BW} = A_{DC}\frac{\omega_{p1}}{\omega_z}\omega_{p2} = \frac{1}{2}(4)(2\pi\, 17.5GHz) = 2\pi(35GHz)$$

$$\frac{g_m}{C_p} = 2\pi(35GHz) \Rightarrow g_m = 2\pi(35GHz)(10fF) = 2.2mA/V$$

$$\text{DC gain} = \frac{g_m R_D}{1 + \frac{g_m R_S}{2}} = \frac{1}{2} \Rightarrow R_S = \frac{\left(g_m R_D - \frac{1}{2}\right)4}{g_m} = \frac{6}{g_m} = 2.73k\Omega$$

$g_{m1,2}$ = $2.2\, mA/V$

R_D = 910Ω

R_S = $2.73k\Omega$

C_S = $18.7fF$

$$\omega_z = \frac{1}{R_S C_S} \Rightarrow C_S = \frac{1}{R_S \omega_z} = \frac{1}{(2.73k\Omega)(2\pi)(3.125GHz)} = 18.7fF$$

i. If I want to decrease the ideal peaking ratio to 6dB without changing the first pole, ω_{p1}, how should I change the CTLE?

$$\text{ideal peaking ratio} = 1 + \frac{g_m R_S}{2} = 2$$

$$\Rightarrow \text{Change } R_S \text{ to } R_S = \frac{2}{g_m} = \frac{2}{2.2\text{mA/V}} = 910\Omega$$

However, this will have some impact on ω_{p1}, so we need to change C_S also

$$\omega_{p1} = \frac{1 + g_m R_S/2}{R_S C_S} \Rightarrow C_S = \frac{1 + g_m R_S/2}{R_S \omega_{p1}} = \frac{2}{(910\Omega)(2\pi)(12.5\text{GHz})}$$

$$\boxed{\begin{matrix} R_S = 910\Omega \\ C_S = 28\text{fF} \end{matrix}}$$

ii. If I want to move the zero frequency f_z to 1GHz without impacting the original ideal peaking ratio of 12dB, how should I change the CTLE?

$$\text{Ideal Peaking Ratio} = \frac{\omega_{p1}}{\omega_z} = \frac{1 + \frac{g_m R_S}{2}}{R_S C_S}(R_S C_S)$$

$$= 1 + \frac{g_m R_S}{2}$$

$$\omega_z = \frac{1}{R_S C_S} \Rightarrow \text{Can tune } C_S \text{ w/o impacting peaking}$$

$$C_S = \frac{1}{R_S \omega_z} = \frac{1}{(2.73k\Omega)(2\pi)(1\text{GHz})}$$

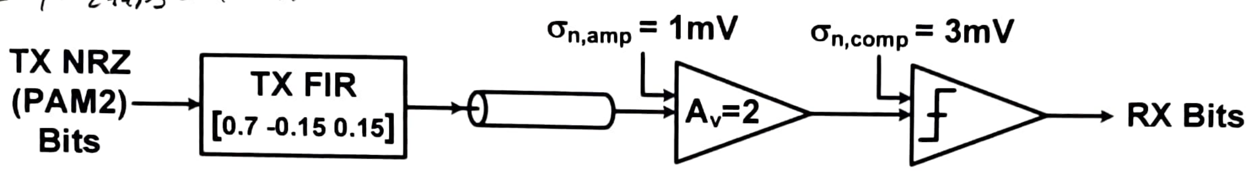
$$\boxed{C_S = 58.3\text{fF}}$$

Problem 2 (30 points)

This problem involves the voltage noise budgeting of a serial link system. Here we will conservatively assume that all distributions combine in a worst-case manner. The system consists of a transmitter with a 3-tap FIR filter which sends NRZ bits over a channel to a receiver modeled as a simple amplifier followed by a comparator. Each receiver block has a noise component which should be referred to the receiver input.

$\sigma_{Rx} = \sqrt{1^2 + \left(\frac{3}{2}\right)^2} = 1.81mV$

Attenuation $= 1 - \Sigma taps = 1 - 0.7 = 0.3$



Complete the following noise budget table assuming a TX peak differential swing of 0.5V_{ppd} and a target BER=10^{-15}. You can refer to the Q_{BER} table on page 2 if needed. (10 points)

Parameter	K_n	RMS	Value (BER=10^{-15})
Peak Differential Swing, V_{swing}			0.5V
RX Offset + Sensitivity			5mV
Power Supply Noise			10mV
Residual ISI	0.05		= 25mV
Crosstalk	0.05		= 25mV
Random Noise		= 1.81mV	= 28.7mV
Attenuation (TX FIR)	= 0.3		= 150mV
Total Noise			= 243.7mV
Differential Eye Height Margin			= 256.3mV

What is the minimum peak differential swing, V_{swing}, for a **BER=10^{-15}**, i.e. as the differential eye height margin goes to zero?

$V_{swing}(1 - \Sigma K_n) \geq$ Fixed Noise

$$V_{swing} \geq \frac{\text{Fixed Noise}}{1-\Sigma K_n} = \frac{43.7mV}{1-0.4} = 72.8mV$$

What is the minimum peak differential swing, V_{swing}, for a **BER=10^{-12}**, i.e. as the differential eye height margin goes to zero?

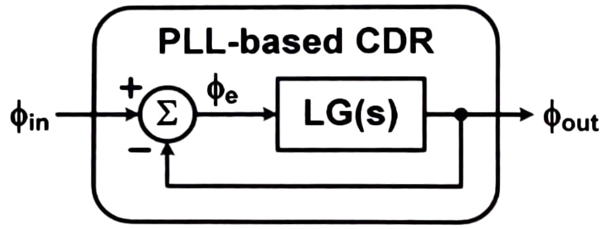
Fixed noise decreases due to consideration of less random noise

For $BER = 10^{-12} \Rightarrow RN = 14.069(1.81mV) = 25.5mV$

$$V_{swing} \geq \frac{40.5mV}{1-0.4} = 67.5mV$$

Problem 3 (35 points)

This problem investigates a simple PLL-based CDR which can be modeled by the simplified transfer function below. Assume that the only source of random noise in the PLL-based CDR below is from the VCO, which has $\kappa = 5\times10^{-9}\sqrt{s}$ and the PLL has a loop bandwidth f_L=10MHz. What is the **self-referenced accumulated rms jitter,** $\sigma_T = \sqrt{2}\sigma_x$?



$$\frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{LG(s)}{1+LG(s)} \approx \frac{1}{1+\frac{s}{2\pi f_L}}$$

$$\sigma_T = \sqrt{2}\,\sigma_x = K\sqrt{\Delta T} = K\sqrt{\frac{1}{2\pi f_{PLL}}}$$

$$= 5\times10^{-9}\sqrt{s}\sqrt{\frac{1}{2\pi(10MHz)}} = 631 fs$$

σ_T = 631 fs

Assume that the PLL is used in a 25Gb/s NRZ half-rate system and the 12.5GHz VCO has a duty cycle error of ±1ps which you can model as a deterministic jitter component, DJ=2ps. Including this DJ and the **transmit-clock referenced** σ_x above, what is the 25Gb/s timing margin for a BER=10^{-15}?

Total jitter (BER = 10^{-15}) = DJ + Qσ_x = 2ps + 15,882$\left(\frac{631 fs}{\sqrt{2}}\right)$ = 9.09 ps

Timing Margin = 40ps − 9.09ps = 30.91ps

= 0.77 UI

25Gb/s timing margin (BER=10^{-15}) = 30.91 ps

Using this timing margin value and assuming that the input data has ONLY a sinusoidal jitter component, sketch the jitter tolerance plot versus frequency. Label the high frequency timing margin and the key frequencies and slopes in the plot.

$$JTOL(s) = \frac{TM}{1-\frac{\Phi_{out}(s)}{\Phi_{in}(s)}}$$