# Texas A&M University Department of Electrical and Computer Engineering

# ECEN 720 - High-Speed Links

## Spring 2017

#### Exam #2

Instructor: Sam Palermo

- Please write your name in the space provided below
- Please verify that there are 7 pages in your exam
- You may use one double-sided page of notes and equations for the exam
- Good Luck!

Problem	Score	Max Score	
1		30	
2		30	
3		30	
4		10	
Total		100	

Name:	SAM PALERMO			
UIN:				

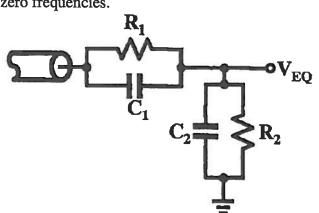
TABLE 13-1.  $Q_{\rm BER}$  as a Function of the Bit Error Rate

BER	$Q_{\mathrm{BER}}$	BER	$Q_{\mathtt{BER}}$	BER	$Q_{BER}$
$   \begin{array}{c}     1 \times 10^{-3} \\     1 \times 10^{-4} \\     1 \times 10^{-5} \\     1 \times 10^{-6} \\     1 \times 10^{-7} \\     1 \times 10^{-8} \\     1 \times 10^{-9}   \end{array} $	6.180 7.438 8.530 9.507 10.399 11.224 11.996	$   \begin{array}{c}     1 \times 10^{-10} \\     1 \times 10^{-11} \\     1 \times 10^{-12} \\     1 \times 10^{-13} \\     1 \times 10^{-14} \\     1 \times 10^{-15} \\     1 \times 10^{-16}   \end{array} $	12.723 13.412 14.069 14.698 15.301 15.882 16.444	$   \begin{array}{c}     1 \times 10^{-17} \\     1 \times 10^{-18} \\     1 \times 10^{-19} \\     1 \times 10^{-20} \\     1 \times 10^{-21} \\     1 \times 10^{-22} \\     7.7 \times 10^{-24}   \end{array} $	16.987 17.514 18.026 18.524 19.010 19.484 20.000

#### Problem 1 (30 points)

### **RX Passive CTLE Equalization**

Design the passive CTLE below to achieve 12dB peaking, HF Gain = 0.9V/V, and a 2GHz zero frequency. Use a total resistance ( $R_1+R_2$ ) of 500 $\Omega$ . Sketch the Bode plot and label the pole and zero frequencies.



$$H(s) = \frac{R_2}{R_1 + R_2} \frac{1 + R_1 C_1 s}{1 + \frac{R_1 R_2}{R_1 + R_2} (C_1 + C_2) s}$$

$$HF$$
 gain =  $\frac{C_1}{C_1+C_2} = 0.9 \% = -0.915d$ 

$$LFgain = \frac{R_2}{R_1 + R_2} = 6.226 v = -12,92d.$$

Peaking = 
$$(0.9)(\frac{500N}{R_2}) = 3.98$$

$$W_2 = 2TT(2GHz) = \frac{1}{R_1C_1}$$
  $W_p = \frac{\frac{1}{R_1R_2}(C_1+C_2)}{R_1+R_2} = 7.96GHz$ 

$$C_2 = \frac{0.1}{0.9}C_1 = \frac{206FF}{9} = 22.9FF$$

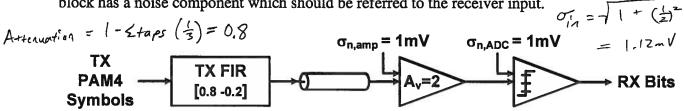
$$R_1 = 387 \Omega$$

$$R_2 = 113 \Omega$$

$$C_2 = 22.9 FF$$

Problem 2 (30 points)

This problem involves the voltage noise budgeting of a serial link system with PAM4 modulation. Here we will conservatively assume that all distributions combine in a worst-case manner. The system consists of a transmitter with a 3-tap FIR filter which sends PAM4 symbols over a channel to a receiver modeled as a simple buffer followed by a 2-bit ADC. Each receiver block has a noise component which should be referred to the receiver input.



Complete the following noise budget table assuming a TX peak differential swing of  $1V_{ppd}$  and a target BER= $10^{-12}$ . You can refer to the  $Q_{BER}$  table on page 2 if needed. (20 points)

Parameter	Kn	RMS	Value (BER=10 <sup>-12</sup> )
Peak Differential Swing, V <sub>swing</sub>			1V
RX Offset + Sensitivity			10mV
Power Supply Noise			10mV
Residual ISI (compute from max. transition)	0.05		= 50mV
Crosstalk (compute from max. transition)	0.05		= 50mV
Random Noise		= 1.(2mV	= 15.76mV
Attenuation (from TX FIR & modulation)	= 0,8		= 800mV
Total Noise		350000	= 935.76mV
Differential Eye Height Margin			= 64,24mV

What is the minimum peak differential swing,  $V_{swing}$ , for a **BER=10**-12, i.e. as the differential eye height margin goes to zero for the PAM4 system? (10 points)

Vswing 
$$(1-4k_N) \ge Fixed Noise$$
  
Vswing  $\ge \frac{Fixed Noise}{1-4k_N} = \frac{35,76mV}{1-6.9}$ 

Min.  $V_{\text{swing}}(PAM4) = 358 \text{mV}$ 

#### Problem 3 (30 points)

This problem involves designing a TX PLL loop bandwidth to satisfy a system jitter budget, given the following jitter components from the TX, channel, and RX. What is the maximum TX random rms jitter,  $\sigma_{RJ,TX}$ , for a BER=10<sup>-12</sup> at a 25Gb/s data rate? Assume that the only source of random noise in the TX PLL below is from the VCO, which has  $\kappa = 10^{-8} \sqrt{s}$ , and that the jitter  $\sigma$  of interest is closed-loop and referenced to an ideal clock. What is the necessary TX PLL loop bandwidth to satisfy the system jitter budget?

Channel DJ = 5ps 
$$RX$$
 $\sigma_{RJ} = ?$ 

DJ = 3ps

 $\partial F = |O|^{-1/2} \Rightarrow \partial F = |A| = |A|$ 

Max 
$$\sigma_{RJ,TX}$$
 (w/ DR=25Gb/s) =  $1.72\rho$ S

PLL Loop Bandwidth (Hz) =  $2.69MHz$ 

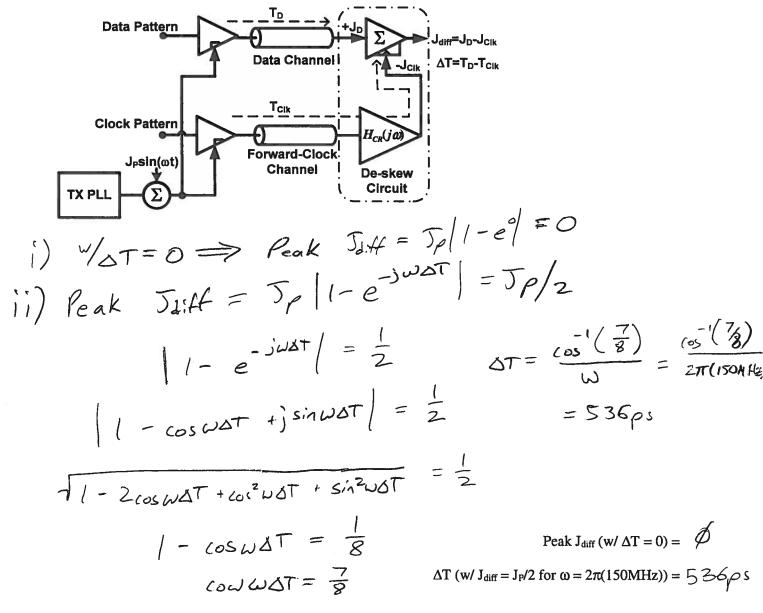
#### Problem 4 (10 points)

The figure below models a forwarded-clock system with a receiver de-skew circuit with a jitter transfer function of  $H_{CR}(j\omega)$  and a skew between the data channel and clock channel of  $\Delta T$ . Assuming a common sinusoidal jitter component with amplitude,  $J_p$ , and frequency,  $\omega$ , on the forwarded clock and the data, the magnitude of the peak differential jitter at the receiver sampler is equal to

Peak 
$$J_{diff} = J_p |1 - e^{-j\omega \Delta T}| H_{CR}(j\omega)|$$

Assuming that the de-skew circuit displays an all-pass jitter transfer characteristic, i.e.  $|H_{CR}(j\omega)| = 1$ , calculate the following:

- i) What is the Peak  $J_{diff}$  if  $\Delta T = 0$ ?
- ii) If the jitter frequency is  $\omega=2\pi(150\text{MHz})$ , what is the allowable skew,  $\Delta T$ , for the Peak  $J_{diff}=\frac{J_p}{2}$ ?



# **Scratch Paper**