Texas A&M University
Department of Electrical and Computer Engineering

ECEN 720 – High-Speed Links

Spring 2025

Exam #1

Instructor: Sam Palermo

- Please write your name in the space provided below
- Please verify that there are **6** pages in your exam
- Good Luck!

Problem	Score	Max Score
1		30
2		30
3		20
4		20
Total		**100**

Name: SAM PALERMO

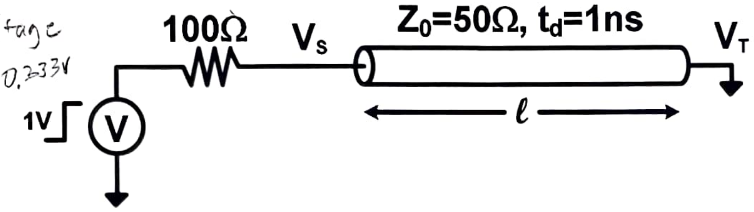
UIN:

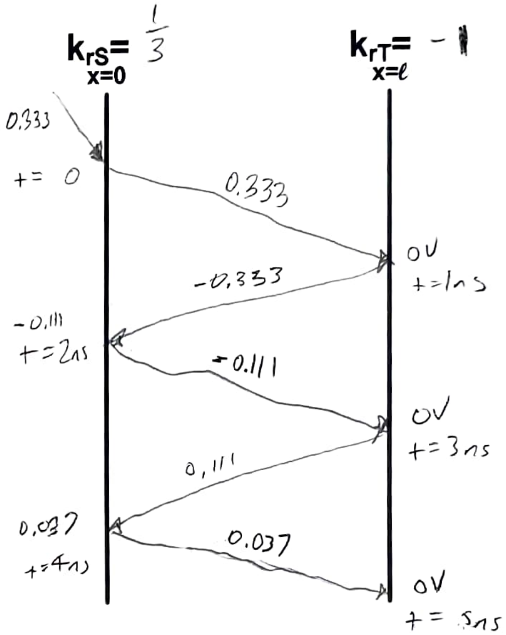
Problem 1 (30 points)

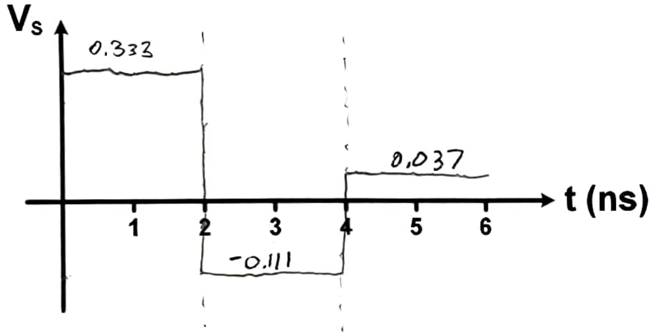
a) A 1V step is launched onto the channel below at t=0ns. (20 points)
   i. Calculate the reflection coefficient at the source, k_{rS}, and at the end termination, k_{rT}
   ii. Fill in the lattice diagram below until the source voltage, V_S, has reached to within 100mV of its final value.
   iii. Also plot the source voltage, V_S, and make sure to label the voltage values in the transient plot.

Initial Voltage

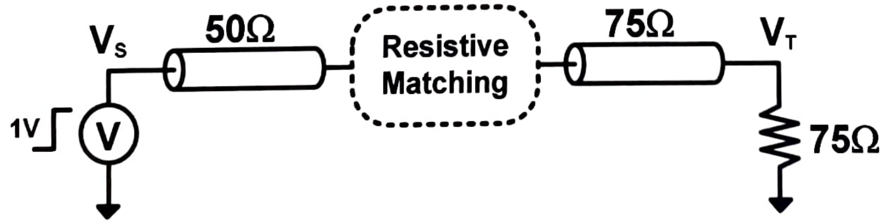
$1V\left(\frac{50}{150}\right) = 0.333V$



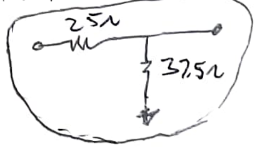


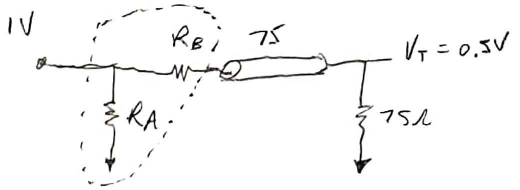


b) For the circuit below, design a resistive matching network to eliminate any reflections of the forward traveling wave originating from the source, V_S, and also produce an output voltage V_T=0.5V with a 1V input step. (10 points)



Another Solution #2





* To make $V_T = 0.5V \Rightarrow R_B = 75\Omega$

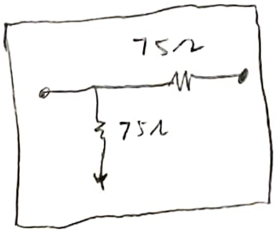
* To satisfy no reflections

$$R_A \| (R_B + 75) = 50$$

$$\frac{R_A(150)}{R_A + 150} = 50$$

$$R_A = 75\Omega$$

Solution #1

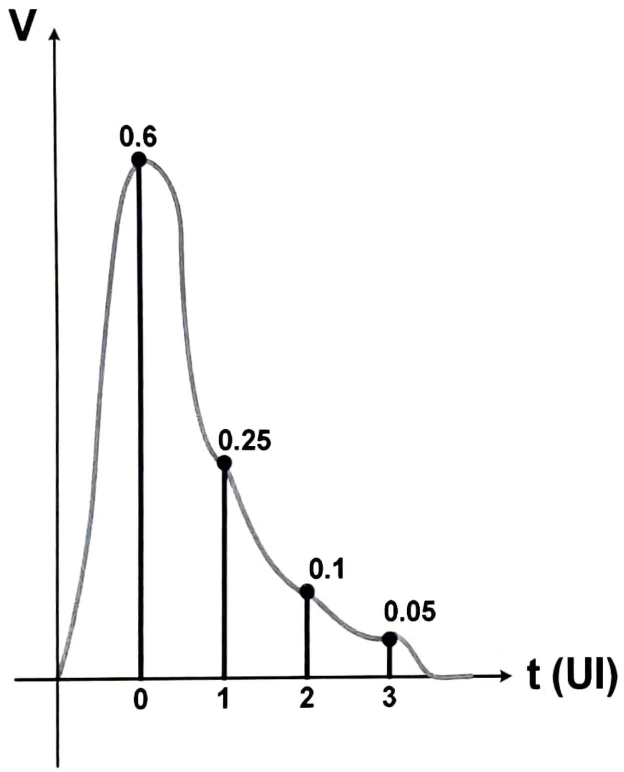


Problem 2 (30 points)

A channel has the pulse response, $y^{(1)}$, below for a "1" symbol.

a. Find the channel's worst-case eye height at this bit rate for **PAM2** modulation.
b. Give the channel's worst-case **PAM2** bit pattern at this bit rate. Make sure to label the cursor in the bit pattern.
c. Find the channel's worst-case eye height at this symbol rate for **PAM4** modulation.

$$y^{(1)} = [0.6\ \ 0.25\ \ 0.1\ \ 0.05]$$



$y_0^{(1)} = 0.6$

$\sum_{k \neq 0} y_k^{(1)} \Big|_{y<0} = 0$

$\sum_{k \neq 0} y_k^{(1)} \Big|_{y>0} = 0.25 + 0.1 + 0.05$
$= 0.4$

PAM2 W.C. Eye Height

$2(0.6 - 0.4) = 0.4$

PAM2 W.C. Bit Pattern

$[0.6\ \ 0.25\ \ 0.1\ \ 0.05] \Longrightarrow [-0.05\ \ -0.1\ \ -0.25\ \ \underset{\updownarrow \text{cursor}}{0.6}]$

$\Downarrow$

$[-1\ \ -1\ \ -1\ \ 1]$

PAM4 W.C. Eye Height; $2\left(\frac{0.6}{3} - 0.4\right) = -0.4$

PAM2 Worst-Case Eye Height = 0.4

PAM2 Worst-Case Bit Pattern = $[-1\ \ -1\ \ -1\ \ \overset{\text{Cursor}}{\overset{\downarrow}{1}}]$ (Worst case "1")

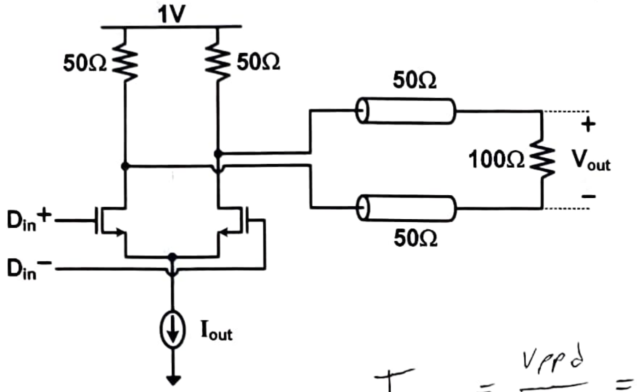
PAM4 Worst-Case Eye Height = -0.4

Problem 3 (20 points)

Answer the following questions for the current-mode driver below

i. Calculate the tail current I_{out} to generate a peak-to-peak differential voltage output swing of $0.6V_{ppd}$.

ii. Give the common-mode value of the output voltage with the $0.6V_{ppd}$ output swing.



$$I_{OUT} = \frac{V_{ppd}}{R} = \frac{0.6V}{50\Omega} = 12mA$$

During "1" bit $V_{OUT}^{+} = 0.85V$ $V_{OUT}^{-} = 0.55V$

"-1" bit $V_{OUT}^{+} = 0.55V$ $V_{OUT}^{-} = 0.85V$

$$V_{OUT,CM} = \frac{0.85 + 0.55}{2} = 0.7V$$

I_{out} = 12mA

$V_{out,CM}$ = 0.7V

Problem 4 (20 points)

For the circuit below, use the following NMOS parameters

$KP_N=\mu_n C_{ox}=600\mu A/V^2$, $V_{TN}=0.35V$, $\lambda_N=0V^{-1}$

and the following PMOS parameters

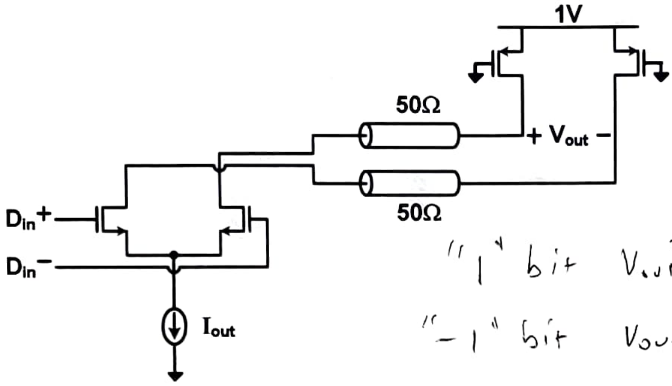
$KP_P=\mu_p C_{ox}=150\mu A/V^2$, $V_{TP}=-0.35V$, $\lambda_P=0V^{-1}$

For the current-mode driver below

i. Calculate the tail current I_{out} to generate a peak-to-peak differential voltage output swing of $600mV_{ppd}$.

ii. Give the common-mode value of the output voltage with the $600mV_{ppd}$ output swing.

iii. Give the PMOS termination transistors aspect ratios for proper termination. Include V_{SD} effects and optimize the termination at the output common-mode level.



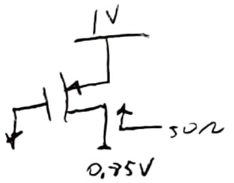
$$I_{OUT} = \frac{V_{ppd}}{2R} = \frac{600mV}{2(50)} = 6mA$$

"1" bit $V_{out}^{+} = 1V$ $V_{out}^{-} = 1V - 6mA(50\Omega) = 0.7V$

"−1" bit $V_{out}^{+} = 0.7V$ $V_{out}^{-} = 1V$

$$V_{OUT,cm} = \frac{1+0.7}{2} = 0.85V$$

* Sizing PMOS termination at common-mode level



$$R_P = \frac{1}{g_o} = \frac{1}{KP_P \frac{W}{L}(V_{SG} - |V_{TP}| - V_{SD})}$$

$$\left(\frac{W}{L}\right)_P = \frac{1}{R_P KP_P (V_{SG} - |V_{TP}| - V_{SD})} = \frac{1}{(50\Omega)(150\mu A/V^2)(1V - 0.35V - 0.15V)}$$

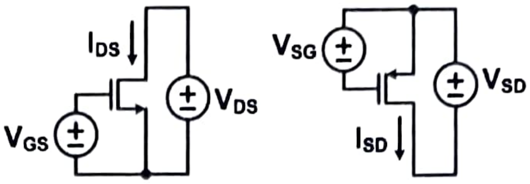
$$= 267$$

$I_{out} =$ 6mA

$V_{out,CM} =$ 0.85V

$(W/L)_P =$ 267

Key MOS Equations & Scratch Paper



$$\text{Saturation: } NMOS\ \ I_{DS} = \frac{1}{2}KP_N\frac{W}{L}(V_{GS} - V_{TN})^2$$

$$\text{Saturation: } \ PMOS\ \ I_{SD} = \frac{1}{2}KP_P\frac{W}{L}(V_{SG} - |V_{TP}|)^2$$

$$\text{Triode: NMOS } \ I_{DS} = KP_N\frac{W}{L}\left(V_{GS} - V_{TN} - \frac{V_{DS}}{2}\right)V_{DS}$$

$$\text{Triode: } PMOS\ I_{SD} = KP_P\frac{W}{L}\left(V_{SG} - |V_{TP}| - \frac{V_{SD}}{2}\right)V_{SD}$$

$$NMOS\ g_m = \frac{\partial I_{DS}}{\partial V_{GS}},\ \ PMOS\ g_m = \frac{\partial I_{SD}}{\partial V_{SG}}$$

$$NMOS\ \ g_o = \frac{\partial I_{DS}}{\partial V_{DS}},\ \ PMOS\ \ g_o = \frac{\partial I_{SD}}{\partial V_{SD}}$$